PRODUCT SPECIFICATION FOR LCD MODULE

Revision: 1.0

Model No: LSC064I01-MP-V1

Module Type: COG+FPC+B/L

APPROVED SIGNATURE

■ Approved Product Specification only

□ Approved Product Specification and Samples

Prepared By	Checked By	Approved By

Contents

目录

1. General Description

LSC064I01-MP-V1 is a transmissive type a-Si TFT-LCD (amorphous silicon thin film transistor liquid crystal display) module, which is composed of a TFT-LCD panel, a driver circuit and a backlight unit. The panel size is 6.4 inch and the resolution is 1440(RGB)*2560, the panel can display up to 16.7M colors.

2. Physical Features

Display Mode	TFT-LCD Module
	Active matrix TFT, Transmissive type
Display Format	Graphic 1440(RGB)×2560 Dot-matrix
Input Data	MIPI
Viewing Direction（Grayscale Inversion）	Free（IPS）
Drive	R63419

3. Mechanical Specification

Item	Specification	Unit
Module size (H×V×D)	80.84 ×148.92 ×1.475	mm
Number of dots	1440(RGB) ×2560	pixel
Active area (H×V)	78.84×140.16	mm

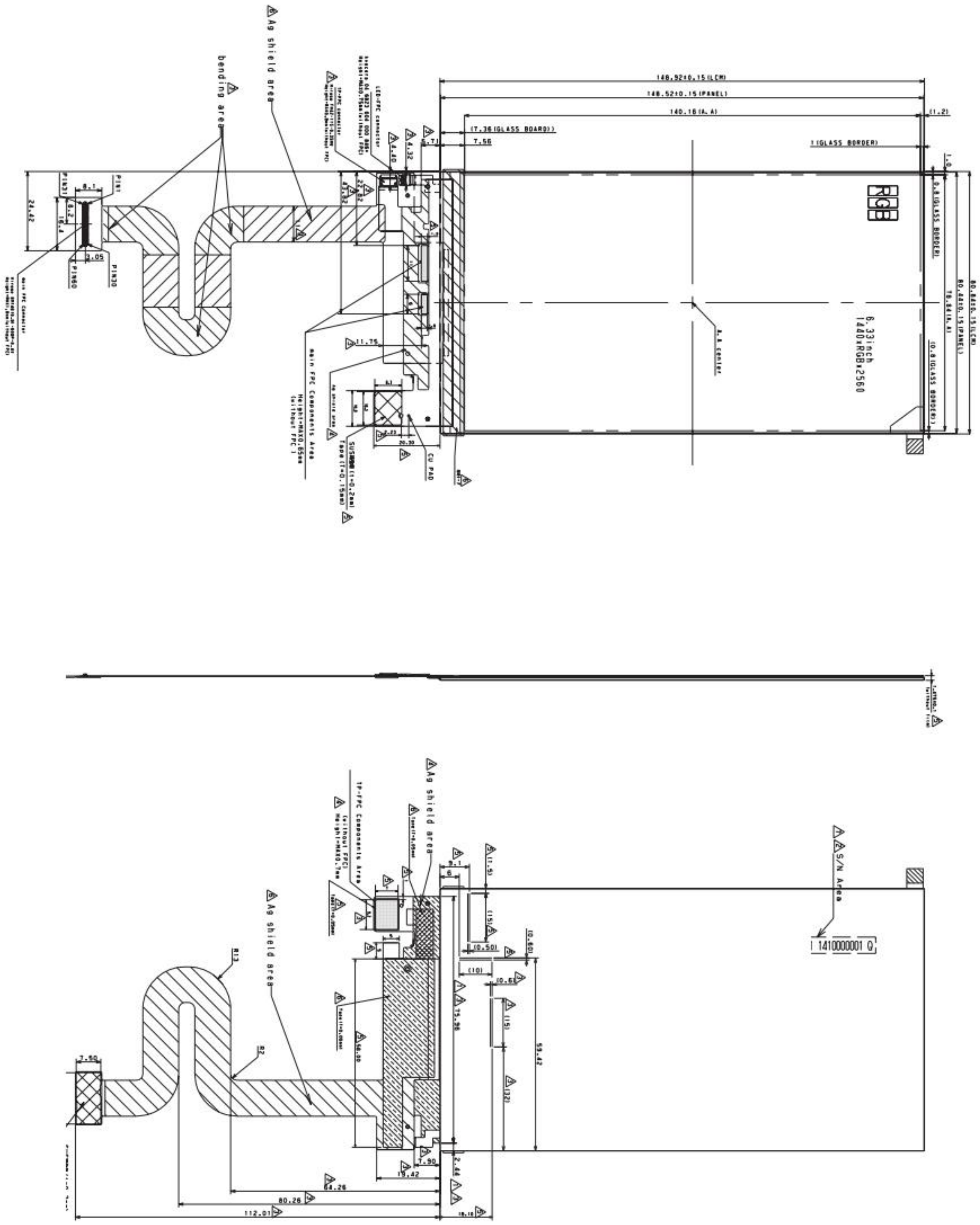
4. Outline Dimension

NOTE

1) Dimensions with branket( ) are reference value
2) Any foreign materials and contamination outside the Active area are to be treated as "NO-Count" at our inspections
3) Guarantee of appearance = LCD Active Area
4) When the set is not properly designed. It is possible that backlight light may leak from the gap at outside of black-mask area which is located at outside of active area.so,please pay attentions to try not to cause such leakage when designing the set.
5) Warpage≤0.3

Pin Assignment

No.	Name	No.	Name
1	DSIB_D3_N	31	GND
2	DSIB_D3_P	32	LED2-
3	GND	33	LED1-
4	DSIB_D0_N	34	LED2+
5	DSIB_D0_P	35	LED1+
6	GND	36	GND
7	DSIB_CLK_N	37	VDDH_3.3V
8	DSIB_CLK_P	38	GND
9	GND	39	/RST
10	DSIB_D1_N	40	INT
11	DSIB_D1_P	41	GND
12	GND	42	SDA
13	DISB_D2_N	43	SCL
14	DISB_D2_P	44	GND
15	GND	45	VBUS
16	DSIA_D2_P	46	VDD_3.3V
17	DSIA_D2_N	47	GND
18	GND	48	XRES
19	DSIA_D1_P	49	PWM
20	DSIA_D1_N	50	GND
21	GND	51	HSYNC
22	DSIA_CLK_P	52	TE
23	DSIA_CLK_N	53	GND
24	GND	54	VDDIO
25	DSIA_D0_P	55	AVDD-
26	DSIA_D0_N	56	AVDD+
27	GND	57	NC
28	DSIA_D3_P	58	CTSI/IDO
29	DSIA_D3_N	59	CTSI/IDI
30	GND	60	GND



5. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Remark
Supply Voltage	IOVCC-GND	-0.3	+4.6	V	*1
	VSP-GND	-0.3	+6.5	V	*1
	VSN-GND	-6.5	+0.3	V	*1

*1: Voltage applied to GND pins.GND pin conditons are based on all the same voltage(0V).
Always connect all GND externally and use at the same voltage.

Table 2-2 Touch panel Ta=25 ℃

Parameter	Symbol	Min	Max	Unit	Remark
Supply voltage	AVDD-GND	-0.3	3.6	V	*1
	VDDIN-GND	-0.3	3.6	V	*1
	VDDIO-GND	-0.3	3.6	V	*1

*1: Input terminal of logic system,SDA,SCL,INT.
Voltage value is based on GND=0V.

Environment Conditions

Table 3

Item	Top		Tstg		Remark
	MIN.	MAX.	MIN.	MAX.	
Ambient temperature	-20 ℃	+60℃	-30 ℃	+70℃	Note 2)
Humidity	Note 1)		Note 1)		No condensation

Note1) Ta ≤ 40 °C.......90% RH Max
Note2) Ta > 40 °C.......Absolute humidity shall be less than Ta=40 °C /90 % RH.

As opt-electrical characteristics of LCD will be changed, dependent on the temperature, the confirmation of display quality and characteristics has to be done after temperature is set at 25 ℃ and it becomes stable.

Be sure not to exceed he rated voltage, otherwise a malfunction may occur.

6. Electrical Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Applicable Pin
LCD Supply voltage1	IOVCC-GND	Ta=-20~60 °C	1.7	1.8	1.9	V	(note 1)
LCD Supply voltage2	VSP-GND	Ta=-20~60 °C	5.8	5.9	6.0	V	(note 1)
LCD Supply voltage3	VSN-GND	Ta=-20~60 °C	-6.0	-5.9	-5.8	V	(note 1)
"H" level input voltage	V_{IH}	Ta=-20~60 °C	0.7 IOVCC	-	IOVCCV		(note 2)
"L" level input voltage	V_{IL}		0	-	0.3 IOVCC	V	
"H" level Input current	I_{IH}	Ta=-20~60 °C	-	-	10	μA	
"L" level Input current	I_{IL}		-10	-	-	μA	
"H" level Output voltage	V_{OH}	Ta=-20~60 °C	0.8 IOVCC	-	IOVCC	V	I_{OH}=-0.1mA
"L" level Output voltage	V_{OL}		-	-	0.2 IOVCC	V	I_{OL}=+0.1mA
MIPI high speed mode							
Common mode voltage High Speed receive mode	VCMRX(DC)	Ta=-20~60 °C	70		330	mV	(note 3)
Differential input high threshold voltage	VIDTH	Ta=-20~60 °C	-	-	70	mV	(Note 3)
Differential input low threshold voltage	VIDTL	Ta=-20~60 °C	-70	-	-	mV	(Note 3)
Single-ended input high voltage	VIHHS	Ta=-20~60 °C	-	-	460	mV	(Note 3)
Single-ended input low voltage	VILHS	Ta=-20~60 °C	-40	-	-	mV	(Note 3)
MIPI LP mode							
Logic High level input voltage	VIH	Ta=-20~60 °C	880		1350	mV	(Note 3)
Logic Low level input voltage	VIL	Ta=-20~60 °C	-50		550	mV	(Note 3)
Logic High level output voltage	VOH	Ta=-20~60 °C	1.1	1.2	1.3	V	(Note 3)
Logic Low level output voltage	VOL	Ta=-20~60 °C	-50		50	mV	(Note 3)
Logic 0 contention threshold	VILCD	Ta=-20~60 °C	-	-	200	mV	(Note 3)
Logic 1 contention threshold	VIHCD	Ta=-20~60 °C	450	-	-	mV	(Note 3)
LCD Current consumption	Iiovcc1	Ta=25 °C	-	24.33	30.34	mA	(note 4)
	Ivsp1	Ta=25 °C	-	22.22	29.47	mA	(note 4)
	Ivsn1	Ta=25 °C	-	17.29	22.94	mA	(note 4)
	Iiovcc1	Ta=25 °C	-	0.005	0.02	mA	(note 5)
	Ivsp1	Ta=25 °C	-	0.005	0.02	mA	(note 5)
	Ivsn1	Ta=25 °C	-	0.005	0.02	mA	(note 5)

(Note 1) Include Ripple Noise

(Note 2) Applied overshoot

(Note 3) VCMRX(DC)=(VP+VDN)/2;
Minimum 110mV/-110mV HS differential swing is required for display data transfer.

(Note 4) Measurement conditions: Ta=25℃Full screen white pattern, VSP=5.9V/VSN=-5.9V/IOVCC=1.8V, 60HZ Refresh MIPI-DSI Video bypass mode.

(Note5) Measurement conditions: Deep standby mode.

TP Electrical characteristics

TP Supply voltage1	VDDH_3.3V-GND	Ta=-20～60 °C	3.1	3.3	3.47	V	(note 1)
TP Supply voltage2	VDD_3.3V-GND	Ta=-20～60 °C	3.1	3.3	3.47	V	(note 1)

(Note 1) Include Ripple Noise

LED back light

(1) The back light uses 8*2pcs edge light type white LED.

Table 6

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit	Remark
Forward current	Ta=25 °C	I_{LED}	-	20*1	-	mA	LED1+/LED1- LED2+/LED2-

LED lamp: SHARP

*1 per one piece of LED

*Please consider Allowable Forward Current on used temperature
(refer to Ambient Temperature vs. Allowable Forward Current curve)

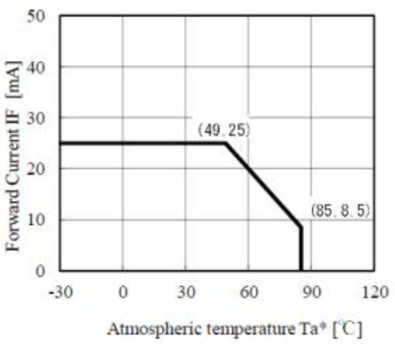


Fig.1 LED Characteristic(De-rating Curve)

(Ta*=25℃)

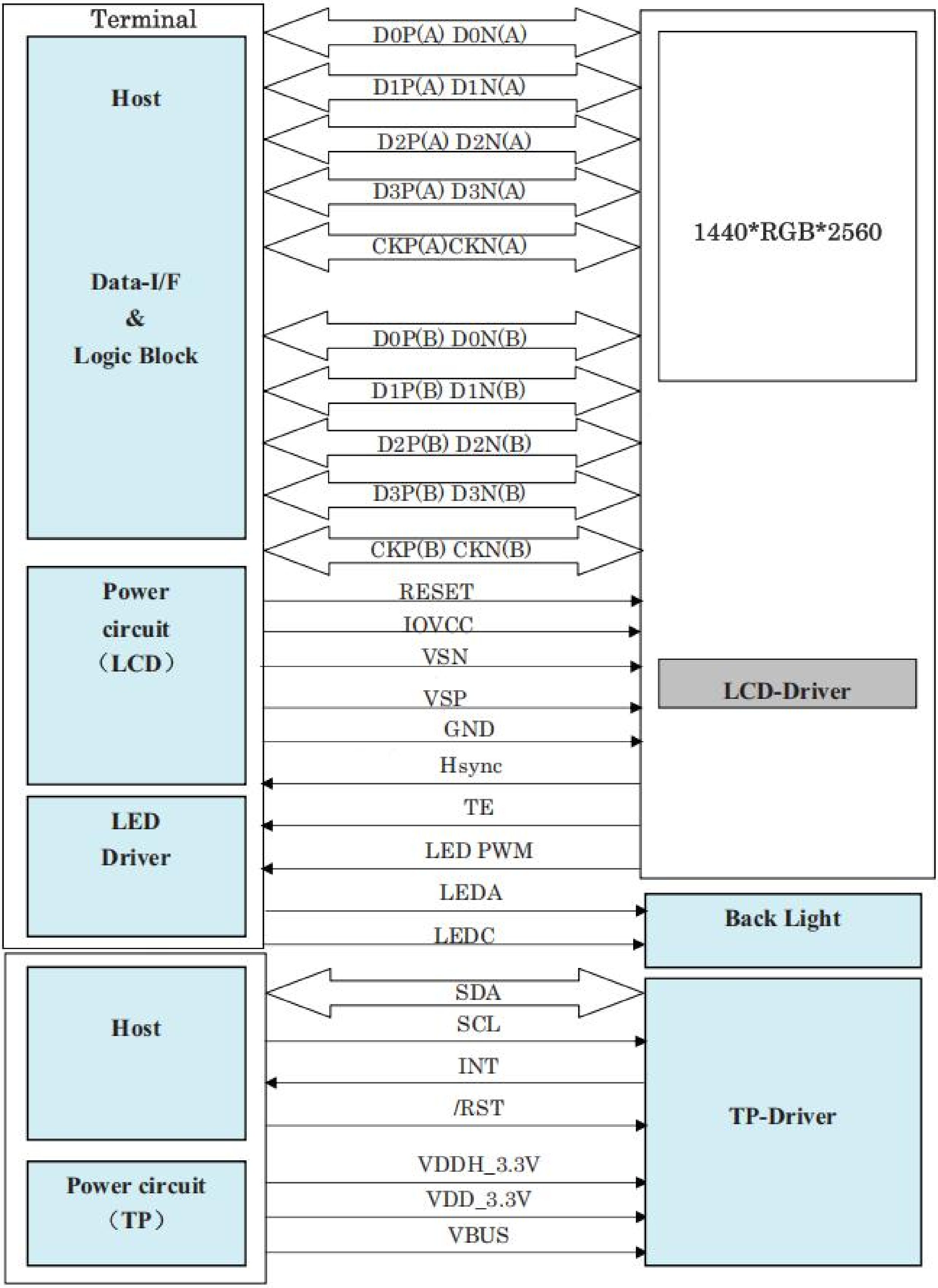
Parameter	Symbol	Rating	Unit
Power dissipation	P	77.5	mW
Forward current	I_F	25	mA
Peak pulsed forward current(*1)	I_{FM}	50	mA
Forward current derating factor	DC	-0.46	mA/℃
	Pulse	-0.67	mA/℃
Reverse voltage	V_R	5	V
Operating temperature(*3)	Topr	-30 to +85	°C
Storage temperature	T_{stg}	-40 to +90	°C

(Ta*=25℃)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Forward Voltage	V_F	I_F=20 mA	-	2.9	3.1	V
Luminous flux (*4)	Φv		6.10	6.7	-	lm
Chromaticity coordinates(*5)	x1		0. 26	0.273	0. 286	-
	y1		0. 24	0.253	0. 266	

7. Module Function Description

7-1. Block Diagram Of LCM



7-2. Pin Description

Table 7-1 LCD module Interface layout

Pin No	Symbol	Description	I/O	Remarks
1	DSIB_D3_N	MIPI DSI (-) of Port B	I	
2	DSIB_D3_P	MIPI DSI (+) of Port B	I	
3	GND	Ground	-	
4.	DSIB_D0_N	MIPI DSI (-) of Port B	I/O	
5	DSIB_D0_P	MIPI DSI (+) of Port B	I/O	
6	GND	Ground	-	
7	DSIB_CLK_N	MIPI DSI clock (-) of Port B	I	
8	DSIB_CLK_P	MIPI DSI clock (+) of Port B	I	
9	GND	Ground	-	
10	DSIB_D1_N	MIPI DSI (-) of Port B	I	
11	DSIB_D1_P	MIPI DSI (+) of Port B	I	
12	GND	Ground	-	
13	DSIB_D2_N	MIPI DSI (-) of Port B	I	
14	DSIB_D2_P	MIPI DSI (+) of Port B	I	
15	GND	Ground	-	
16	DSIA_D2_P	MIPI DSI (+) of Port A	I	
17	DSIA_D2_N	MIPI DSI (-) of Port A	I	
18	GND	Ground	-	
19	DSIA_D1_P	MIPI DSI (+) of Port A	I	
20	DSIA_D1_N	MIPI DSI (-) of Port A	I	
21	GND	Ground	-	
22	DSIA_CLK_P	MIPI DSI clock (+) of Port A	I	
23	DSIA_CLK_N	MIPI DSI clock(-) of Port A	I	
24	GND	Ground	-	
25	DSIA_D0_P	MIPI DSI (+) of Port A	I/O	
26	DSIA_D0_N	MIPI DSI (-) of Port A	I/O	
27	GND	Ground	-	
28	DSIA_D3_P	MIPI DSI (+) of Port A	I	
29	DSIA_D3_N	MIPI DSI (-) of Port A	I	
30	GND	Ground	-	
31	GND	Ground	-	
32	LED2-	LED back light power group2 negative	I	
33	LED1-	LED back light power group1 negative	I	
34	LED2+	LED back light power group2 positive	I	
35	LED1+	LED back light power group1 positive	I	
36	GND	Ground	-	
37	VDDH_3.3V	Power Input（3.3v）for TP	I	
38	GND	Ground	-	
39	/RST	Reset pin for TP	I	
40	INT	State change interrupt-TP	OD	
41	GND	Ground	-	
42	A	Serial interface data-TP	OD	43
	SCL	Serial interface dock-TP	OD	44
	GND	Ground	-	45
	VBUS	Power input-TP	I	
46	VDD_3.3V	Power input（3.3v）-TP	I	
47	GND	Ground	-	
48	XRES	Device reset signal	I	
49	PWM	Backlight LED driver PWM	O	
50	GND	Ground	-	
51	*HSYNC*	*Horizontal Synchronizing signal*	*O*	
52	TE	Tearing signal output from driver IC	O	

53	GND	Ground	-	
54	VDDIO	Power supply for I/O	-	
55	AVDD-	Power supply for source negative	-	
56	AVDD+	Power supply for source positive	-	
57	NC	NC	-	
58	CTSI/ID0	ID(connect to GND in FPC)		
59	CTSI/ID1	ID(connect to GND in FPC)		
60	GND	Ground	-	

Mounted connector : 60pins; 0.4mm pitch; B to B connector. (HIROSE- BM14B(0.8)-60DP-0.4V)

Corresponded connector : 60pins; 0.4mm pitch; B to B connector. (HIROSE- BM14B(0.8)-60DS-0.4V)

Signals connect to LCD module. Symbols correspond able to Circuit diagram in Page 12.

Table 7-2 Touch Panel Interface layout

Pin No	Symbol	Description	I/O	Remarks
1	GND	Ground	-	
2	VDDH_3.3V(AVDD)	Power Input（3.3v）for TP(AVDD)	I	
3	GND	Ground	-	
4	/RST	Reset pin for TP	I	
5	INT	State change interrupt-TP	OD	
6	GND	Ground	-	
7	SDA	Serial interface data-TP	I/O	
8	SCL	Serial interface dock-TP	OD	
9	GND	Ground	-	
10	VBUS(VDDIO)	Power input-TP(VDDIO)	I	
11	VDD_3.3V(VDDIN)	Power input（3.3v）-TP(VDDIN)	I	

Mounted connector : 11pins; 0.6mm pitch; ZIF connector. (HIROSE- FH42-11S-0.3SHW)

Signals connect to TP module. Symbols correspond able to Circuit diagram in Page 13.

7-3 Timing Characteristics

<DC characteristics>

Item		Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
HS-RX	Differential input high threshold	VIDTH	mV	IOVDD= 1.65V~3.30V	-	-	70	2
	Differential input low threshold	VIDTL	mV	IOVDD= 1.65V~3.30V	-70	-	-	2
	Single-ended input low voltage	VILHS	mV	IOVDD= 1.65V~3.30V	-40	-	-	
	Single-ended input high voltage	VIHHS	mV	IOVDD= 1.65V~3.30V	-	-	460	
	Common-mode voltage HS receive mode	VCMRX(DC)	mV	IOVDD= 1.65V~3.30V	70	-	330	1
	Differential input impedance	ZID	Ω	IOVDD= 1.65V~3.30V	-	100	-	
LP-RX	Logic 0 input voltage not in ULP State	VIL	mV	IOVDD= 1.65V~3.30V	-50	-	550	
	Logic 1 input voltage	VIH	mV	IOVDD= 1.65V~3.30V	880	-	1350	
	I/O leakage current	ILEAK	μA	Vin = -50mV - 1350mV	-10	-	10	
LP-TX	Thevenin output low level	VOL	mV	IOVDD= 1.65V~3.30V	-50	-	50	
	Thevenin output high level	VOH	V	IOVDD= 1.65V~3.30V	1.1	1.2	1.3	
	Output impedance of LP transmitter	ZOLP	Ω	IOVDD=1.80V	110	-	-	
CD-RX	Logic 0 contention threshold	VILCD	mV	IOVDD= 1.65V~3.30V	-	-	200	
	Logic 1 contention threshold	VIHCD	mV	IOVDD= 1.65V~3.30V	450	-	-	

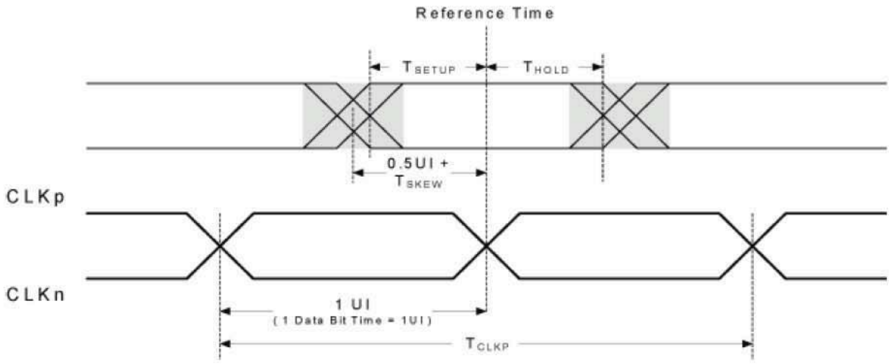
Notes: 1. VCMRX (DC) = (VP+VDN)/2

2. Minimum 110mV/-110mV HS differential swing is required for display data transfer.

<AC Characteristics>

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
DSICLK Frequency	fDSICLK	MHz	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	100	-	500	1
DSICLK Cycle time	tCLKP	ns	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	1	-	10	
DSI Data Transfer Rate	tDSIR	Mbps	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V DSI 2 lanes, 3 lanes,4lane	200	-	1000	1
Data to Clock Setup Time	tSETUP	UI	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	0.15	-	-	3
		ns	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	0.15	-	-	2 ,3
Clock to Data Hold Time	tHOLD	UI	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	0.15	-	-	3
		ns	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	0.15	-	-	2,3

Notes:
1. When fDSICLK<125MHz, change auto load NV setting so that it is compliant with THS-PREPARE+THS-ZERO spec.
2. Minimum tSETUP/tHOLD Time is 0.15UI. This value may change according to DSI transfer rate.
3. tSETUP/tHOLD Time are measured without HS-TX Jitter.



(6) Reset Timing Characteristics

Table 31

Item	Symbol	Unit	Test condition	Min.	Max.
Reset low-level width1	tRW1	us	Power supply on	1000	—
Reset low-level width2	tRW2	us	Operation	1000	—
Reset time (Sleep IN)	tRT1	ms	—	—	3
Reset time (Sleep OUT)	tRT2	ms	—	—	3
Noise reject width	tRESNR	us	—	—	1

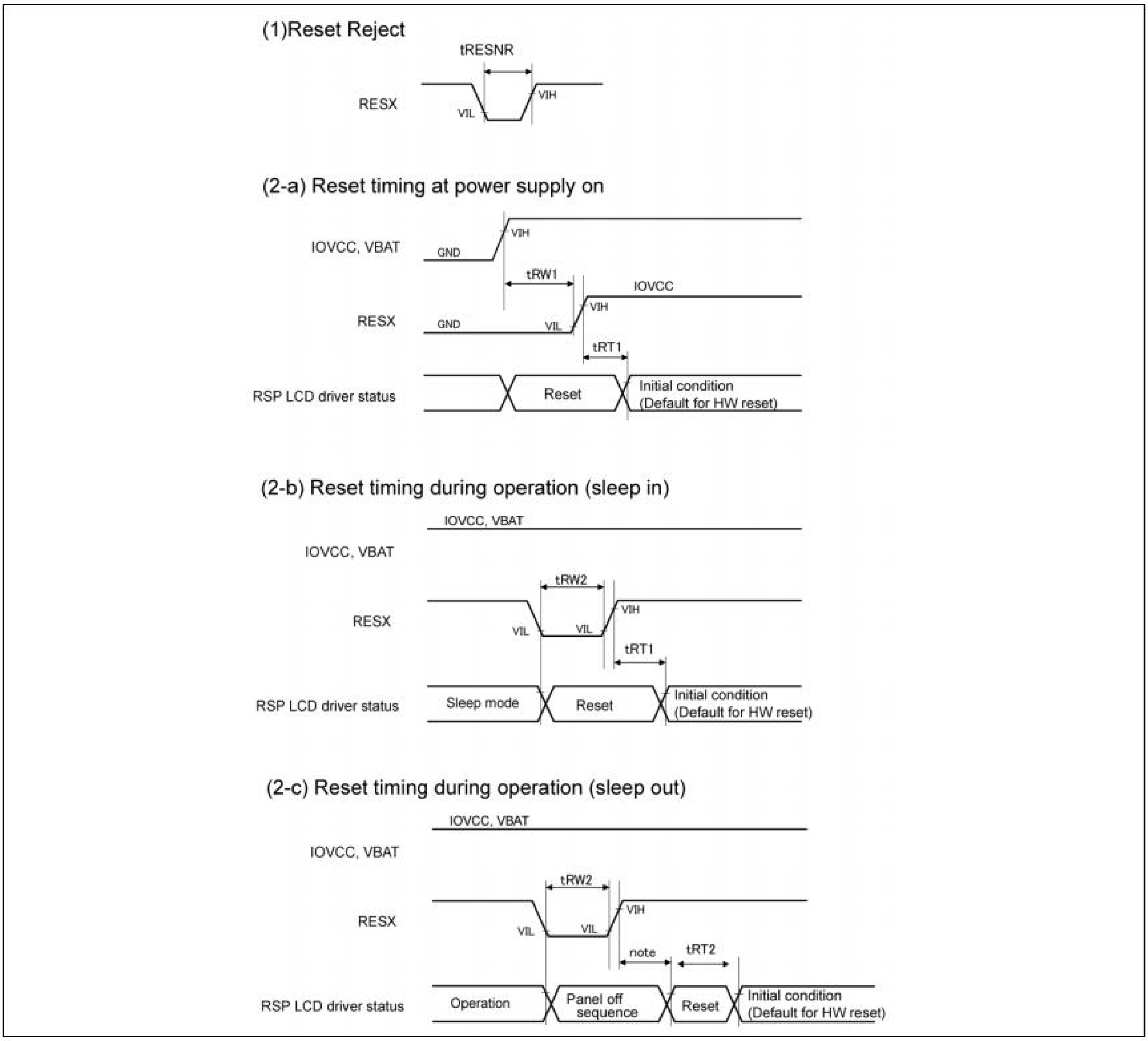


Figure 9 Reset Timing Characteristics (1)

(8) MIPI DSI Characteristics

Table 33

Item		Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
HS-RX	Differential input high threshold	VIDTH	mV	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	-	-	70	
	Differential input low threshold	VIDTL	mV	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	-70	-	-	
	Single-ended input low voltage	VILHS	mV	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	-40	-	-	
	Single-ended input high voltage	VIHHS	mV	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	-	-	460	
	Common-mode voltage HS receive mode	VCMRX(DC)	mV	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	70	-	330	1
	Differential input impedance	ZID	Ω	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	-	100	-	2
LP-RX	Logic 0 input voltage not in ULP State	VIL	mV	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	-50	-	550	
	Logic 1 input voltage	VIH	mV	IOVCC=1.65V~ 1.95V	880	-	1350	
	I/O leakage current	ILEAK	μA	Vin = -50mV - 1350mV	-10	-	10	
LP-TX	Thevenin output low level	VOL	mV	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	-50	-	50	
	Thevenin output high level	VOH	V	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	1.1	1.2	1.3	
	Output impedance of LP transmitter	ZOLP	Ω	IOVCC=DPHYVCC= 1.80V	110	-	-	2
CD-RX	Logic 0 contention threshold	VILCD	mV	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	-	-	200	
	Logic 1 contention threshold	VIHCD	mV	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	450	-	-	

Notes: 1. VCMRX (DC) = (VP+VDN)/2
2. Excluding COG resistance (contact resistance and ITO wiring resistance).

MIPI DSI HS-RX Clock and Data-Clock Specifications

Table 34

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
DSICLK Frequency	fDSICLK	MHz	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	100	-	500	4
DSICLK Cycle time	tCLKP	ns	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	1	-	10	
DSI Data Transfer Rate	tDSIR	Mbps	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	200	-	1000	4
Data to Clock Setup Time	tSETUP	UI	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1,95V	0.15	-	-	6
		ns	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	0.15	-	-	5,6
Clock to Data Hold Time	tHOLD	UI	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	0.15	-	-	6
		ns	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	0.15	-	-	5,6

Notes: 4. When fDSICLK<125MHz, change auto load NV setting so that it is compliant with THS-PREPARE+THS-ZERO spec.
5. Minimum tSETUP/tHOLD Time is 0.15UI. This value may change according to DSI transfer rate.
6. tSETUP/tHOLD Time is measured without HS-TX Jitter.

MIPI DSI LP-RX/TX Clock and Data-Clock Specifications

Table 35

Item	Symbol	Unit	Test condition	Min	Typ	Max	Notes
Time to drive LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$		IOVCC=DPHYVCC =1.65 ~ 1.95V	40 ns + 4*UI	-	85ns + 6*UI	
$T_{HS-PREPARE}$ + Time to drive HS-0 before the Sync sequence	$T_{HS-PREPARE}$ + $T_{HS-ZERO}$		IOVCC=DPHYVCC =1.65 ~ 1.95V	145ns + 10*UI	-	-	
Time to drive flipped differential state after last payload data bit of a HS transmission burst	$T_{HS-TRAIL}$		IOVCC=DPHYVCC =1.65 ~ 1.95V	max (n*8*UI, 60 ns + n*4*UI)	-	-	1,2
Time to drive LP-11after HS burst	$T_{HS-EXIT}$	ns	IOVCC=DPHYVCC =1.65 ~ 1.95V	100	-	-	
Time to drive LP-00 after Turnaround Request	T_{TA-GO}		IOVCC=DPHYVCC =1.65 ~ 1.95V	4*T_{LPTX}			
Time-out before new TX side starts driving	$T_{TA-SURE}$		IOVCC=DPHYVCC =1.65 ~ 1.95V	1*T_{LPTX}	-	2*T_{LPTX}	
Time to drive LP-00 by new TX	T_{TA-GET}		IOVCC=DPHYVCC =1.65 ~ 1.95V	5*T_{LPTX}			
Length of any Low-Power state period	T_{LPX}	ns	IOVCC=DPHYVCC =1.65 ~ 1.95V	50	-	-	
Ratio of $T_{LPX(MASTER)}$/$T_{LPX(SLAVE)}$ between Master and Slave side	Ratio T_{LPX}		IOVCC=DPHYVCC =1.65 ~ 1.95V	2/3	-	3/2	
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLK-POST}$		IOVCC=DPHYVCC =1.65 ~ 1.95V	60 ns + 52UI	-	-	3
$T_{CLK-PREPARE}$ +time for lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE}$ +$T_{CLK-ZERO}$	ns	IOVCC=DPHYVCC =1.65 ~ 1.95V	300	-	-	
Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	$T_{CLK-PRE}$	UI	IOVCC=DPHYVCC =1.65 ~ 1.95V	8	-	-	
Time to drive LP-00 to prepare for HS clock transmission	$T_{CLK-PREPARE}$	ns	IOVCC=DPHYVCC =1.65 ~ 1.95V	38	-	95	
Time to drive HS differential state after last payload clock bit of an HS transmission burst	$T_{CLK-TRAIL}$	ns	IOVCC=DPHYVCC =1.65 ~ 1.95V	60	-	-	
Time from start of THS-TRAIL period to start of LP-11 state	T_{EOT}		IOVCC=DPHYVCC =1.65 ~ 1.95V	-	-	105 ns + n*12*UI	2
Length of Low-Power TX period in case of using DSI clock	T_{LPTX1}	UI	IOVCC=DPHYVCC =1.65 ~ 1.95V	-	32	-	4
Length of Low-Power TX period in case of using internal OSC clock	T_{LPTX2}	ns	IOVCC=DPHYVCC =1.65 ~ 1.95V	-	1/(fosc/4)	-	

Notes:
1. If a > b then max(a, b) = a, otherwise max(a, b) = b
2. Where n = 1 for Forward-direction HS mode.
3. The R63419 can work with this specification although the end part of internal process is remained when Clock Lane enter LP-11 and the R63419 can work without the remained process if tCLK-POST is more than 512 UI.
4. The R63419 uses DSI clock from the Host processor if Clock Lane is active, and internal oscillator clock if Clock Lane is disabled.

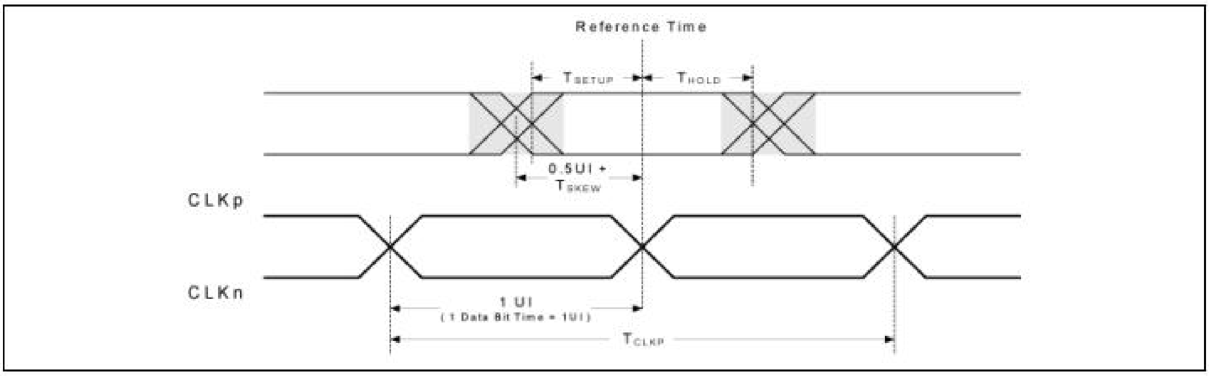


Figure 12 Data to Clock Timing Definitions

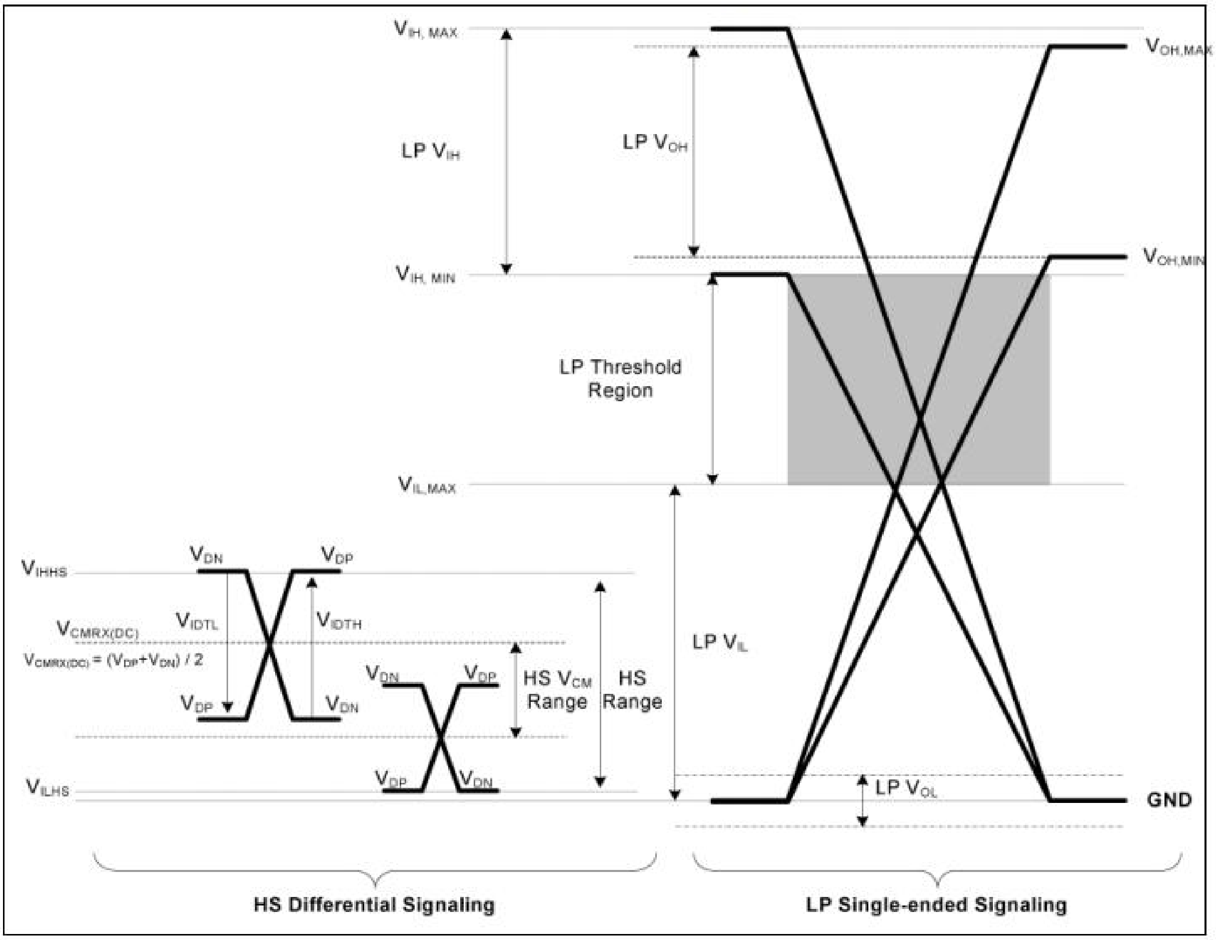


Figure 13 DSI LP Mode

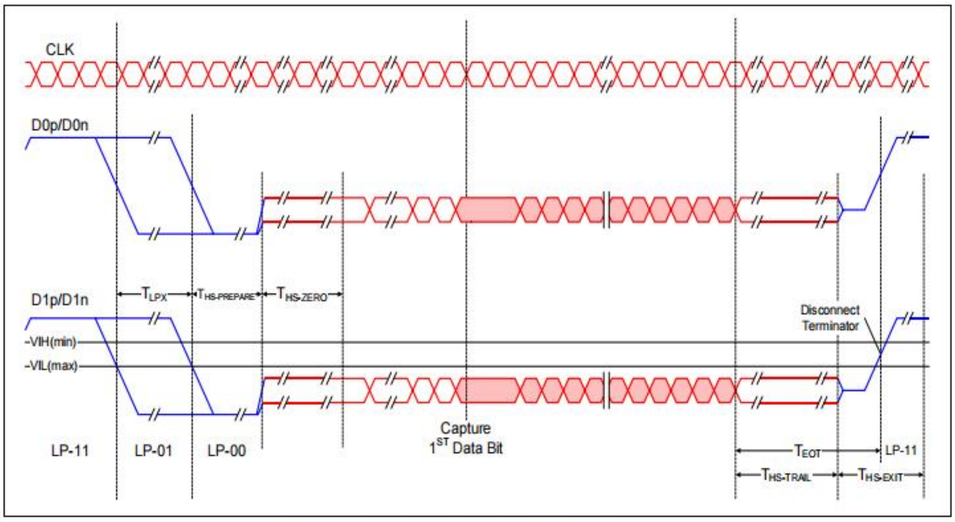


Figure 14 HS Data Transmission in Bursts

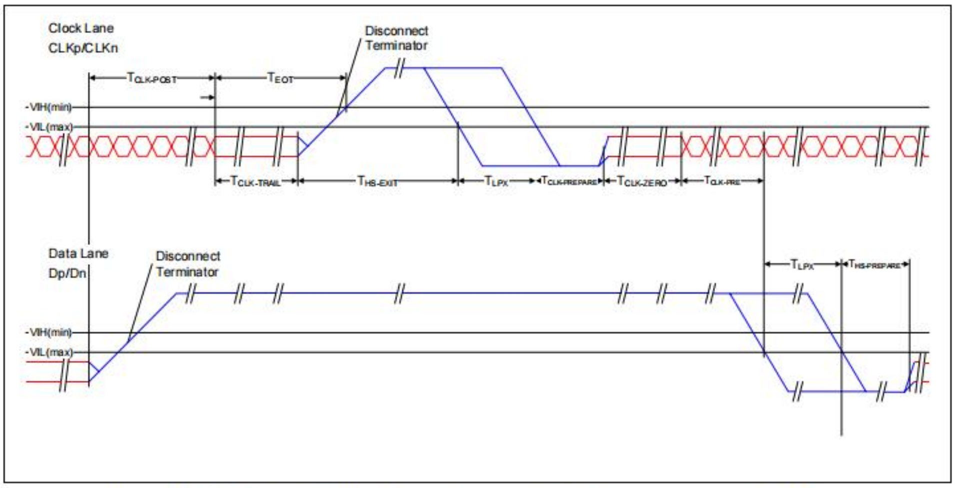


Figure 15 Switching the Clock Lane between Clock Transmission and LP Mode

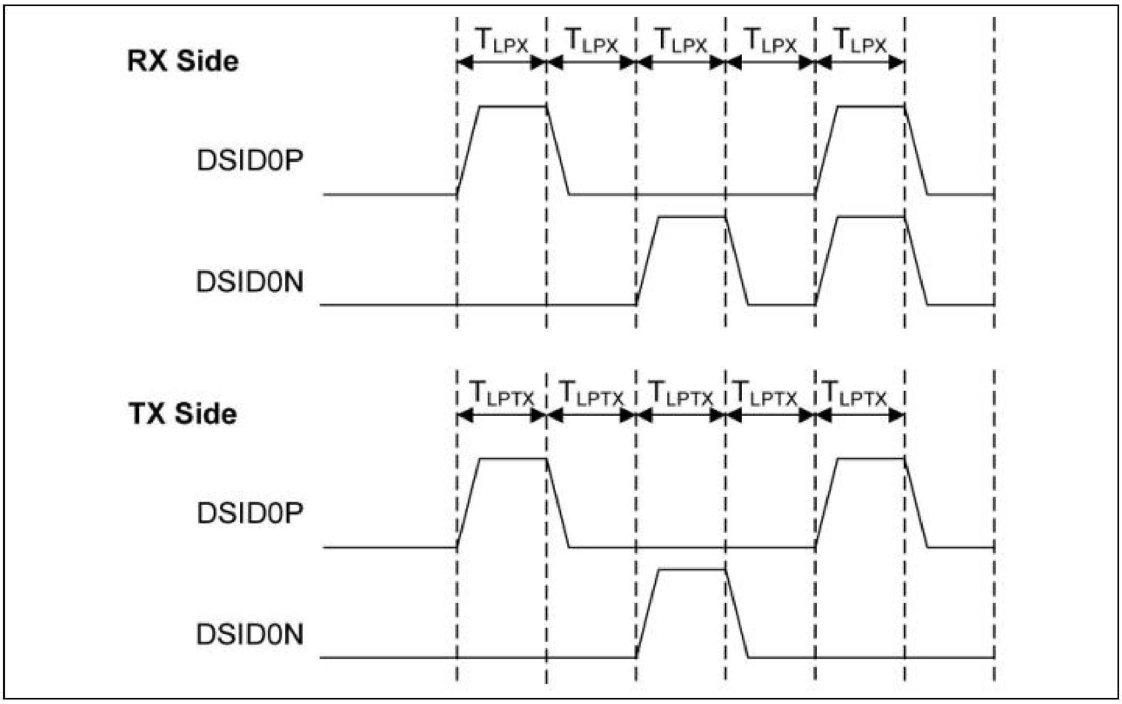


Figure 16 DSI LP Mode

1) Display Timing (Video Mode)

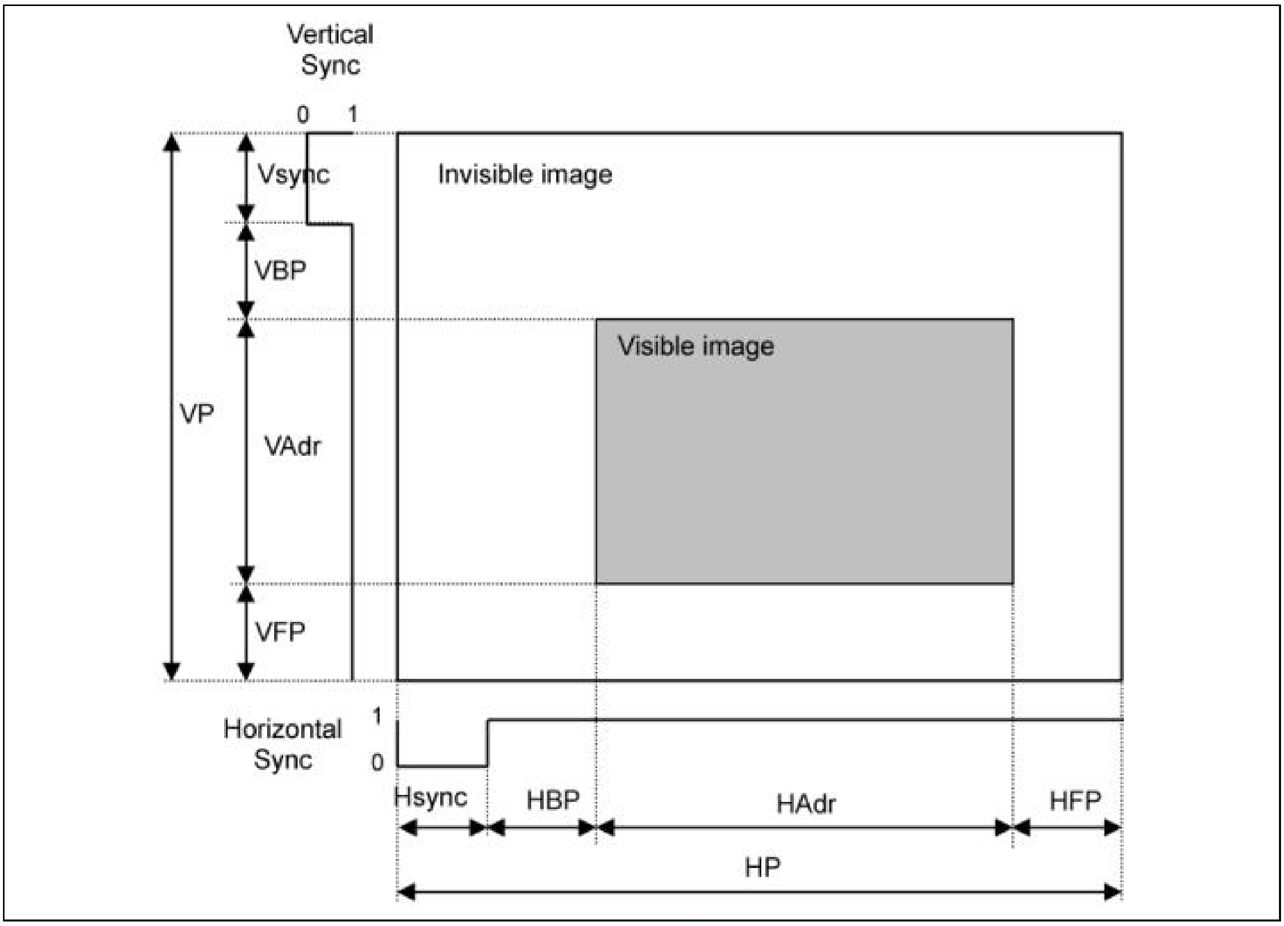
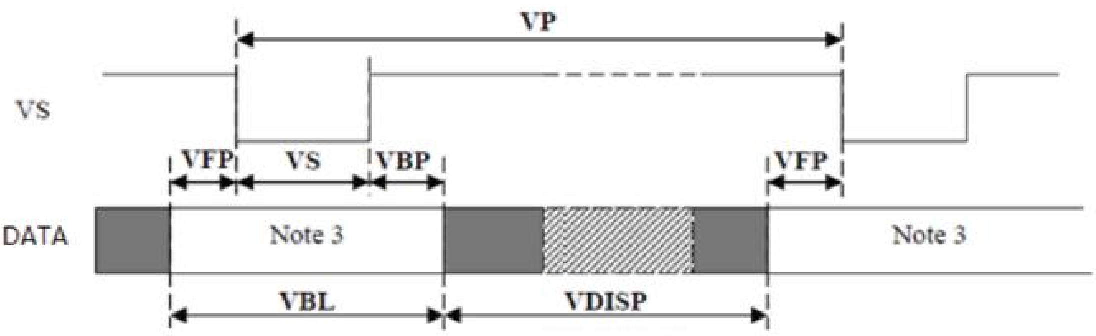


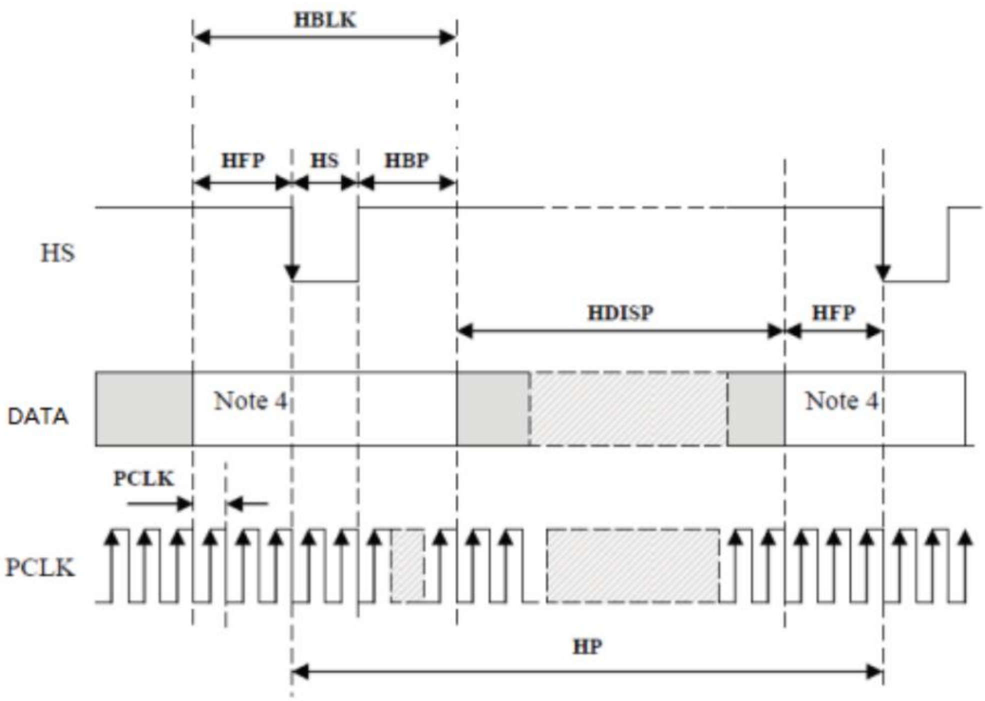
Figure 30

Vertical Timing



Item	Symbol	Conditions	Min	Recommend	Max	Unit
Vertical cycle	VP		-	2568	-	Line
Vertical low pulse width	VS		1	2	-	Line
Vertical front porch	VFP		2	4	-	Line
Vertical back porch	VBP		2	2	-	Line
Vertical data start point		VS+VBP	4	4	-	Line
Vertical blanking period	VBL	VFP+VS+VBP	6	8	-	Line
Vertical active area		VDISP	-	2560	-	Line
Vertical Refresh Rate	VRR		57	60	63	Hz

Horizontal Timing



Item	Symbol	Conditions	Min	Recommend	Max	Unit
HS cycle	HP		-	1688	-	PCLK
HS low Pulse width	HS		-	20	-	PCLK
Horizontal back porch	HBP		-	80	-	PCLK
Horizontal front porch	HFP		-	148	-	PCLK
Horizontal data start point		HS+HBP	-	100	-	PCLK
Horizontal blanking period	HBLK	HFP+HS+HBP	-	248	-	PCLK
orizontal active area	HDISP		-	1440	-	PCLK
1 Horizontal timing			6.472	6.472	-	us
Pixel clock frequency	PCLK		-	3.8	-	ns
			-	260.8	-	MHz
MIPI Speed(4 lane)*2ports	-	-	780	-	1000	Mbps/lane

8. Initial Sequence

(8-1) LCD Power On Sequence

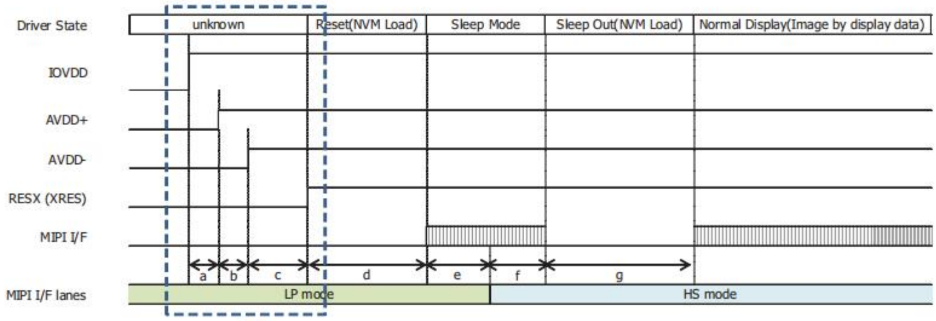
I/F: MIPI 4lane*2ports

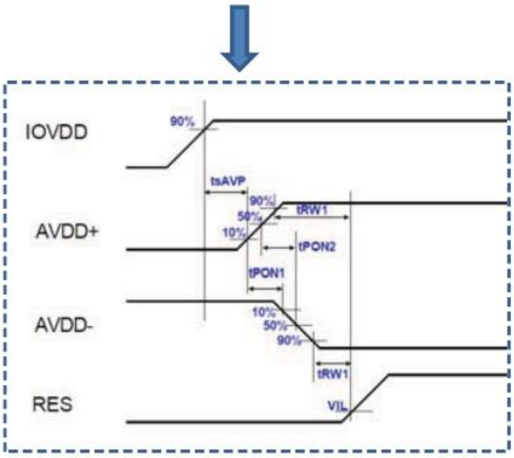
Panel Size : WQHD (1440xRGBx2560)

VSP=5.9,VSN-=-5.9V, VDDIO=1.8V

Color Mode:24bit

Frame frequency:60Hz





Item	Symbol	min
AVDD+ to AVDD- delay time (10% to 10%)	tPON1	0ms
AVDD+ to AVDD- delay time (50% to 50%)	tPON2	0ms
System power on to AVDD+ ON time	tsAVP	1ms
Reset low-level width	tRW1	1ms

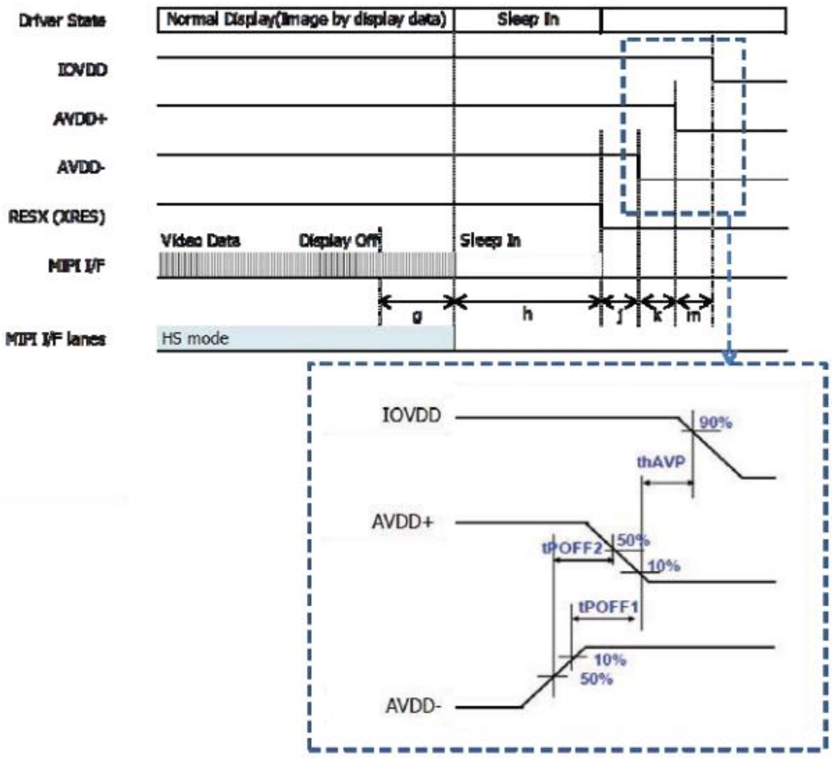
	State	Action/Command	DSI Data Type		Adress	Para.	Data	Note
1		RESX = L						
2		Power Supply IOVDD ON (Typ1.8V)						
3		- Wait Min. 200ms						Wait to IOVDD=90% (depends on Power Supply Circuit)
4		Power Supply AVDD+ ON (Typ5.9V)						
5		- Wait 20ms						Wait for VSP->VSN ordering (depends on Power Supply Circuit)
6		Power Supply AVDD- ON (Typ-5.9V)						
7		- Wait 20 ms						
8		RESX = L						
9		- Wait Min. 10ms						Wait to VSP/VSN=±90% and RESX=Low period (depends on Power Supply Circuit)
10		RESX = H						
11		- Wait MIN 10ms						
12	NVM Auto Load							
13	Sleep Mode On							
14		Manufacture Command Access Protect	Generic	29h	B0h	P1	04h	Unlock manufacturing command write (CE etc.)
15		NVM Load setting	Generic	29h	D6h	P1	01h	The command to remove NVM reload after sleep out
16		Set Mipi display mode	Generic	29h	B3h	P1	08h	Set Mipi display mode 0x08(command mode enable) 0x18(video RAM bypass mode enable)
17	(note1)	set column address	DCS	39h	2Ah	P1	00h	0x00/00h : Start Column Address = 0
						P2	00h	
						P3	05h	0x05/9Fh : End Column Address = 1439
						P4	9Fh	
18		If customer need, please add initial command in here						
19		Manufacture Command Access Protect	Generic	29h	B0h	P1	03h	Lock manufacturing command write
20	(note2)	**DSI signal transfer Start**						
21		Exit_sleep_mode	DCS	39h	11h	-	-	
22	Sleep Mode exit	- Wait 200ms						After Wait Min. 6 frame, automaticaly sleep mode off.
23		Write_Display_Brightness	DCS	39h	51h	P1	FFh	0xFFh : LED 100% Duty
24		Write_CTRL_Display	DCS	39h	53h	P1	0Ch	0x0Ch : LED ON(BL=1h), Dimming ON(DD=2h)
25	Display on	Set_display_on	DCS	39h	29h	-	-	
26		Send Picture image						Image write

NOTE1: STEP17 can be deleted if video mode is used.

NOTE2: The above Sequence applies on the premise of MIPI command mode.

If MIPI Video has been used, please set step20.

(8-2)LCD Power Off sequence



Item	Symbol	Min
AVDD- to AVDD+ delay time (10% to 10%)	tPOFF1	0ms
AVDD- to AVDD+ delay time (50% to 50%)	tPOFF2	0ms
AVDD+ off to system power off time	thAVP	0ms

Step	State	Action/Command	DSI Data Type		Adress	Para.	Data	Note
1	Backlight OFF	Backlight OFF	DCS	39h	53h	P1	00h	LED OFF
2	Display OFF	set_display_off	DCS	39h	28h	-	-	
3		- Wait Min. 20ms						
4		enter_sleep_mode	DCS	39h	10h	-	-	
5	Sleep Mode On	- Wait Min. 120ms						
6	note 3	**DSI signal transfer stop**						
7		RESX=L						
8		- Wait 10ms						
9		Power Supply AVDD- OFF (GND=0V)						
10		- Wait 20ms						Wait for VSN->VSP ordering (depends on Power Supply Circuit)
11		Power Supply AVDD+ OFF (GND=0V)						
12		- Wait 20ms						Wait to VSP=10%, VSN=10% (depends on Power Supply Circuit)
13		Power Supply IOVDD OFF (GND=0V)						
14	Power OFF	- Wait 20ms						Wait to IOVDD OFF stable

NOTE3：STEP6 can be deleted if command mode is used.

(8-3)Deep standby IN Sequence

Table 18

Step	State	Action/Command	DSI Data Type		Adress	Para.	Data	Note
1	Backlight OFF	Backlight OFF	DCS	39h	53h	P1	00h	LED OFF
2	Display OFF	set_display_off	DCS	39h	28h	-	-	
3		- Wait Min. 20ms						
4		enter_sleep_mode	DCS	39h	10h	-	-	
5	Sleep Mode On	- Wait Min. 120ms						
6	note4	**DSI signal transfer stop**						
7		Manufacture Command Access Protect	Generic	29h	B0h	P1	04h	Unlock manufacturing command write
8			Generic	29h	B1h	P1	01h	Low power mode
9		Power Supply AVDD- OFF (GND=0V)						
10		- Wait 20ms						
11		Power Supply AVDD+ OFF (GND=0V)						
12	Deeptandby mode IN	- Wait 20ms						

NOTE4：STEP6 can be deleted if command mode is used.

(8-4)Deep standby OUT Sequence

Table 19

	State	Action/Command	DSI Data Type		Adress	Para.	Data	Note
1		RESX = L						
2		Power Supply AVDD+ ON (Typ5.9V)						
3		- Wait 20ms						Wait for VSP->VSN ordering (depends on Power Supply Circuit)
4		Power Supply AVDD- ON (Typ-5.9V)						
5		- Wait 20 ms						
6		RESX = L						
7		- Wait Min. 10ms						Wait to VSP/VSN=±90% and RESX=Low period (depends on Power Supply Circuit)
8		RESX = H						
9		- Wait MIN 10ms						
10	NVM Auto Load							
11	Sleep Mode On							
12		Manufacture Command Access Protect	Generic	29h	B0h	P1	04h	Unlock manufacturing command write (CE etc.)
13		NVM Load setting	Generic	29h	D6h	P1	01h	The command to remove NVM reload after sleep out
14		Set Mipi display mode	Generic	29h	B3h	P1	08h	Set Mipi display mode 0x08(command mode enable) 0x18(video RAM bypass mode enable)
15	(note4)	set column address	DCS	39h	2Ah	P1	00h	0x00/00h : Start Column Address = 0
						P2	00h	
						P3	05h	0x05/9Fh : End Column Address = 1439
						P4	9Fh	
16		If customer need, please add initial command in here						
17		Manufacture Command Access Protect	Generic	29h	B0h	P1	03h	Lock manufacturing command write
18	(note5)	**DSI signal transfer Start**						
19		Exit_sleep_mode	DCS	39h	11h	-	-	
20	Sleep Mode exit	- Wait 200ms						After Wait Min. 6 frame, automaticaly sleep mode off.
21		Write_Display_Brightness	DCS	39h	51h	P1	FFh	0xFFh : LED 100% Duty
22		Write_CTRL_Display	DCS	39h	53h	P1	0Ch	0x0Ch : LED ON(BL=1h), Dimming ON(DD=2h)
23	Display on	Set_display_on	DCS	39h	29h	-	-	
24	Deepstandby mode out	Send Picture image						Image write

NOTE5: STEP15 can be deleted if video mode is used.

NOTE6: The above Sequence applies on the premise of MIPI command mode.

If MIPI Video has been used, please set step18.

(8-5)Touch Panel Power ON Sequence

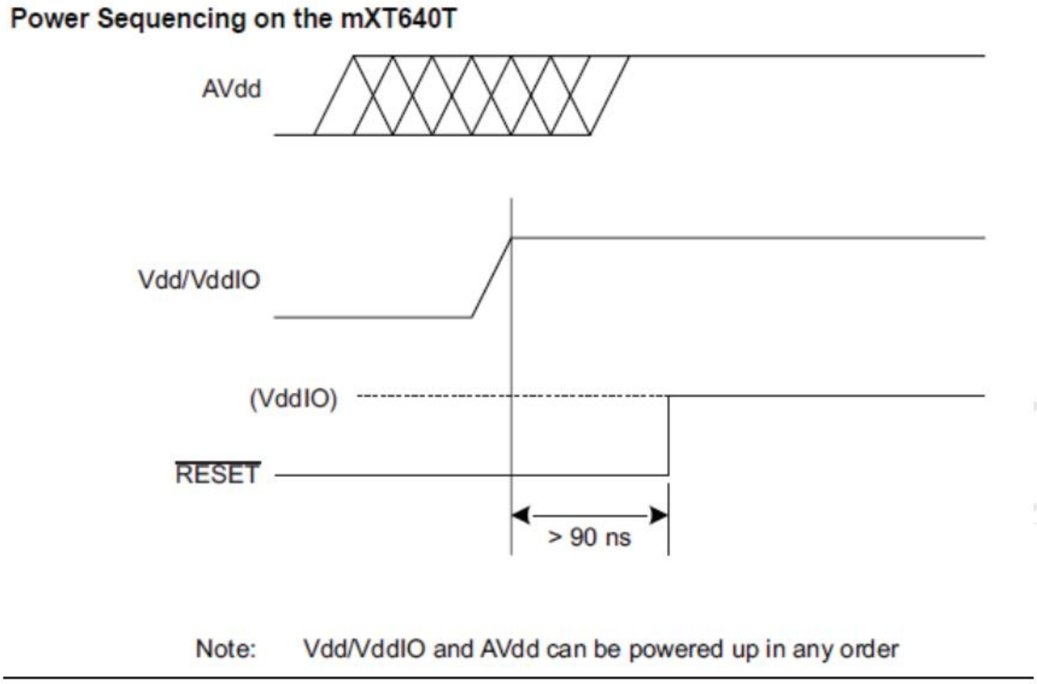


Fig .11

Touch Panel Power OFF Sequence
Power Off can be setted freely.

9. Electro-Optical Characteristics

Vddio=1.8V, VSP=5.9V, VSN=-5.9V, ILED=20mA/pcs, Ta = 25℃

Optical Characteristics							
Parameter	symbol	condition	MIN	TYP	MAX	unit	Remark
Brightness	Br	θ=0°	300	400	-	cd/m²	Note1,2
Contrast	Co	θ=0°	910	1300	-		Note1,3
Viewing Angle	θ11	Co > 10	80	-	-	deg	Note1
	θ12		80	-	-		
	θ21		80	-	-		
	θ22		80	-	-		
White chromaticity	x	θ=0°	0.27	0.30	0.33		Note.1,3
	y		0.29	0.32	0.35		
Uniformity	-	θ=0°	80	85	-	%	Note.5
NTSC ratio	-	θ=0°	-	90	-	%	Note.1,3
Response Time	(τr+td)	θ=0°	-	35	-	ms	Note1,6
Flicker ratio	-	θ=0°	-	-	10	%	Note.4

Note 1) Definition of range of visual angle

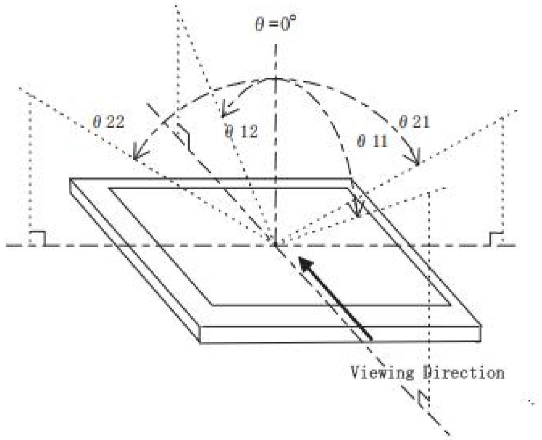


Fig .12 Definition of viewing angle

Note 2) Brightness is measured as shown in Fig.13, and is defined as the brightness of all pixels "White" at the center of display area on optimum contrast.

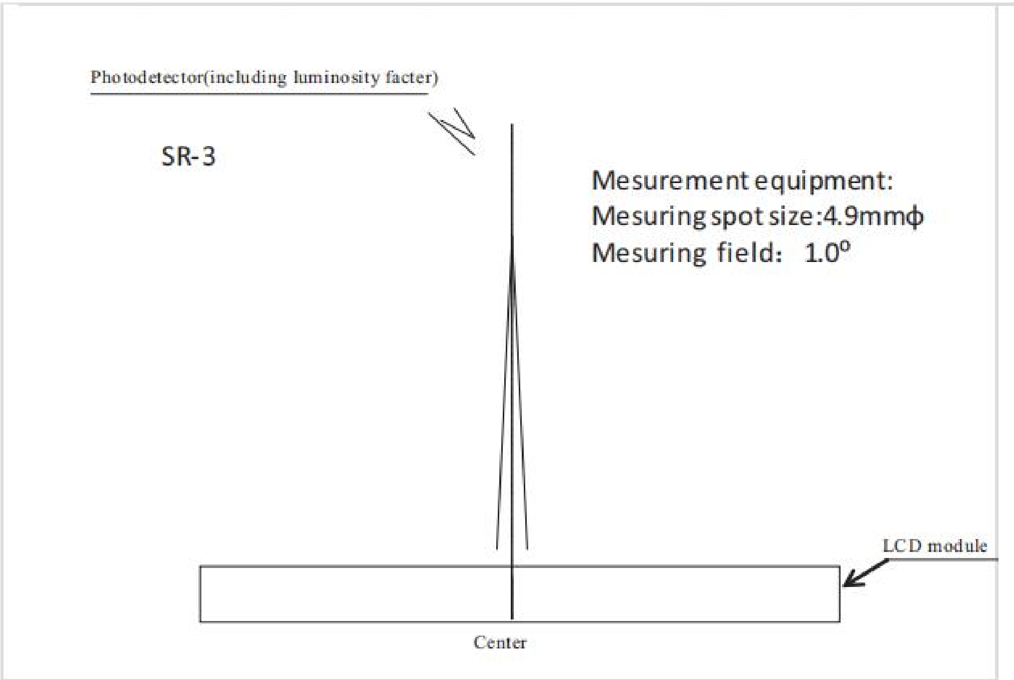


Fig. 13 Optical characteristics Test Method (Brightness)

Note 3) Contrast ratio is defined as follows:

$$Co=\frac{\text{Luminance(brightness) all pixcels "White"}}{\text{Luminance(brightness) all pixcels "Black"}}$$

Note 4) Measuring systems: YOKOGAWA 3298_01 + 3298_11

- Temperature = 25℃(±3℃), Frame Frequency = 53Hz~62Hz, LED back-light: ON, Environment brightness < 300 lx
- Measured sample : New sample before a long term aging.
- Flicker ratio is very sensitive to measuring condition.
- Measuring pattern Please refer to figure below.

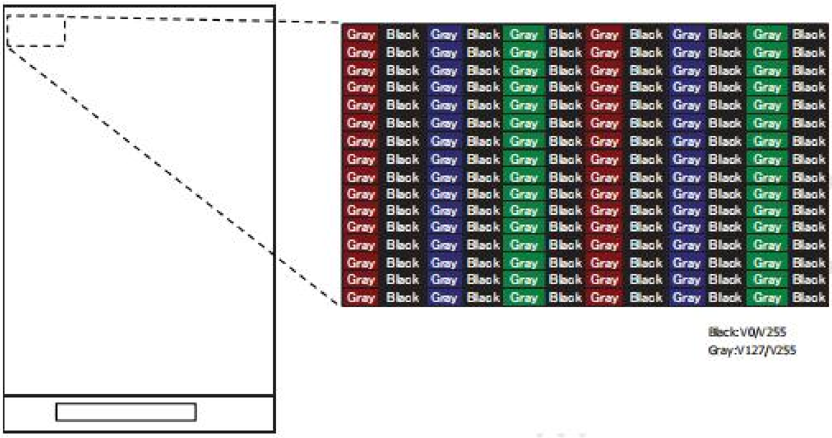


Fig. 14 Flicker Measuring pattern

Note 5) Uniformity is defined as follows:

$$\text{Uniformity} = \frac{\text{Minimum Luminance(brightness) in 9 points}}{\text{Maximum Luminance(brightness) in 9 points}}$$

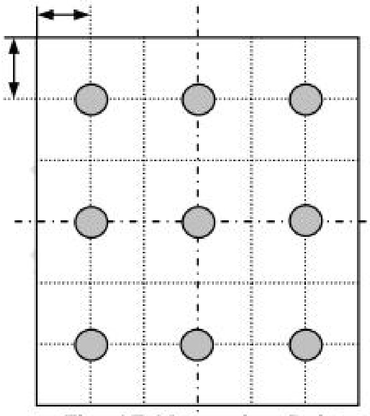


Fig. 15 Measuring Point

Note 6) Response time is defined as follows:

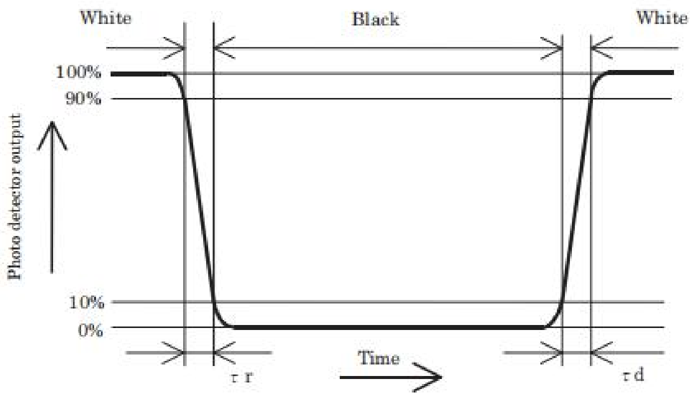


Fig.16 Response time

10.Reliability

No.	Test	Condition	Judgment criteria
1	Temperature Cycling	-30℃ → 70℃ → -30℃ ... 30min (3min) 30min (3min)30min 10cycle	Per table in below
2	High Temp. Storage	Ta=70℃ 240h	Per table in below
3	Low Temp. Storage	Ta=-30℃ 240h	Per table in below
4	Humidity Operation	Ta=40℃ 90%RH 240h	Per table in below (polarizer discoloration is excluded)
5	High Temp. Operation	Ta=60℃ 240h	Per table in below
6	Low Temp. Operation	Ta=-20℃ 240h	Per table in below
7	ESD	Discharge resistance: 0 Ω Discharge capacitor: 200 pF Discharge voltage: ±200 V Max Discharge 1 time to each input line ※ "GND" of display module is connected GND of test system ground.	Per table in below

※Reliability test result is guaranteed at the conditions of a module attached with CG and OCA(~~ZY404~~ CBS-HC01).

(OCA recommended by Sharp: ~~ZY404~~ CBS-HC01 made in Hitachi Chemical.)

If CG laminating process is applied in customer factory, please confirm the reliability and CG laminating process is no problem before mass production began using the OCA and CG.

If problem happened at mass production, Sharp will not to follow.

Because Sharp cannot guarantee the customer 's CG laminating process.

INSPECTION	CRITERION(after test)
Appearance	No Crack on the FPC, on the LCD Panel
Alignment of LCD Panel	No Bubbles in the LCD Panel No other Defects of Alignment in Active area
Electrical current	Within device specifications
Function / Display	No Broken Circuit, No Short Circuit or No Black line No Other Defects of Display

11.Records Of Version

Version	Revise Date	Page	Content
00		ALL	New released