PRODUCT SPECIFICATION FOR LCD MODULE

Revision: 1.0

Model No: LS070I18-MP-V1

Module Type: COG+FPC+B/L

APPROVED SIGNATURE

■ Approved Product Specification only

□ Approved Product Specification and Samples

Prepared By	Checked By	Approved By

Record of Revisions

Rev	Date	Sub-Model	Description of change
V01			

Table of contents

1. General description

1.1 Introduction

Low-Key SeiKo model is a color active matrix thin film transistor (TFT) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. This model is composed of a TFT LCD panel, a driving circuit and a back light system. This TFT LCD has a 7.0 inch diagonally measured active display area with WXGA (800 horizontal by 1280 vertical pixel) resolution.

1.2 Features

7.0 inch configuration

4wire mipi interface

LED Backlight

RoHS Compliance

1.3 Applications

Mobile

Personal Navigation Device

Multimedia applications and Others AV system

1.4 General information

Item		Specification	Unit
Outline Dimension		103.66x162.60x2.90(Typ.)	mm
Display area		94.2(H) x 150.72(V)	mm
Number of Pixel		800 RGB(H) x 1280 (V)	pixels
Pixel pitch		0.03925(H) × 0.11775(V)	mm
Pixel arrangement		RGB Vertical stripe	
Display mode		IPS, Normally Black	
Surface treatment		Antiglare, Hard-Coating(3H)	
IC		GH8555BL	
Back-light		Single LED (Side-Light type)	
Power Consumption	B/L System	NA(Max.)	w

1.5 Mechanical Information

item		Min.	Typ.	Max.	Unit
Module Size	Horizontal(H)	103.46	103.66	103.86	mm
	Vertical(V)	162.40	162.60	162.80	mm
	Depth(D)	2.75	2.90	3.01	mm

2.0 ABSOLUTE MAXIMUM RATINGS

2.1 Electrical Absolute Rating

2.1.1 TFT LCD Module

Item	Symbol	Min.	Max.	Unit.	Note
Power supply voltage	VCI	-0.3	3.6	V	GND=0
Logic Signal Input Level	VCC	-0.3	VCI+0.3	V	

2.1.2 Back-Light Unit

Item	Symbol	MIN.	TYP.	Max.	Unit	Note
Current of Backlight Unit	Ib	--	80	--	mA	
Voltage of Backlight Unit	Vb	--	16	17.5	V	

Note:

Permanent damage to the device may occur if maximum values are exceeded or reverse voltage is loaded.

2.2 Environment Absolute Rating

Item	**Symbol**	**Min.**	**Max.**	**Unit**	**Remarks**
Operating Temperature	**Topa**	**-20**	**+70**	℃	
Storage Temperature	**Tstg**	**-30**	**+80**	℃	

3.0 OPTICAL CHARACTERISTICS

3.1 Optical specification:

Item	Symbol	Temp.	Min.	Typ.	Max.	Unit	Condition
Response Time	Tr+Tf	25℃		30	35	msec	θ =0 °,φ=0 ° (Note 1,3)
Contrast Rate	Cr	25℃	700	850	--	--	θ =0 °, φ=0 ° LED:ON, LIGHT:OFF(Note1,2)
Brightness	YL	25℃	400	450		Cd/m2	(IL=80mA)(Note1,4)
Visual angle range front and rear	θ	25℃	(θ_L) 85 (θ_R) 85			De-gree	ϕ = 0°, CR≧10 LED:ON LIGHT:OFF(Note 1,4)
Visual angle range left and right	θ	25℃	(θ_U) 85 (θ_D) 85			De-gree	ϕ =90°, CR≧10 LED:ON LIGHT:OFF(Note 1,4)
Brightness uniformity	BUNI		80			%	Θ =0(Note5,7)
Visual angle			all				(Note 6)

Item	Symbol	Transmissive			Conditions
		Min.	Typ.	Max.	
Red	XR				Reference: LCD Panel, CIE (x, y) chromaticity (Note 1,4)
	YR				
Green	XG				
	YG				
Blue	XB				
	YB				
White	XW	0.27	0.31	0.35	
	YW	0.29	0.32	0.36	

3.2 Measuring Condition

Measuring surrounding: dark room ,LED current IL : 80mA

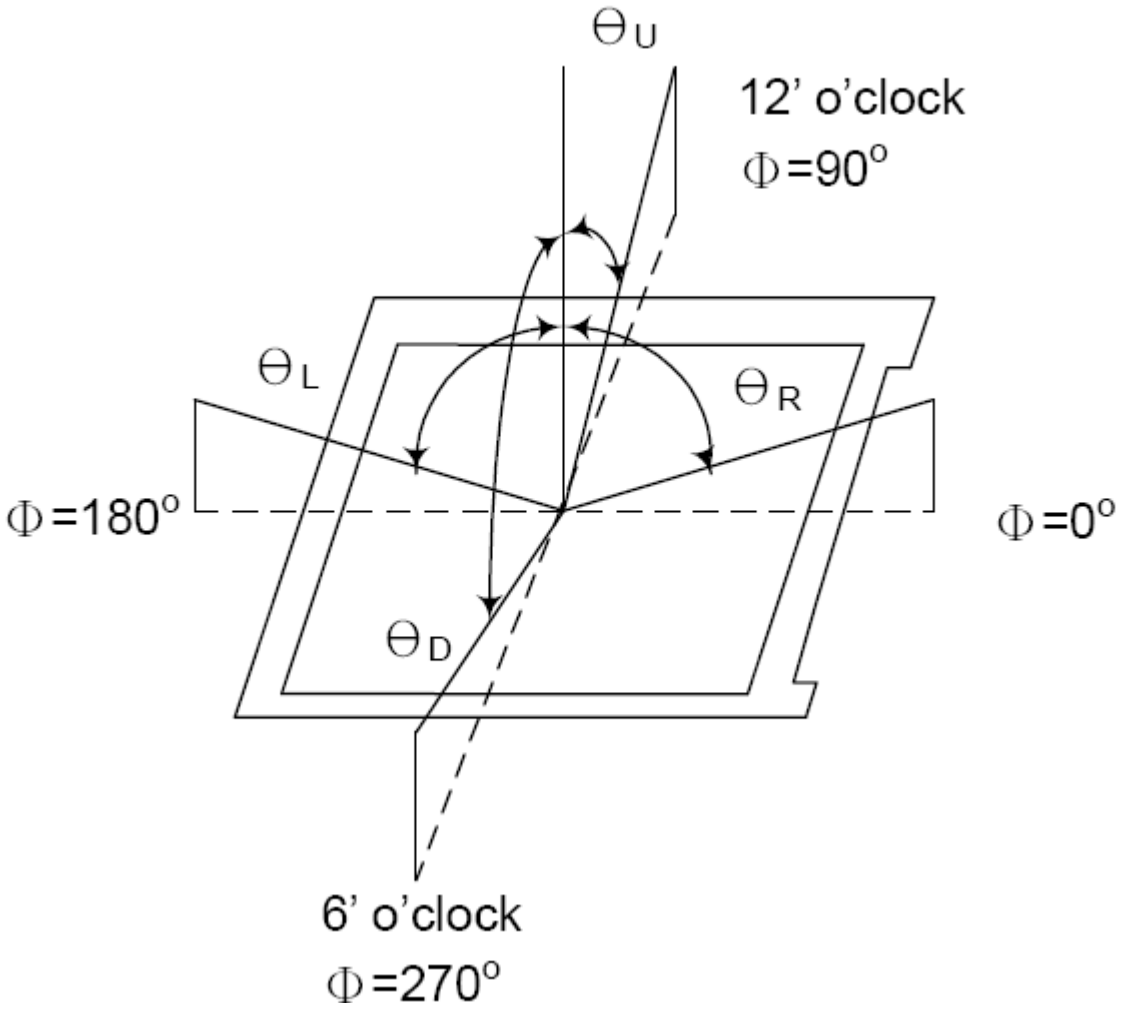
Ambient temperature: 25±2°C

15min. warm-up time.

3.3 Measuring Equipment

FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics. Measuring spot size: 20 ~ 21 mm

Note (1) Definition of Viewing Angle :

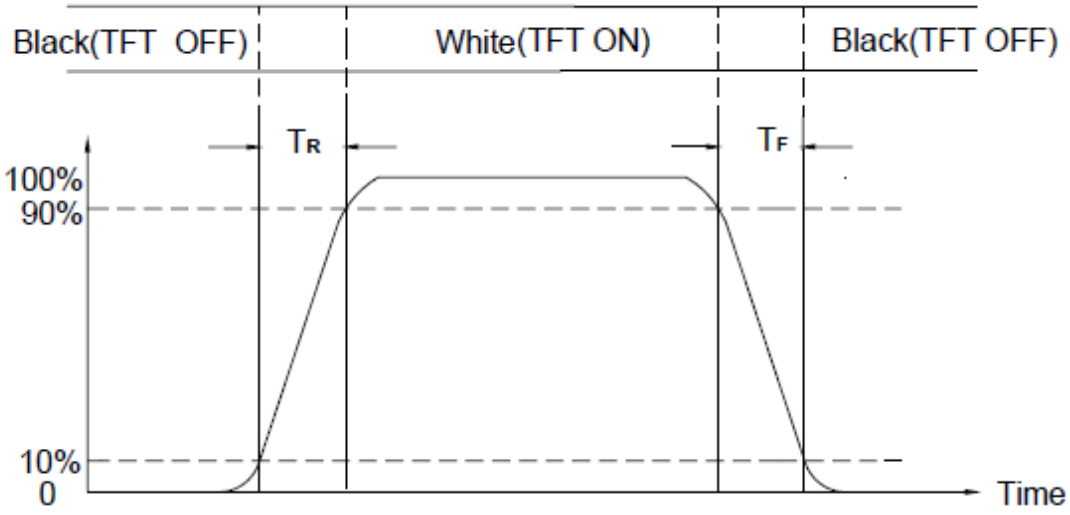


Note (2) Definition of Contrast Ratio (CR):

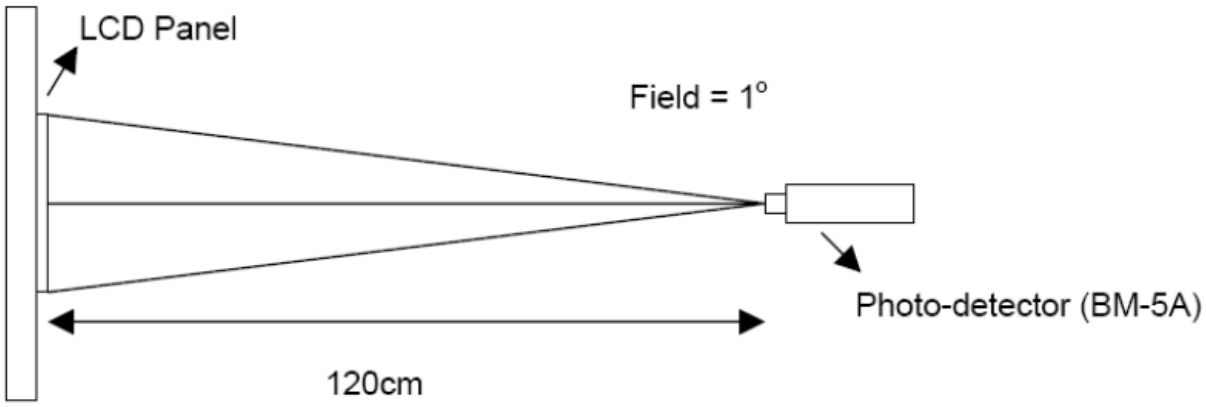
Measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

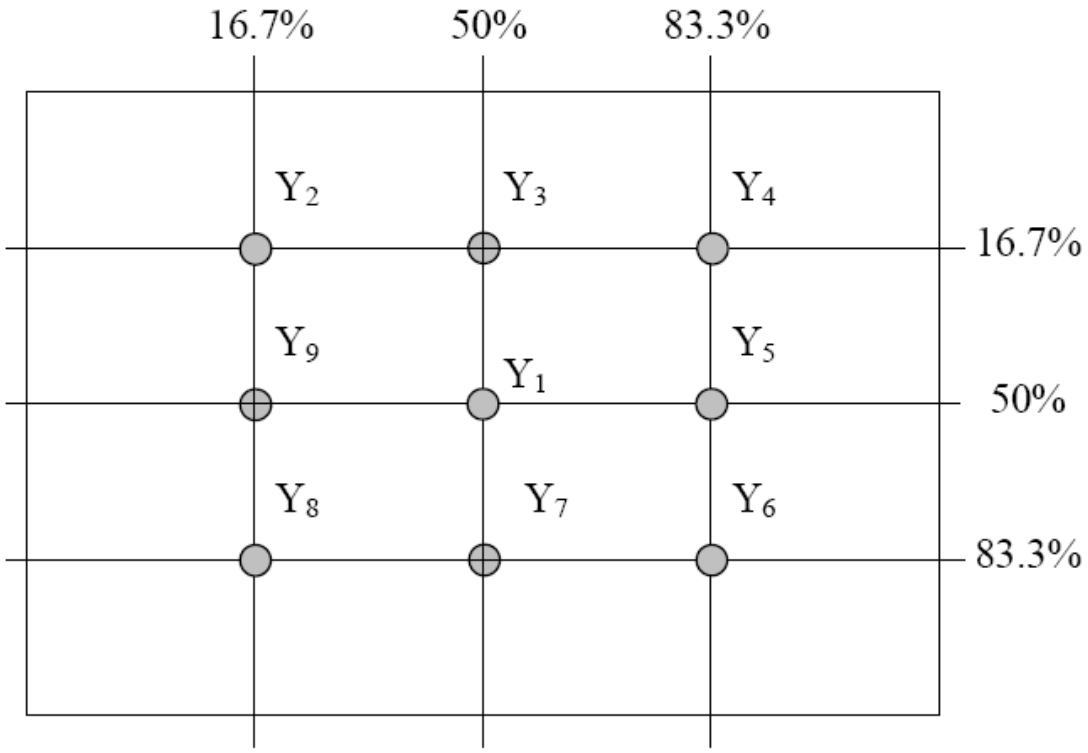
Note (3) Definition of Response Time: Sum of TR and TF



Note (4) Definition of optical measurement setup



Note (5) Definition of brightness uniformity



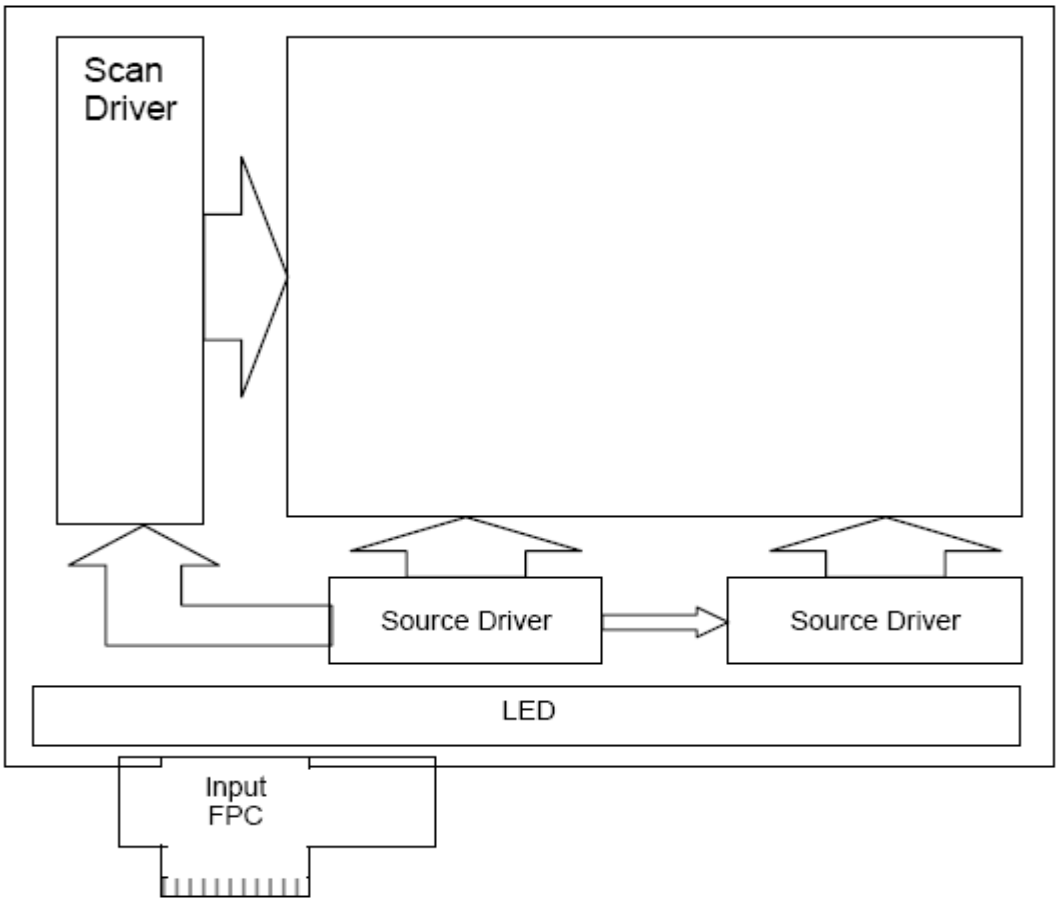
$$\text{Luminance uniformity} = \frac{\text{(Min Luminance of 9 points)}}{\text{(Max Luminance of 9 points)}} \times 100\%$$

Note (6) Rubbing Direction (The different Rubbing Direction will cause the different optimal view direction).

Note (7) Measured at the brightness of the panel when all terminals of LCD panel are electrically open.

4.0 BLOCK DIAGRAM

4.1 TFT LCD Module



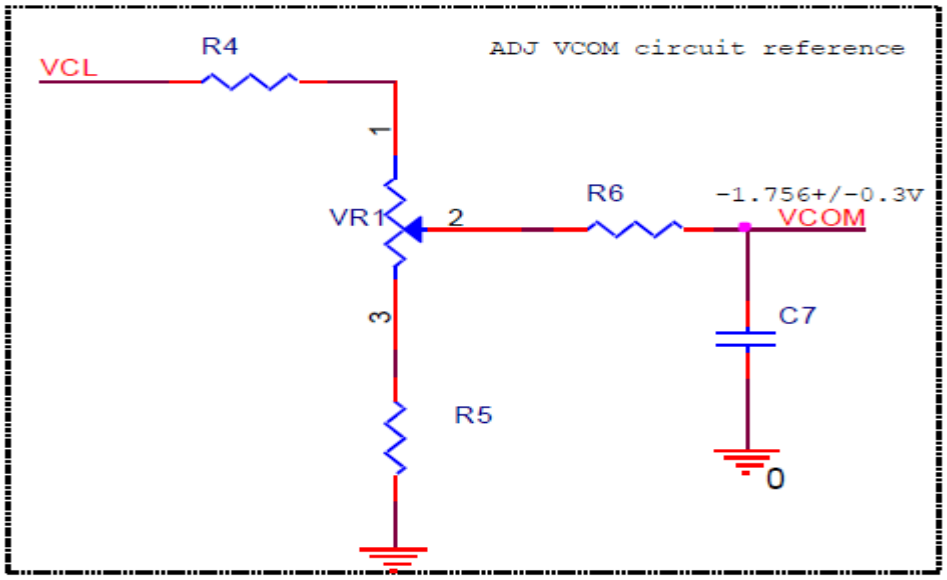
5.0 INTERFACE PIN CONNECTION

5.1 TFT LCD ModuleCN (Input signal): FPC Down Connector, (FH33J-40S-0.5H (10) (HIROSE), 40pin,pitch = 0.5mm)

Terminal No.	Symbol	I/O	Functions
1	VCOM	P	Common Voltage(-1.756+/-0.3V)
2	VDDIN	P	Power input 3.3 Voltage
3	VDDIN	P	Power input 3.3 Voltage
4	GND	P	Power Ground
5	RST	I	Globel reset signal,low active
6	NC	-	No connection
7	GND	P	Power Ground
8	MIPI_0N	I	MIPI DSI differential data pair
9	MIPI_0P	I	MIPI DSI differential data pair
10	GND	P	Power Ground
11	MIPI_1N	I	MIPI DSI differential data pair
12	MIPI_1P	I	MIPI DSI differential data pair
13	GND	P	Power Ground
14	MIPI_CKN	I	MIPI DSI differential CLK pair
15	MIPI_CKP	I	MIPI DSI differential CLK pair
16	GND	P	Power Ground
17	MIPI_2N	I	MIPI DSI differential data pair
18	MIPI_2P	I	MIPI DSI differential data pair
19	GND	P	Power Ground
20	MIPI_3N	I	MIPI DSI differential data pair
21	MIPI_3P	I	MIPI DSI differential data pair
22	GND	P	Power Ground
23	NC	-	No connection
24	NC	-	No connection
25	GND	P	Power Ground
26	NC	-	No connection
27	PWMO	O	PWM control signal for BL driver
28	NC	-	No connection
29	VCL	O	Output voltage pin
30	GND	P	Power Ground
31	LED-	P	Power for LED backlight negative
32	LED-	P	Power for LED backlight negative

33	**NC**	**-**	**No connection**
34	**NC**	**-**	**No connection**
35	**AVEE**	**p**	**Analog supply negative voltage**
36	**NC**	**-**	**No connection**
37	**NC**	**-**	**No connection**
38	**AVDD**	**P**	**Analog supply positive voltage**
39	**VLED+**	**P**	**Power for LED backlight anode**
40	**VLED+**	**P**	**Power for LED backlight anode**

Note (1): Be sure to apply the power voltage as the power sequence spec.
Note (2): DGND=AGND=0V



6.0 ELECTRICAL CHARACTERISTICS

6.1 TFT LCD Module

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	**VDDIN**	3.0	3.3	3.6	V
	AVDD	5.2	5.8	6.0	V
	AVEE	-6.0	-5.8	-5.2	V
Current for Driver	Iavdd		28	32	mA
	Iavee		17	20	mA
	Ivddin		33	40	mA
Input voltage 'H' level	VIH	0.7 VCI	-	VCI	V
Input voltage 'L' level	VIL	0	-	0.3 VCI	V

6.2 Back-Light Unit

The backlight system is an edge-lighting type with 20 LED.

The characteristics of the LED are shown in the following tables.

Item	Symbol	Min.	Typ.	Max.	Unit	Note
LED current	IL	-	80	-	mA	(2)
LED Voltage	VL	-	16	17.5	V	
Operating LED life time	Hr	50000	-	-	Hour	(1)(2)

Note (1) LED life time (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25±3 ℃, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note (2) The "LED life time" is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL=80mA. The LED lifetime could be decreased if operating IL is larger than 80mA. The constant current driving method is suggested.

6.3 AC Characteristics

DSI layer definitions

According Figure 4.21 DSI transmitter and receiver interface to understand simple interface block diagram. Then under diagram is internal block for DSI which include four types: PHY Layer, Lane Management Layer, Low level protocol and Application Layer.

The PHY Layer specifies the characteristics of transmission medium and electrical parameters for signaling the timing relationship between clock and Data Lanes.

The Lane Management Layer specifies DSI is Lane-scalable for increased performance. The data signals maybe transmission through one or more channel depending on the bandwidth requirements of the application.

The Protocol Layer specifies at the lowest level, DSI protocol specifies the sequence and value of bits and bytes traversing the interface. It specifies how bytes are organized into defined groups called packets.

The Application Layer describes higher-level encoding and interpretation of data contained in the data stream. The DSI specification describes the mapping of pixel values, commands and command's parameters to bytes in the packet assembly.

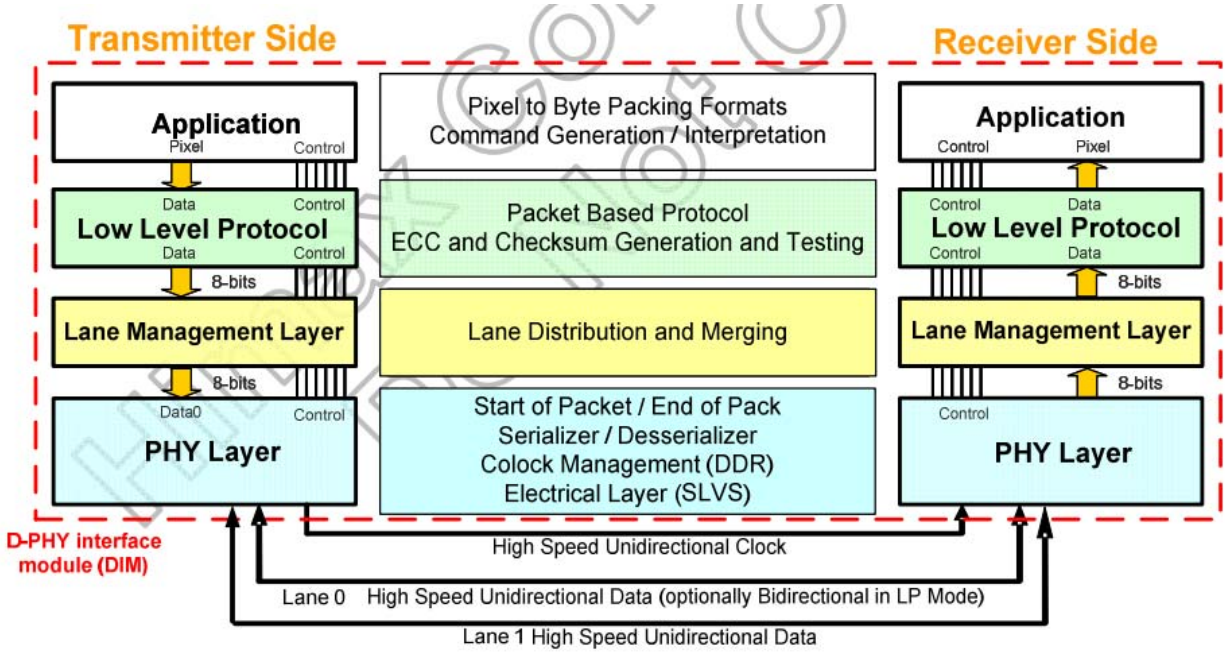


Figure 4.21: DSI layer

The state code of HS and LP Lane pair are defined as below:

State Code	Line Voltage Levels		High-Speed	Low-Power	
	Dp-Line	Dn-Line	Burst Mode	Control Mode	Escape Mode
HS-0	HS Low	HS High	Differential-0	Note(1)	Note(1)
HS-1	HS High	HS Low	Differential-1	Note(1)	Note(1)
LP-00	LP Low	LP Low	N/A	Bridge	Space
LP-01	LP Low	LP High	N/A	HS-Rqst	Mark-0
LP-10	LP High	LP Low	N/A	LP-Rqst	Mark-1
LP-11	LP High	LP High	N/A	Stop	Note(2)

Note: (1) During High-Speed transmission the Low-Power Receivers observe LP-00 on the Lines.
(2) If LP-11 occurs during Escape mode the Lane returns to Stop state **(Control Mode LP-11)**

Clock lane mode

Figure 4.22 shows the state diagram for Clock Lane Mode. The Clock Lane has three different power modes: Low Power Stop State, Ultra Low Power State **(ULPS)** and High Speed clock transmission.

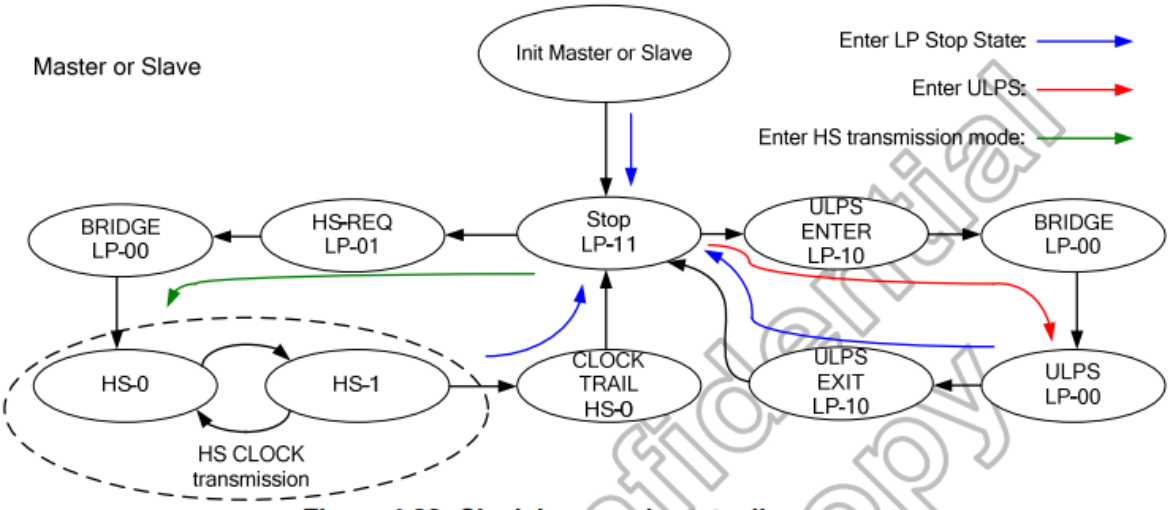
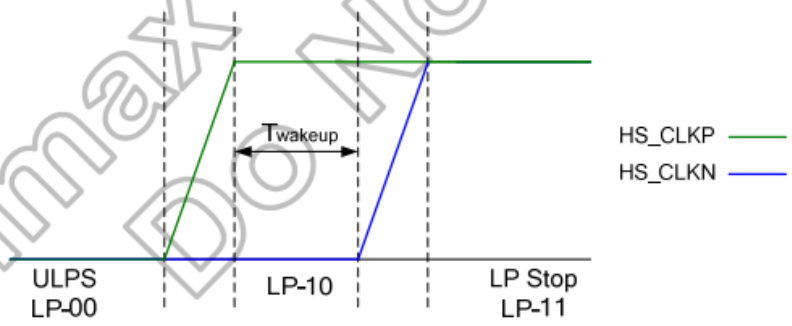


Figure 4.22: Clock lane mode state diagram

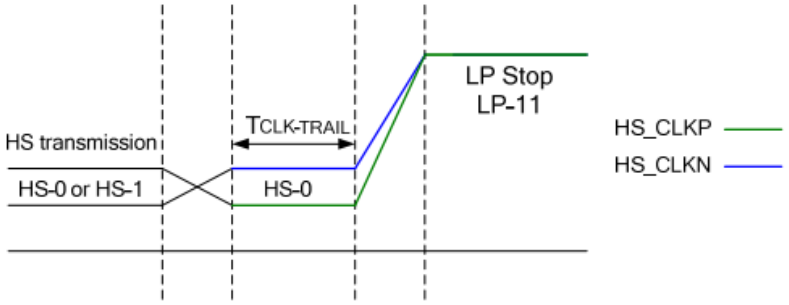
Clock Lane can be driven LP-11 to enter Low Power Stop State. There are three ways to enter Lower Power Stop State:

A. After Initial state **(HW reset, SW reset, Power on sequence)**.

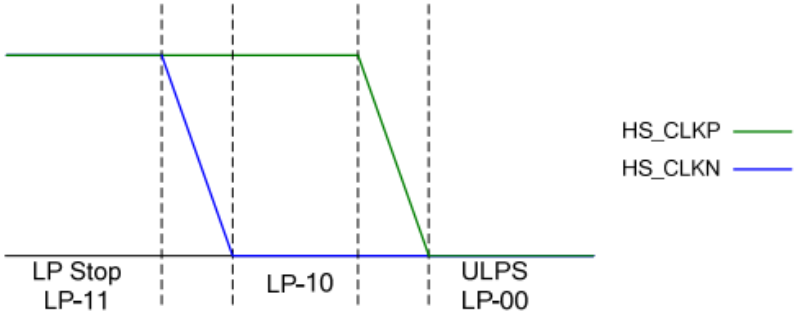
B. Leaving ULPS: ULPS LP-00→ LP-10→ Low Power Stop State LP-11.



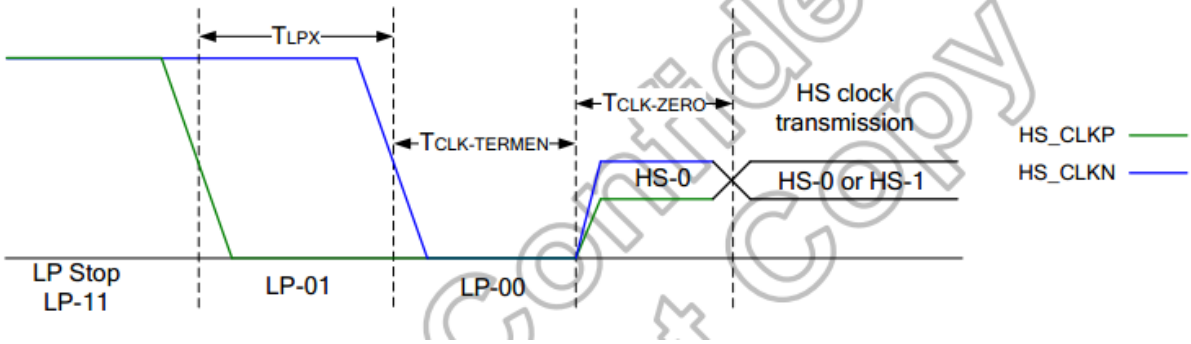
C. Leaving HS clock transmission mode: HS mode **(HS-0 or HS-1)**→HS-0→Low Power Stop State LP-11.



Clock Lane can be driven LP-00 to enter Ultra Low Power State from Low Power Stop State. The flow is Low Power Stop State LP-11→ LP-10→ULPS LP-00.



Clock Lane can be High Speed Clock Transmission State from Low Power Stop State. The flow is Low Power Stop State LP-11→LP-01→LP-00→HS-0→HS-0/1.



Data lane mode

Figure 4.23 shows the operational flow diagram for Data Lane Mode. There are three operating modes in Data Lane: Escape mode, High-Speed transmission mode and Turnaround.

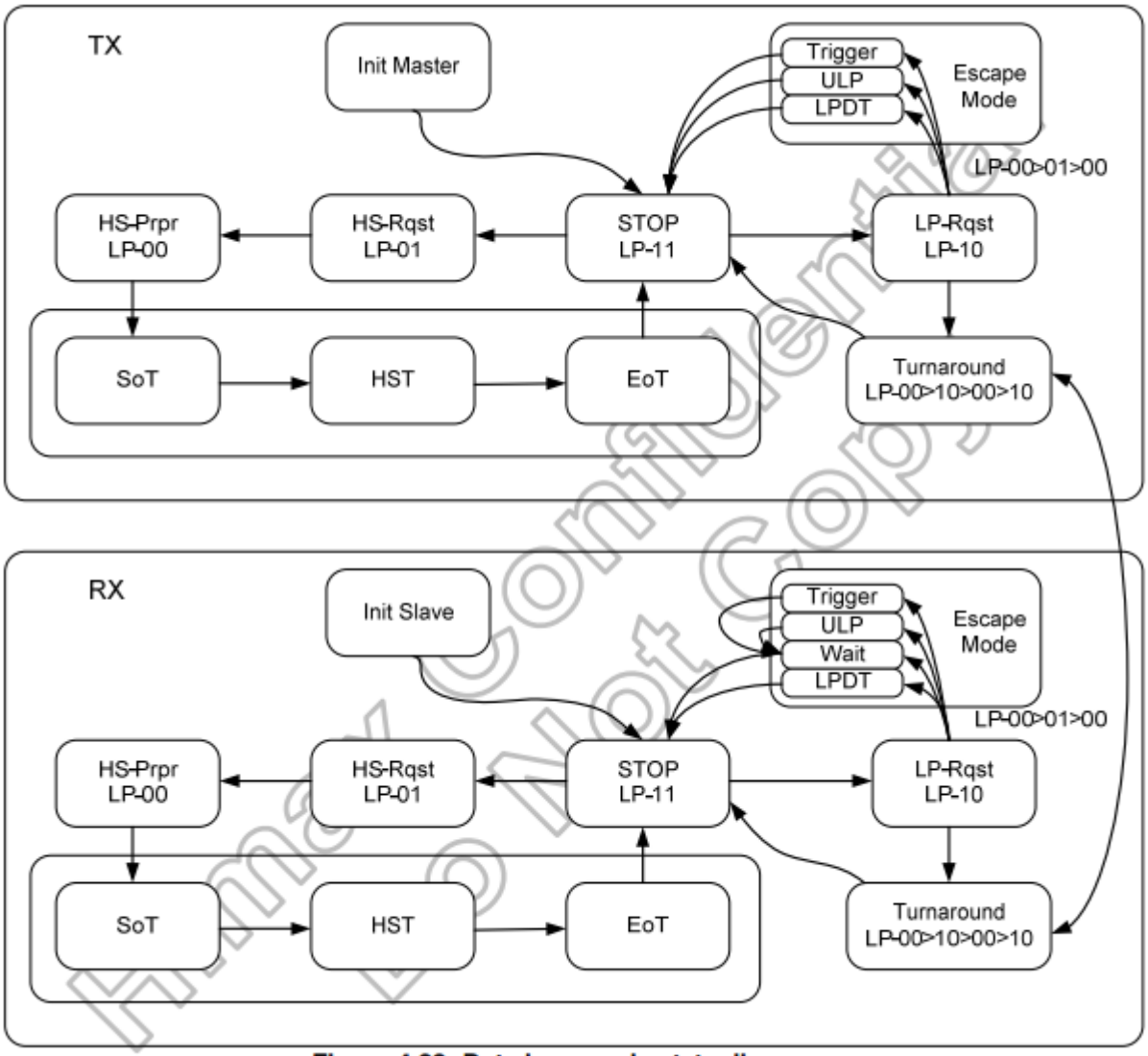


Figure 4.23: Data lane mode state diagram

Escape mode

Data Lane0 is used in Escape Mode when data lane in LP mode. Data Lane shall enter Escape mode via LP-11， LP-10， LP-00， LP-01， LP-00 and exit Escape mode via LP-10， LP-11.

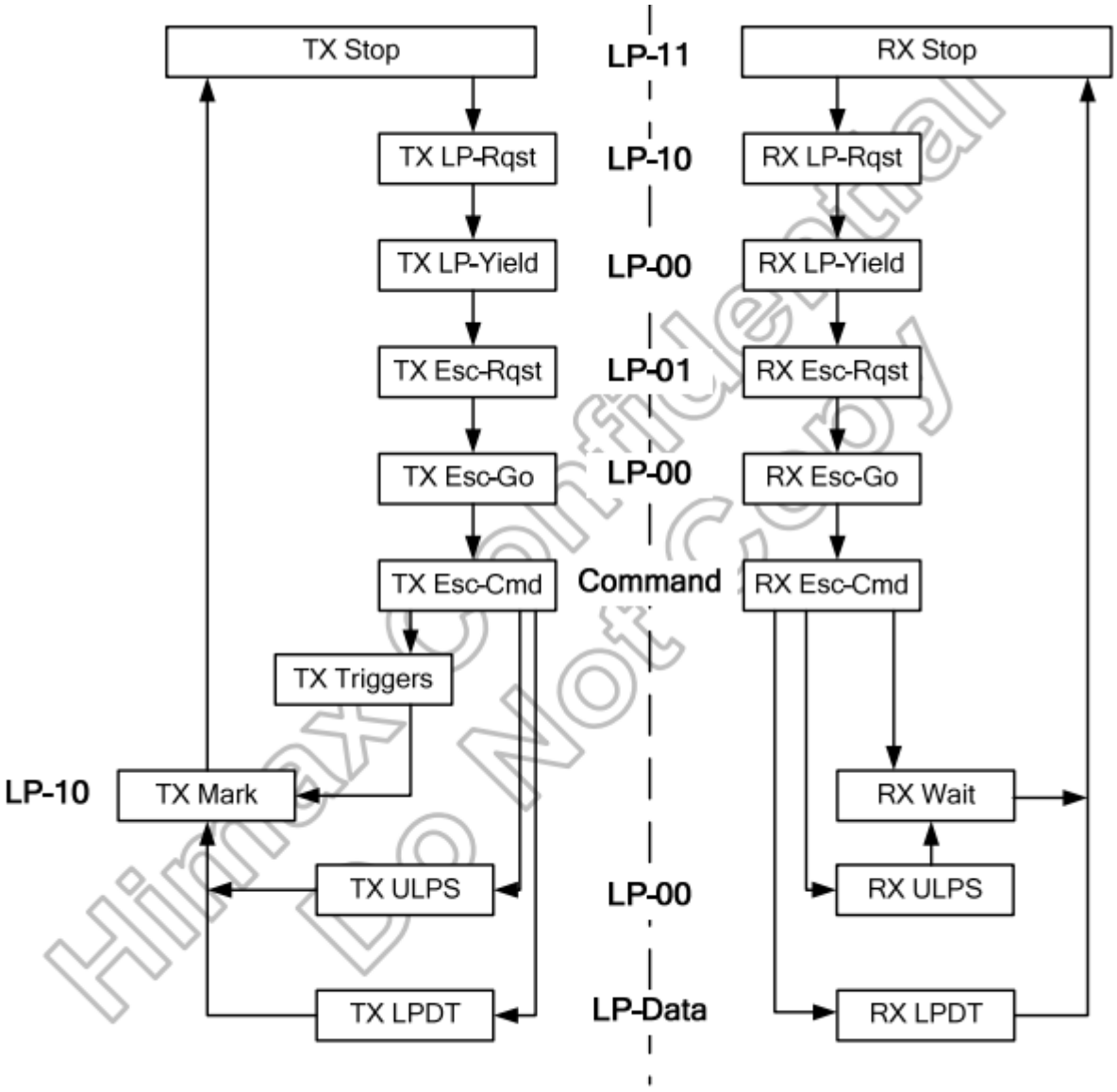


Figure 4.24: Escape mode state machine

Once Escape mode is entered, the transmitter shall send an 8-bit entry code to indicate the requested action. The Entry Code as follows:

A. Trigger **(Reset-Trigger(46h)**, Tearing effect **(BAh)**, Acknowledge **(84h)**
B. Drive Data Lane to Ultra Low Power State **(78h)**
C. Send Low Power Data Transmission **(87h)**

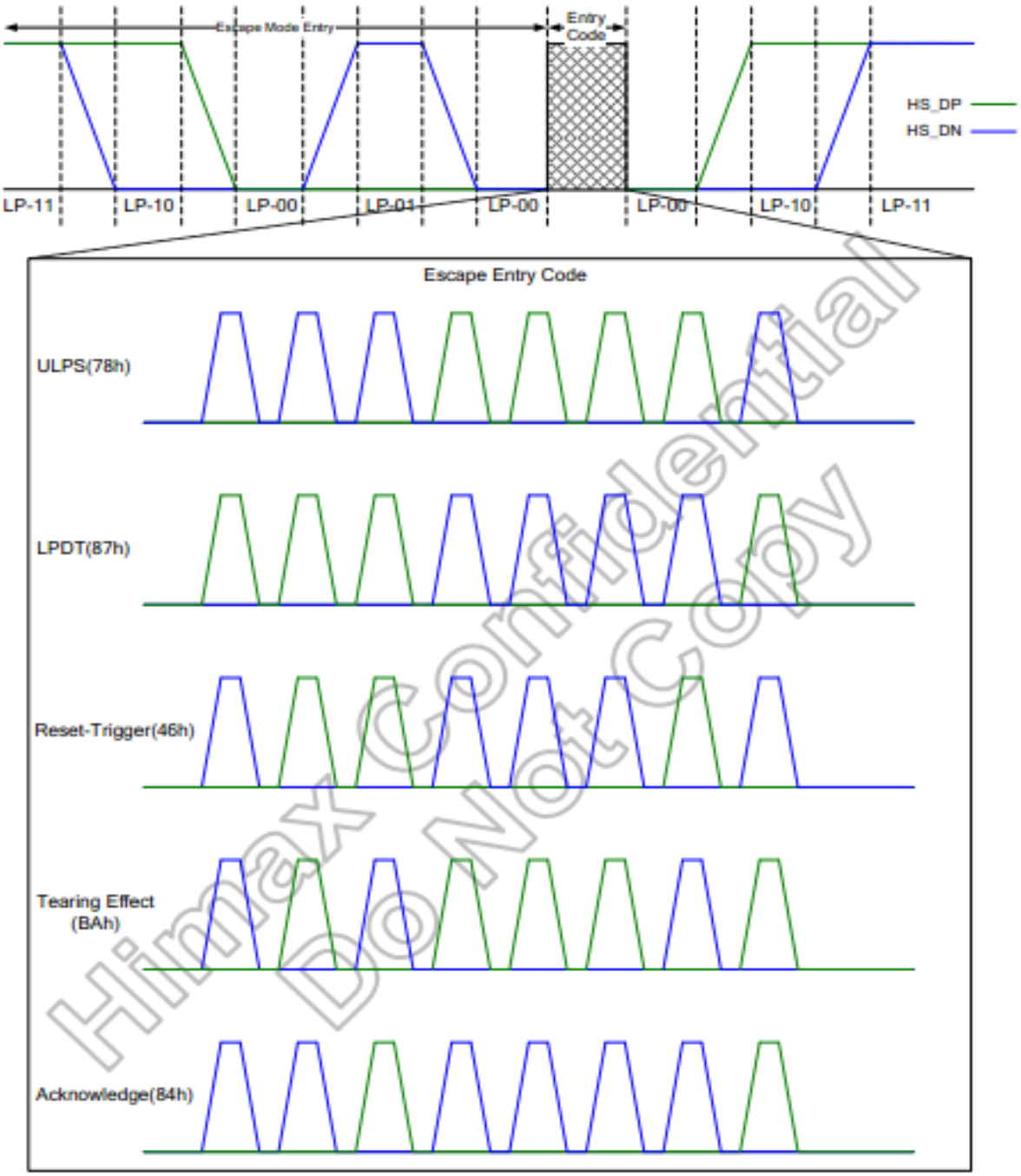


Figure 4.25: Escape mode timing sequence

High speed data transmission

The display module can enter High Speed Data Transmission when Clock Lane in the High Speed Clock Mode. All Data Lane enter High Speed Data Transmission synchronously but may end at different time. Data Lane enters High Speed Data Transmission by the flow: LP-11→LP-01→LP-00→SoT (**HS-00011101**), and exits High Speed Data Transmission by the flow: Toggle the last payload data bit to different state immediately and keeps that state for a time $T_{HS-TRAIL}$.

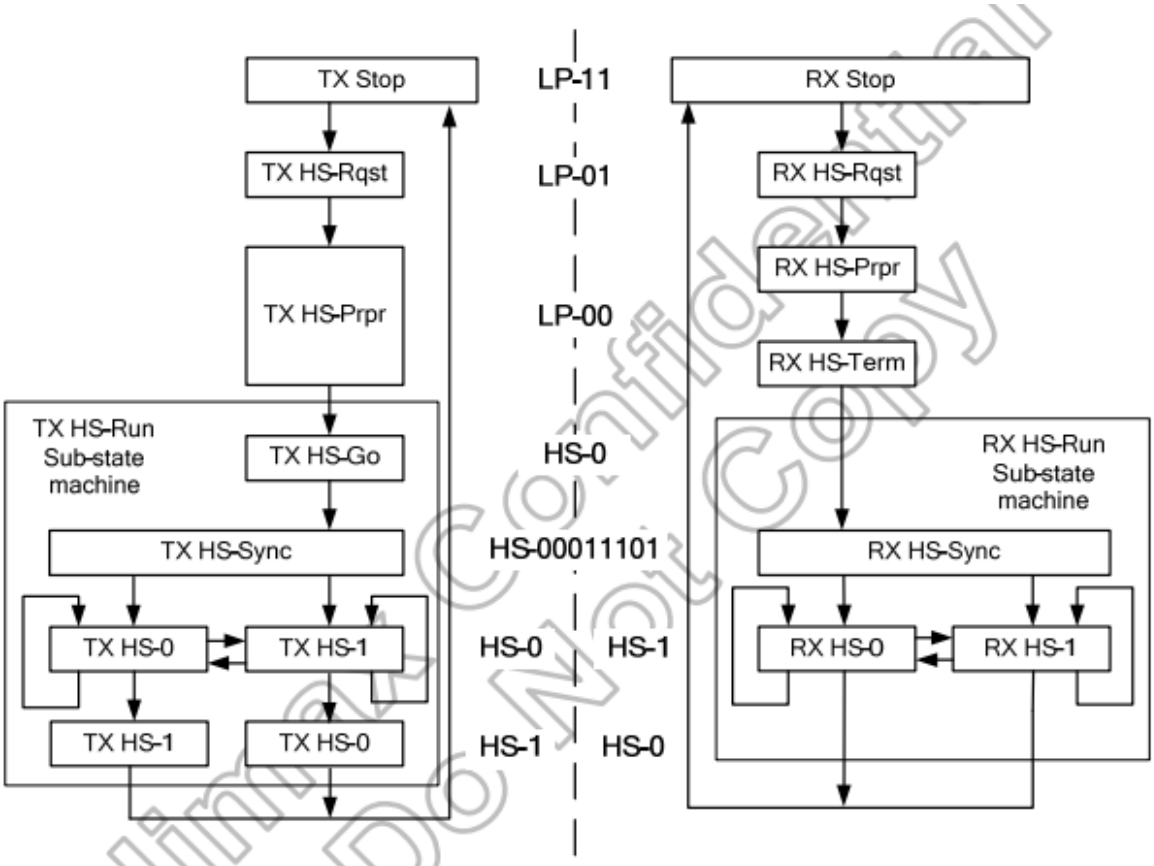


Figure 4.26: High speed data transmission state machine

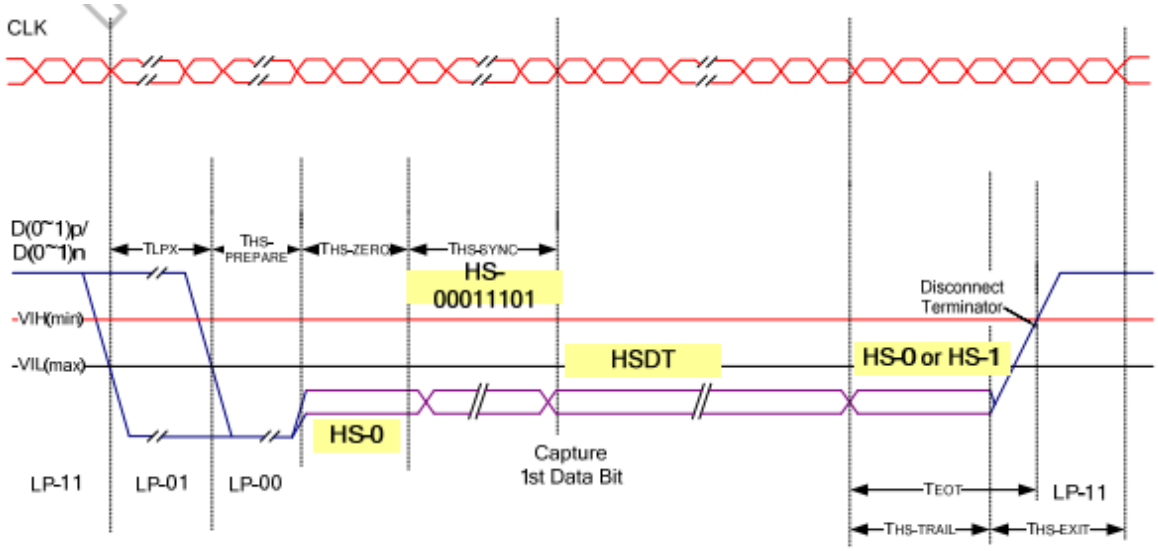


Figure 4.27: High speed data transmission timing sequence

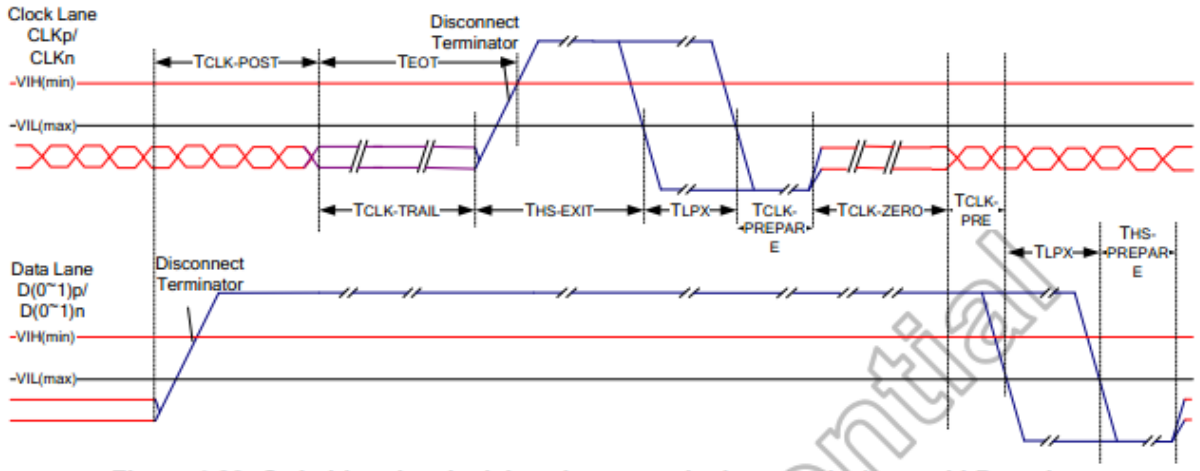


Figure 4.28: Switching the clock lane between clock transmission and LP mode

Bi-directional data lane turnaround

The transmission direction of a bi-directional Data Lane can be swapped by means of a Link Turnaround procedure. This procedure enables information transfer in the opposite direction of the current direction. The procedure is the same for either a change from Forward-to-Reverse direction or Reverse-to-Forward direction.

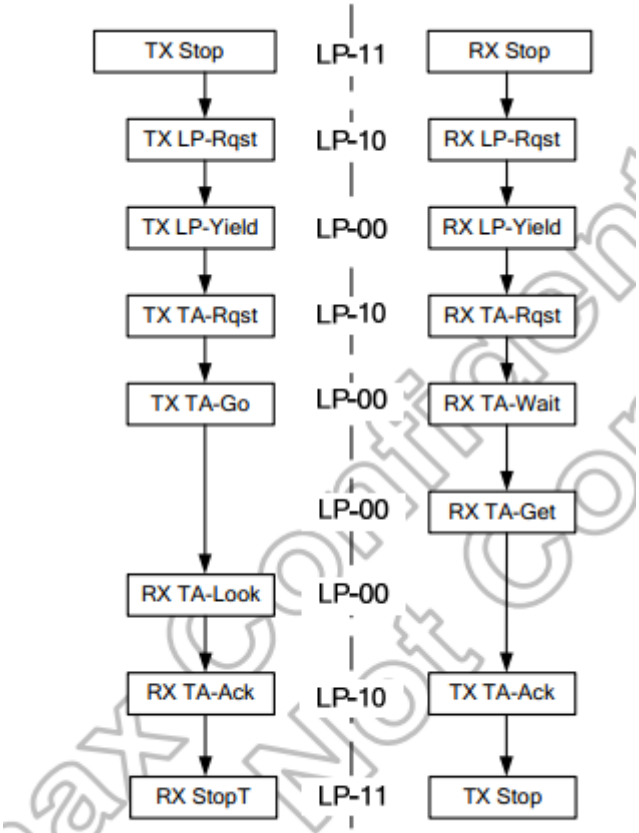
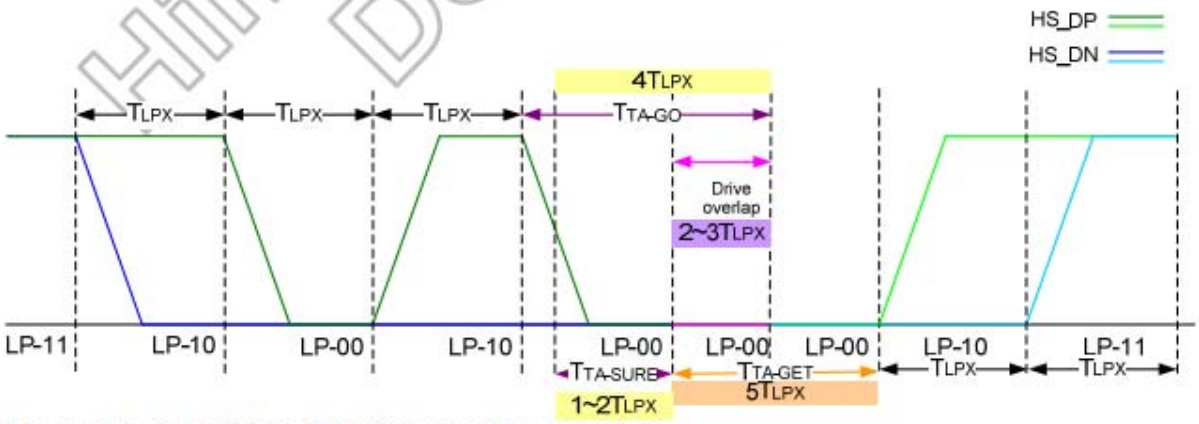


Figure 4.29: Turnaround state machine



Note: (1) Ratio of TLPX**(Master)**/TLPX**(Slave)** is between 2/3~3/2

Figure 4.30: Turnaround procedure

DSI protocol

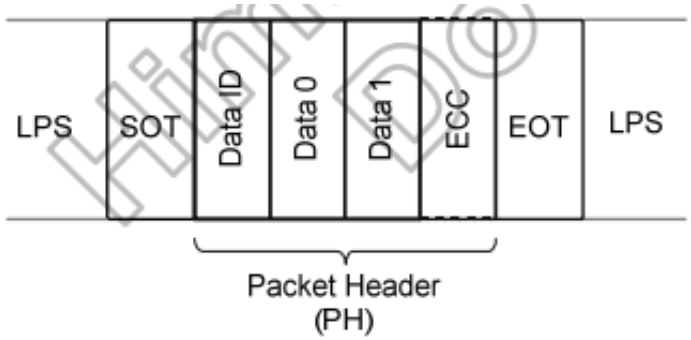
The protocol layer appends packet-protocol information and headers. The receiver side of a DSI Link performs the converse of the transmitter side, decomposing the packet into parallel data, signal events and commands. The DSI protocol permits multiple packets which is useful for events such as peripheral initialization, where many registers may be loaded with separate write commands at system startup. Figure 4.31 illustrates a case where multiple packets are being sent separately.

LPS：Low power state
SOT：Start of Transmission
SP：Short Packet
LP：Long Packet
EOT：End of Transmission

Figure 4.31: Separate HS transmission packets

The packet includes two types which are Long packet and Short packet. The first byte of the packet, the Data Identifier (**DI**), includes information specifying the type of the packet.

Short packets shall contain an 8-bit Data ID followed by two command or data bytes and an 8-bit ECC; a Packet Footer shall not be present. Short packets shall be four bytes in length. Figure 4.32 shows the structure of the Short packet.

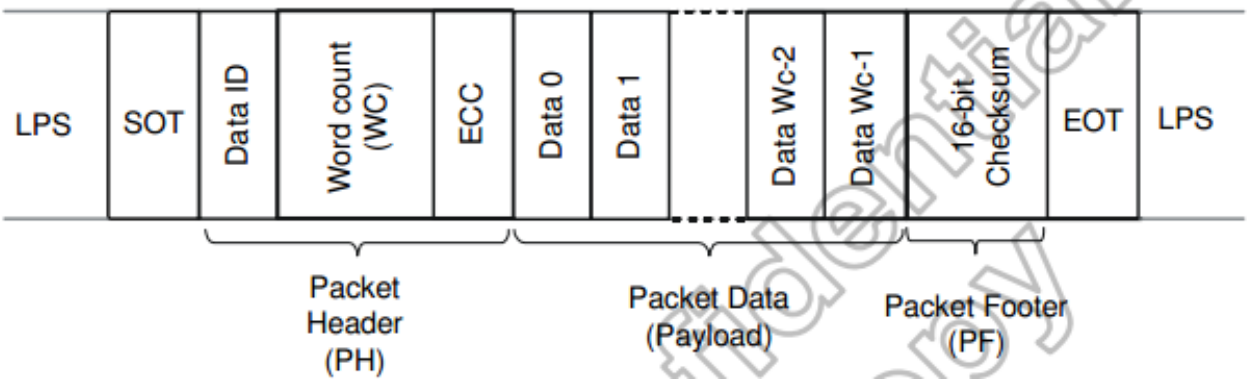


DI (Data ID): Contain Virtual Channel Identifier and Data Type.
ECC (Error Correction Code): The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header.

Figure 4.32: Short packet structure

Long packets specify the payload length using a two-byte Word Count Field and then the payload maybe from 0 to 65,541 bytes in length. Long packets permit transmission of large blocks of pixel or other data. Figure 4.33 shows the structure of the Long packet. Long Packet Header composed of three elements: an 8-bit Data Identifier, a 16-bit Word Count, and 8-bit ECC. The Packet Footer has one element, a 16-bit checksum. Long packets can be from 6 to 65,541 bytes in length.

Where 65,541 bytes = (2^{16}-1) + 4 bytes PH + 2 bytes PF



DI (Data ID): Contain Virtual Channel Identifier and Data Type.
WC (Word Count): The receiver use WC to define packet end.
ECC (Error Correction Code): The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header.
PF (Packet Footer): 16-bit Checksum.

Figure 4.33: Long packet structure

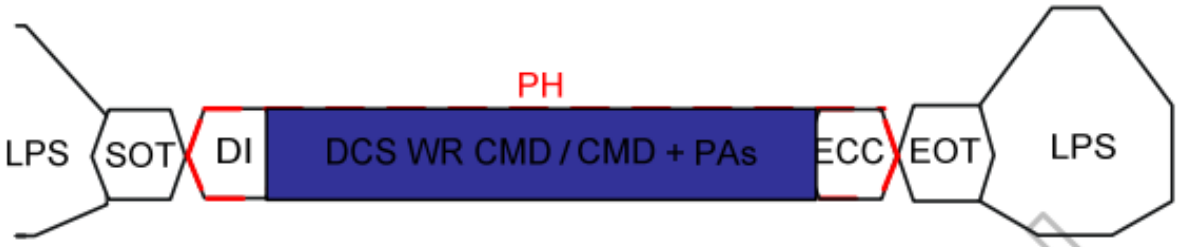
According to packet form, basic elements include DI and ECC. Figure 4.34 shows the format of Data ID.

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
VC (**Virtual Channel**)		DT (**Data Type**)					

DI[7:6]: These 2-bit identify the data as directed to one of four virtual channels.
DI[5:0]: These 6-bit specify the Data Type, which specifies the size, format and, in some cases, the interpretation of the packet contents.

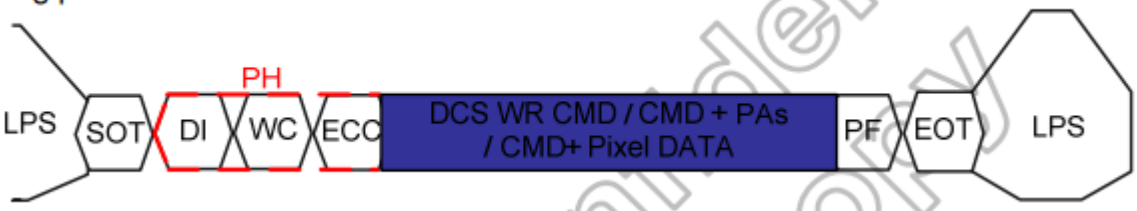
Figure 4.34: The format of data ID

Figure 4.35 show Short / Long-packet command transmission sequence.
Short packet writes Command / Parameters:



DI ➔ Write suitable Data type.
Ex: One CMD write, DI + DCS WR CMD
CMD + PAs write, DI + DCS WR CMD + PAs

Long packet write Command / Parameters / Pixel Data:



DI ➔ Write suitable Data type.
WC ➔ Write number of Payload Data.
Ex: One CMD write, WC setting as **1.**
CMD + PAs write, WC setting as number of (CMD+PAs).
CMD + DATA write, WC setting as number of (CMD + Pixel DATA).

Figure 4.35: Short/long packet command transmission sequence

6.3.1 Timing

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Clock Frequency	fclk	40.8	51.2	67.2	MHz	Frame rate =60Hz
Horizontal display area	thd		800		DCLK	
Horizontal Back Porch	HBP		20		DCLK	
Horizontal Pulse Width	HS		20		DCLK	
Horizontal Front Porch	HFP		32		DCLK	
HS Blanking	thb		72		DCLK	
HS period time	th		872		DCLK	
Vertical display area	tvd		1280		H	
Vertical Back Porch	VBP		6		H	
Vertical Pulse Width	VS		4		H	
Vertical Front Porch	HFP		8		H	
VS Blanking	thb		18		H	
VS period time	tv		1298		H	

7.0 Reliability test items

NO.	Item	Conditions	Remark
1	High Temperature Storage	Ta=+80℃,240hrs	Inspection after2～4 hours storage at room temperature, the sample shall be free from defects 1. Air bubble in the LCD 2. Seal leak 3. non-display 4. missing segments 5. glass crack 6. Current idd is twice higher than initial value.
2	Low Temperature Storage	Ta=-30℃,240hrs	
3	High Temperature Operation	Ta=+70℃,240hrs	
4	Low Temperature Operation	Ta=-20℃,240hrs	
5	High Temperature and High Humidity(Operation)	Ta=+60℃, 90%RH, 240hrs	
6	Thermal cycling Test (non operation)	-20℃(30min)→+70℃(30min),100cycles	
7	Electrostatic discharge	200V 200pf(0ohm) 1time/each terminal	
8	Vibration	1. Random: 1.04 Grms,5～500HZ, X/Y/Z,30min/each direction 2. Sine: Freq. Range:8～33.3hz Stoke:1.3mm Sweep:2.9G,33.3～400HZ X/Z:2hr,Y:4hr,cyc:15min	
9	Shock	100G,6ms,±X, ±Y, ±Z 3 times for each direction	JIS C7021,A-10 (Condition)
10	Vibration(with carton)	Random:0.015G∧2/HZ, 5～200HZ -6dB/octave,200～400HZ XYZ each dirction:2hr	
11	Drop (with carton)	Height:60cm 1corner,3edges,6surfaces	JIS Z0202

Note:

1.There is no display function NG issue occurred, all the cosmetic specification is judged before the reliability stress.

2.the test samples should be applied to only one test item

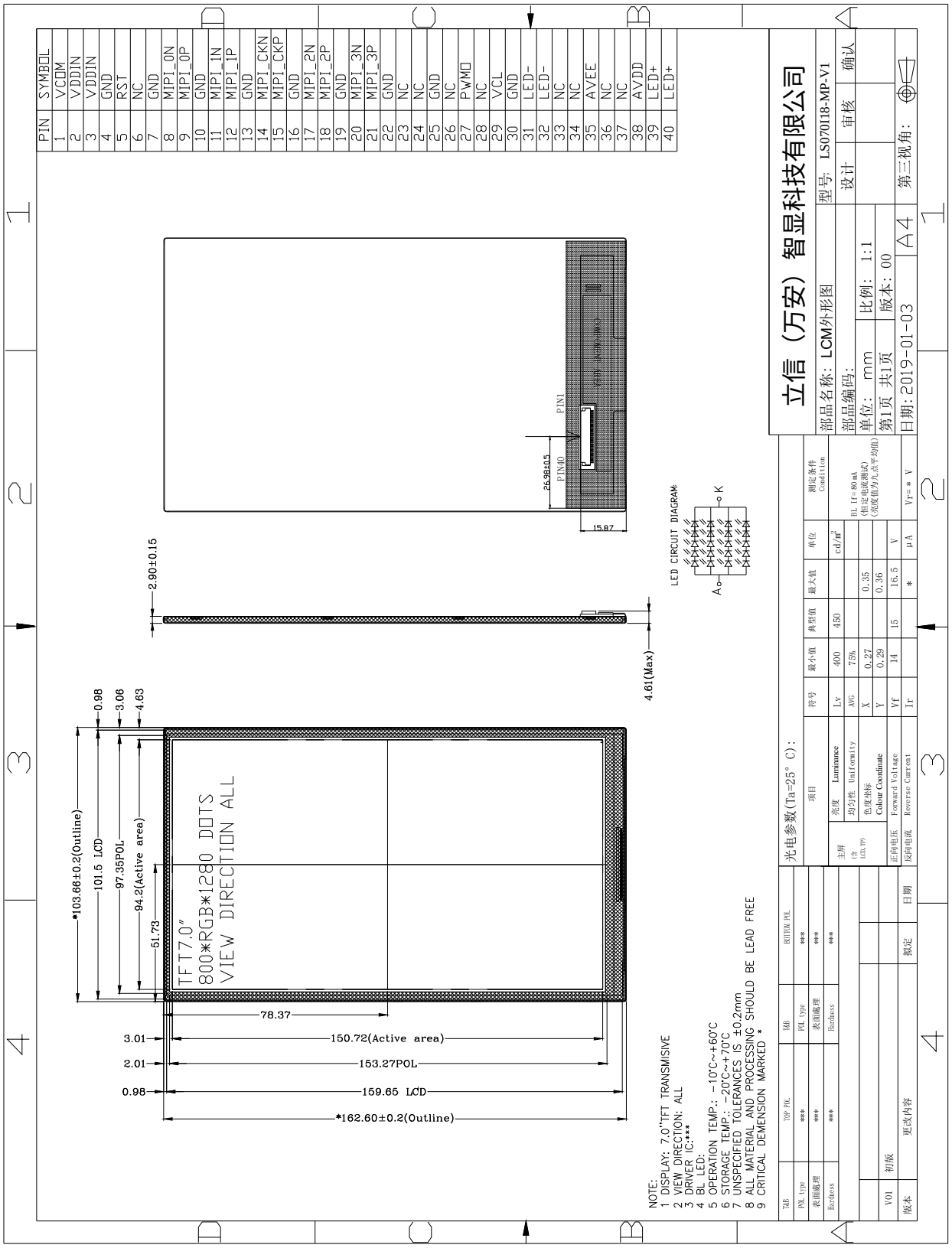
3.for damp proof test, Pure water(resistance>10M ohm)should be used

4.in case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part

5.Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic

8.0 OUTLINE DIMENSION

Outline Dimension:



9.0 GENERAL PRECAUTION

9.1 Use Restriction

This product is not authorized for use in life supporting systems, aircraft navigation control systems, military systems and any other application where performance failure could be life threatening or otherwise catastrophic.

9.2 Disassembling or Modification

Do not disassemble or modify the module. It may damage sensitive parts inside LCD module, and may cause scratches or dust on the display. HannStar does not warrant the module, if customers disassemble or modify the module.

9.3 Breakage of LCD Panel

9.3.1.If LCD panel is broken and liquid crystal spills out, do not ingest or inhale liquid crystal, and do not contact liquid crystal with skin.
9.3.2. If liquid crystal contacts mouth or eyes, rinse out with water immediately.
9.3.3. If liquid crystal contacts skin or cloths, wash it off immediately with alcohol and rinse thoroughly with water.
9.3.4. Handle carefully with chips of glass that may cause injury, when the glass is broken.

9.4 Electric Shock

9.4.1. Disconnect power supply before handling LCD module.
9.4.2. Do not pull or fold the LED cable.
9.4.3. Do not touch the parts inside LCD modules and the fluorescent LED's connector or cables in order to prevent electric shock.

9.5 Absolute Maximum Ratings and Power Protection Circuit

9.5.1. Do not exceed the absolute maximum rating values, such as the supply voltage variation, input voltage variation, variation in parts' parameters, environmental temperature, etc., otherwise LCD module may be damaged. 9.5.2. Please do not leave LCD module in the environment of high humidity and high temperature for a long time. 11.5.3. It's recommended to employ protection circuit for power supply.

9.6 Operation

9.6.1 Do not touch, push or rub the polarizer with anything harder than HB pencil lead.
9.6.2 Use fingerstalls of soft gloves in order to keep clean display quality, when persons handle the LCD module for incoming inspection or assembly.

9.6.3 When the surface is dusty, please wipe gently with absorbent cotton or other soft material.

9.6.4 Wipe off saliva or water drops as soon as possible. If saliva or water drops contact with polarizer for a long time, they may causes deformation or color fading.

9.6.5 When cleaning the adhesives, please use absorbent cotton wetted with a little petroleum benzine or other adequate solvent.

9.7 Mechanism

Please mount LCD module by using mouting holes arranged in four corners tightly.

9.8 Static Electricity

9.8.1 Protection film must remove very slowly from the surface of LCD module to prevent from electrostatic occurrence.

9.8.2. Because LCD module use CMOS-IC on circuit board and TFT-LCD panel, it is very weak to electrostatic discharge. Please be careful with electrostatic discharge. Persons who handle the module should be grounded through adequate methods.

9.9 Strong Light Exposure

The module shall not be exposed under strong light such as direct sunlight. Otherwise, display characteristics may be changed.

9.10 Disposal

When disposing LCD module, obey the local environmental regulations.

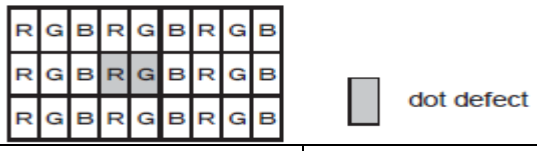
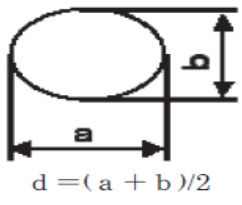
10. Package Specification

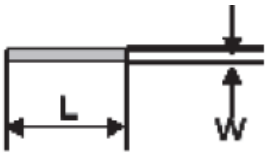
10.1 Packing format

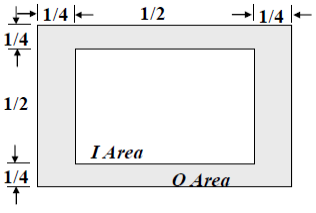
(1) package quantity in one carton :60PCS .

(2) Carton size:43mmX37mmX18mm.

11.Visuals Specification: 1)Note

<table>
<tr><td>General</td><td colspan="3">1. Customer identified anomalies not defined within this inspection standard shall be reviewed by LowKey, and an additional standard shall be determined by mutual consent.
2. This inspection standard about the image quality shall be applied to any defect within the effective viewing area and shall not be applicable to outside of the area.
3. Inspection conditions
Luminance : 500 Lux min.
Inspection distance : 300 mm.
Temperature : 25±5°C
Direction : Directly above</td></tr>
<tr><td rowspan="7">Definition of inspection item</td><td rowspan="3">Dot defect</td><td>Bright dot defect</td><td>The dot is constantly “on” when power applied to the LCD, even when all “Black” data sent to the screen. Inspection tool: 5% Transparency neutral density filter.Count dot: If the dot is visible through the filter. Don’t count dot: If the dot is not visible through the filter.
 
</td></tr>
<tr><td>Black dot defect</td><td>The dot is constantly “off” when power applied to the LCD, even when all “White” data sent to the screen.</td></tr>
<tr><td>Adjacent dot</td><td>Adjacent dot defect is defined as two or more bright dot defects or black dot defects.
 
</td></tr>
<tr><td>External inspection</td><td>Bubble ,scratch(foreign Particle polarizer, Cell, Backlight)</td><td>Visible operating (all pixels “Black” or “White”) and non operating.</td></tr>
<tr><td rowspan="2"></td><td>Appearance inspection</td><td>Does not satisfy the value at the spec.</td></tr>
<tr><td>Others</td><td>LED wires</td><td>Damaged to the LED wires, connector, pin, functional failure or appearance failure.</td></tr>
<tr><td></td><td>Definition of Size</td><td colspan="2">Definition of circle : definition of linear size definition Area I/O
 




</td></tr>
</table>

2) Standard

Classification		Inspection item			Judgment Standard	
Defect (in LCD glass)	Dot defect	Area			I	O
		Bright dots(Note: Visible under:ND5%) 1:D≤0.15mm:No count); D>0.15mm acceptable: 2			N≤0	N≤2
		Dark dots (0.15mm<D≤0.3mm), D>0.3mm Not allowable			N≤3	
		Bright dot-2Adjacent			N≤0	
		Dark dot-2Adjacent			N≤0	
		Dark or bright dots-3 and more adjacent(note6)			N≤0	
		Total bright and dark dots			N≤5	
		Minimum distance between bright dots			5mm	
		Minimum distance between dark dots			5mm	
		Minimum distance between bright and bright dots			5mm	
	Other	White dot ,dark dot (circle)	Size (mm)	Acceptable number		
			d≤0.2	Neglected		
			0.2mm<D≤0.3mm	N≤4		
			0.3mm<D≤0.4mm	N≤2		
			D>0.4mm	Not allowable		
Visual defect		Foreign partial	Circular foreign material: dark/bright sport	Visible under:ND5% 1:D≤0.2mm:No count 2:0.2mm<D≤0.3mm,N≤4 3:D>0.3mm:Not allowable		
			Linear foreign material: bright or dark line	Invisible under ND5% 0.1mm<W≤0.3mm, 0.3mm<L≤1.5mm,N≤4 Visible under ND5% 0.05mm≤w≤0.1mm, 0.3mm≤L≤0.7mm,N≤4		
		Polarizer	Linear scratch	1:BM:No Count 2:Pixel area 0.05mm≤w≤0.2mm, 1.0mm≤L≤5.0mm,N≤4		
			Bubble peeling	1:BM:No Count 2:Pixel area 0.15mm≤D<0.3mm,N≤4		
		Mura & leak		ND5%		