PRODUCT SPECIFICATION FOR LCD MODULE

Revision: 1.0

Model No: LS070T06-R-V1

Module Type: COG+FPC+B/L

APPROVED SIGNATURE

■ Approved Product Specification only
□ Approved Product Specification and Samples

Prepared By	Checked By	Approved By

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1. General Description

LS070T06-R-V1 is a transmissive type a-Si TFT-LCD (amorphous silicon thin film transistor liquid crystal display) module, which is composed of a TFT-LCD panel, a driver circuit and a backlight unit. The panel size is 7.0 inch and the resolution is 800(RGB)*480, the panel can display up to 16.7M colors.The is intended to support applications where thin thickness, wide viewing angle and low power are critical factors and graphic displays are important.

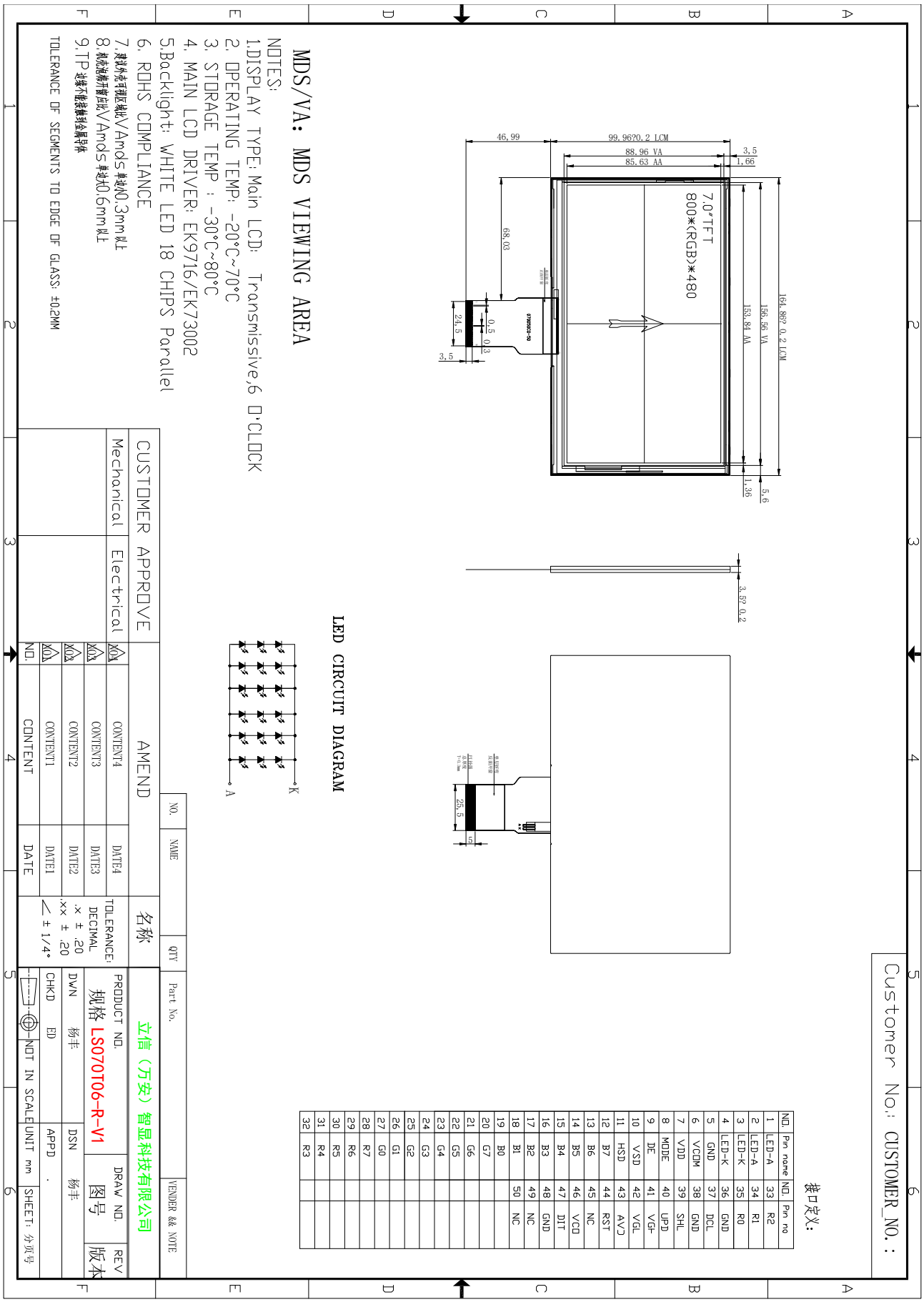
2. Physical Features

Display Mode	TFT-LCD Module
	Active matrix TFT, Transmissive type
Display Format	Graphic 800(RGB)×480 Dot-matrix
Input Data	RGB
Viewing Direction （Grayscale Inversion）	6 O'CLOCK
Drive	EK9716/EK73002

3. Mechanical Specification

Item	Specification	Unit
Module size (H×V×D)	164.86 ×99.96 ×3.5	mm
Number of dots	800(RGB) ×480	pixel
Active area (H×V)	154.08×85.92	mm

4. Outline Dimension



NO.	Pin name	NO.	Pin no
1	LED-A	33	R2
2	LED-A	34	R1
3	LED-K	35	R0
4	LED-K	36	GND
5	GND	37	DCL
6	VCOM	38	GND
7	VDD	39	SHL
8	MODE	40	UPD
9	DE	41	VGH
10	VSD	42	VGL
11	HSD	43	AVD
12	B7	44	RST
13	B6	45	NC
14	B5	46	VCD
15	B4	47	DIT
16	B3	48	GND
17	B2	49	NC
18	B1	50	NC
19	B0		
20	G7		
21	G6		
22	G5		
23	G4		
24	G3		
25	G2		
26	G1		
27	G0		
28	R7		
29	R6		
30	R5		
31	R4		
32	R3		

5. Absolute Maximum Ratings

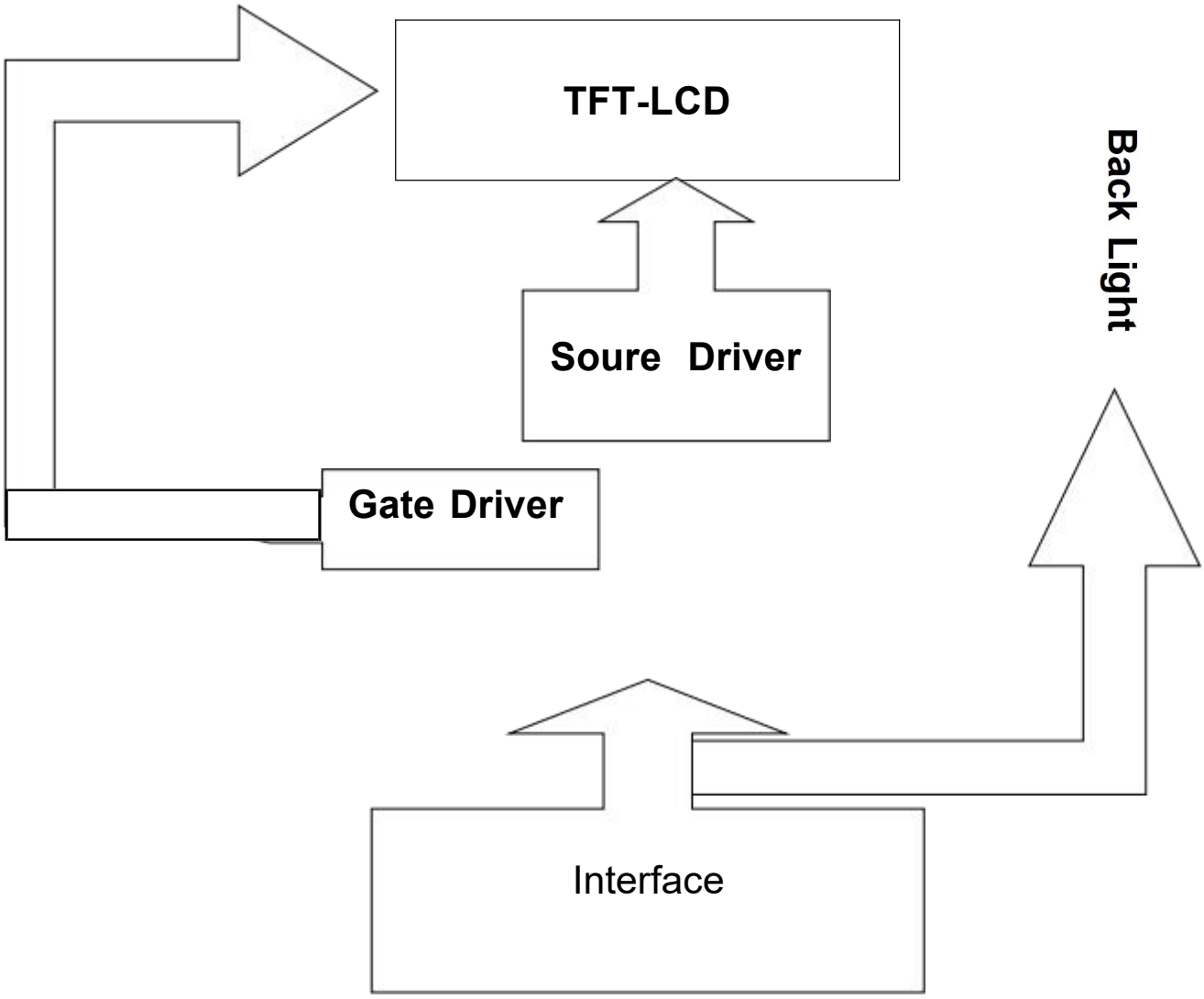
Item	Symbol	Min	Max	Unit	Remark
Supply voltage	VDD	-0.3	3.3	V	Note1 Note2
Supply voltage	VCI	-0.3	5.0	V	
Operating temperature	TOPR	-20	70	℃	
Storage temperature	TSTR	-30	80	℃	

6. Electrical Characteristics

Item		Symbol	Rating			Unit	Remark
			Min	Typ	Max		
Supply voltage		VDD	3.2	3.3	3.4	V	Note1
Supply voltage		VGH	15	16	17	V	
Supply voltage		VGL	-8	-7	-6		
Supply voltage		AVDD	9.5	10	10.5		
Supply voltage		VCOM	3.5	3.7	3.9		
Input Voltage	L level	VIL	0	---	0.1*VDD	V	
	H level	VIH	0.9*VDD	---	VDD	V	

7. Module Function Description

7-1. Block Diagram Of LCM



7-2. Pin Description

PIN NO.	Symbol	I/O	Description
1	VLEDA+	P	Power for LED backlight (Anode)
2	LLEDA+	P	Power for LED backlight (Anode)
3	VLED-	P	Power for LED backlight (Catgode)
4	VLED-	P	Power for LED backlight (Catgode)
5	GND	P	Power ground
6	VCOM	I	Common Voltage
7	DVDD	P	Digital Power
8	MODE	I	DE/SYNC mode select Normally pull high H;DE mode.L:HSD/VSD mode
9	DE	I	Data Enable signal
10	VS	I	Vertical sync input.Negative polarity
11	HS	I	Horizontal sync input.Negative polarity
12	B7	I	Blue Data lnput(MSB)
13	B6	I	Blue Data lnput
14	B5	I	Blue Data lnput
15	B4	I	Blue Data lnput
16	B3	I	Blue Data lnput
17	B2	I	Blue Data lnput
18	B1	I	Blue Data lnput
19	B0	I	Blue Data lnput(LSB)
20	G7	I	Green Data lnput(MSB)
21	G6	I	Green Data lnput
22	G5	I	Green Data lnput
23	G4	I	Green Data lnput
24	G3	I	Green Data lnput
25	G2	I	Green Data lnput
26	G1	I	Green Data lnput

27	G0	I	Green Data lnput(LSB)
28	R7	I	Red Data lnput(MSB)
29	R6	I	Red Data lnput
30	R5	I	Red Data lnput
31	R4	I	Red Data lnput
32	R3	I	Red Data lnput
33	R2	I	Red Data lnput
34	R1	I	Red Data lnput
35	R0	I	Red Data lnput(LSB)
36	GND	P	Power ground
37	DCLK	I	Clock input
38	GND	P	Power ground
39	SHLR	I	Left or Right DisplayControl
40	UPDN	I	Up/Down Display Control
41	VGH	P	Positive Power for TFT
42	VGL	P	Negative Power forTFT
43	AVDD	P	Analog Power
44	RSTB	I	Global reset pin Active low to enter reset state. Suggest to connecting with an RC reset circuit for stability. Normally pull high.(R=10KΩ，C=1μF)
45	NC		Not connect
46	VCOM	I	Common Voltage
47	DITH	I	Dithering setting DITH=”H” 6bit resolution(last 2 bit of input data truncated) DITH=”L” 8bit resolution(default setting)
48	GND	P	Power ground
49	NC		Not connect
50	NC		Not connect

7-3 Timing Characteristics

Table 16. Horizontal input timing

Parameter	Symbol	Value			Unit	Note
Horizontal display area	thd	800			DCLK	
DCLK frequency	fclk	Min.	Typ.	Max		
		28.2	29.2	46.5	MHz	
1 Horizontal Line	th	908	928	1088	DCLK	thb+thpw=88 DCLK is fixed.
HSD pulse width	thpw	1	48	87		
HSD Back Porch (Blanking)	thb	87	40	1		
HSD Front Porch	thfp	20	40	200		

Table 17. Vertical input timing

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Vertical display area	tvd		480		H	
VSD period time	tv	517	525	712	H	tvpw+tvb=32H Is fixed
VSD pulse width	tvpw	1	1	3	H	
VSD Back Porch (Blanking)	tvb	31	31	29	H	
VSD Front Porch	tvfp	5	13	200	H	

7.5. Timing Table

Table 31. Parallel 24-bit RGB Mode

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CLKIN Frequency(Dual gate)	Fclk	VDD = 3.3V	-	29.2	46.5	MHz
CLKIN Cycle Time(Dual gate)	Tclk	-	22	34	-	ns
CLKIN Frequency(cascade)	Fclk	VDD = 3.3V	-	29.2	40	MHz
CLKIN Cycle Time(cascade)	Tclk	-	25	34	-	ns
CLKIN Pulse Duty	Tcwh	Tclk	40	50	60	%
Time from HSD to Source Output	Thso	-	-	46	-	CLKIN
Time from HSD to LD	Thld	-	-	46	-	CLKIN
Time from HSD to STV	Thstv	-	-	2	-	CLKIN
Time from HSD to CKV	Thckv	-	-	20	-	CLKIN
Time from HSD to OEV	Thoev	-	-	4	-	CLKIN
LD Pulse W idth	Twld			10		CLKIN
CKV Pulse Width	Twckv	-	-	66	-	CLKIN
OEV Pulse Width	Twoev	-	-	74	-	CLKIN

7.6. Timing Waveform

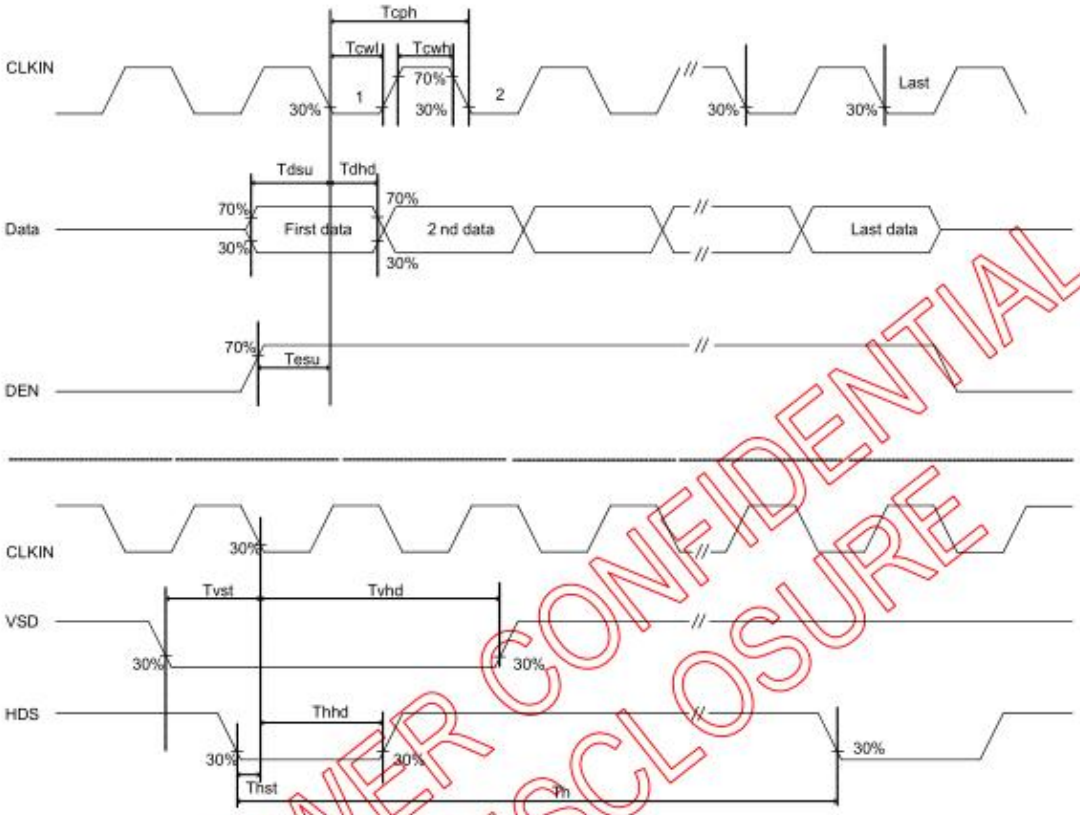


Figure 10. Input Clock and Data Timing Diagram

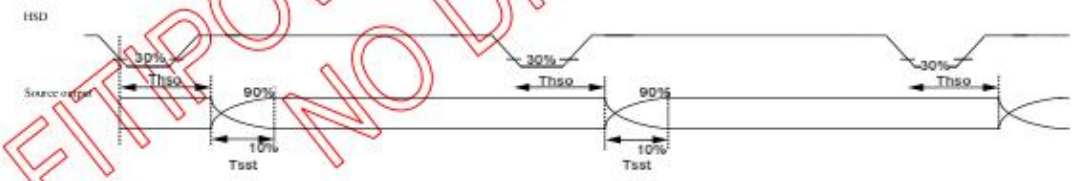


Figure 11. Source Output Timing Diagram(Cascade)

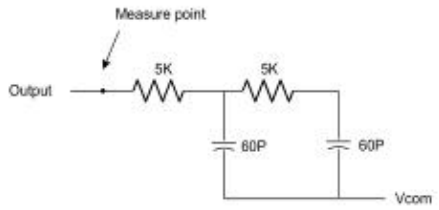


Figure 12. Output load condition

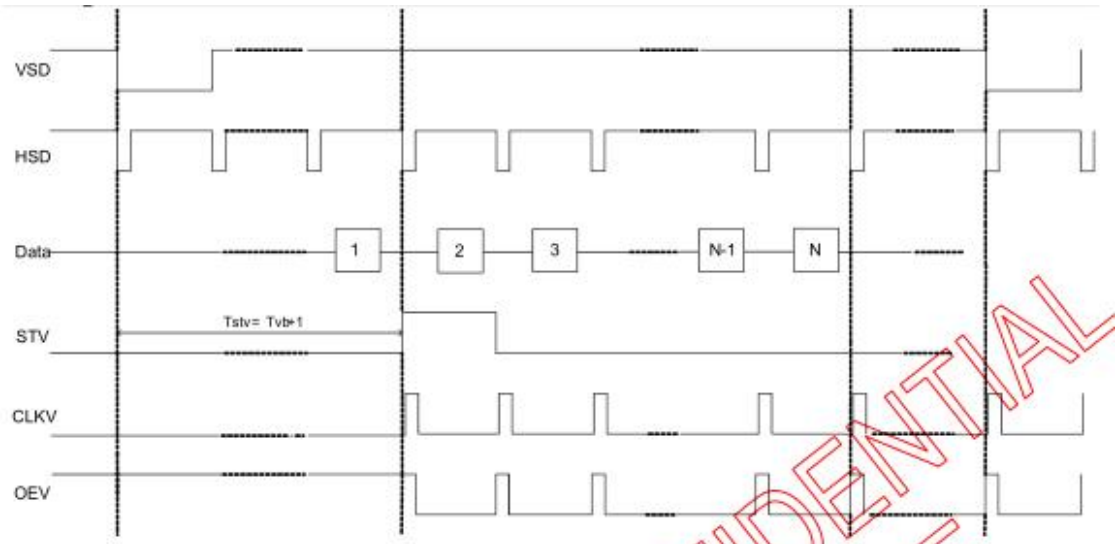


Figure 13. Vertical Timing Diagram HV (Cascade)

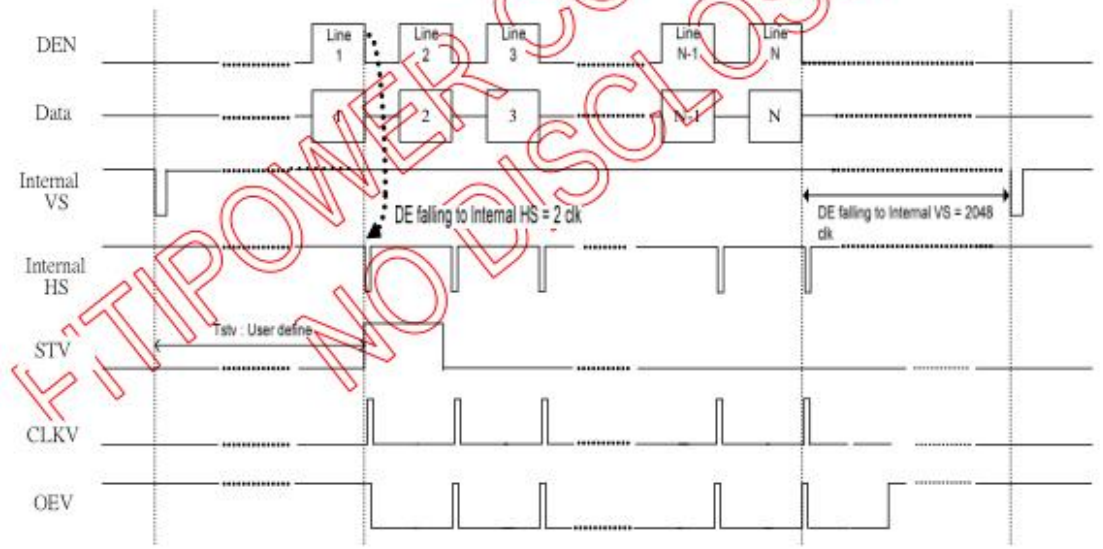


Figure 14. Vertical Timing Diagram DE (Cascade)

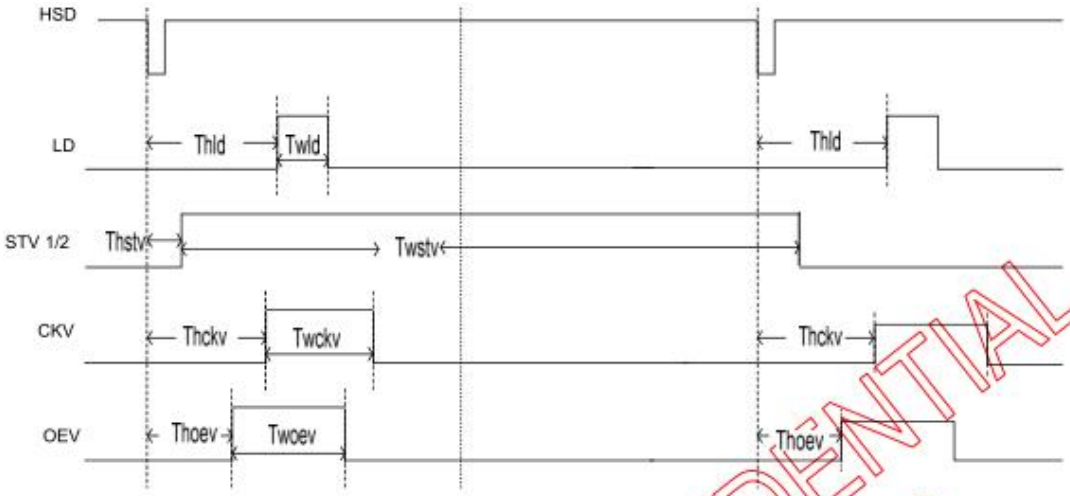


Figure 15. Gate Output Timing Diagram (Cascade)

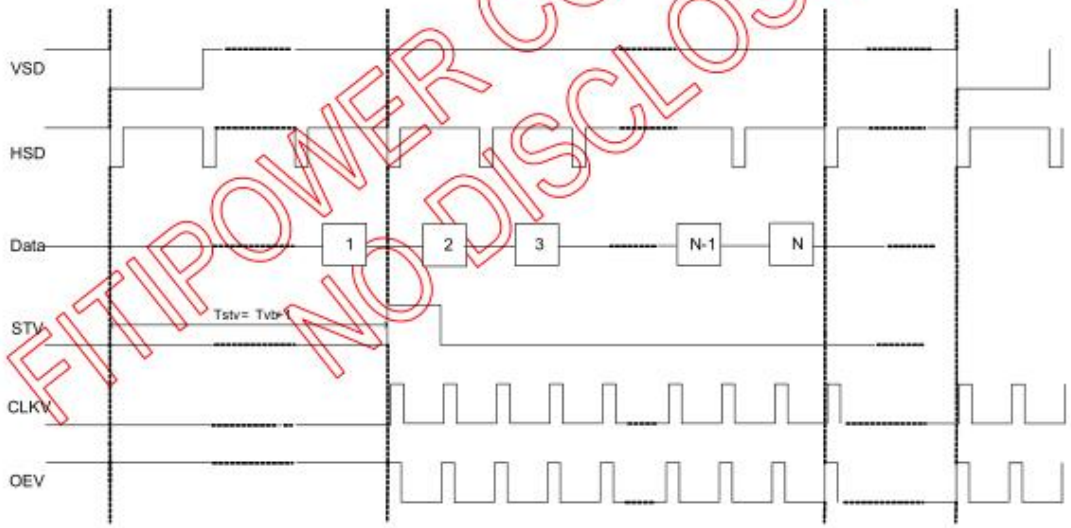


Figure 16. Vertical Timing Diagram HV (Dual Gate)

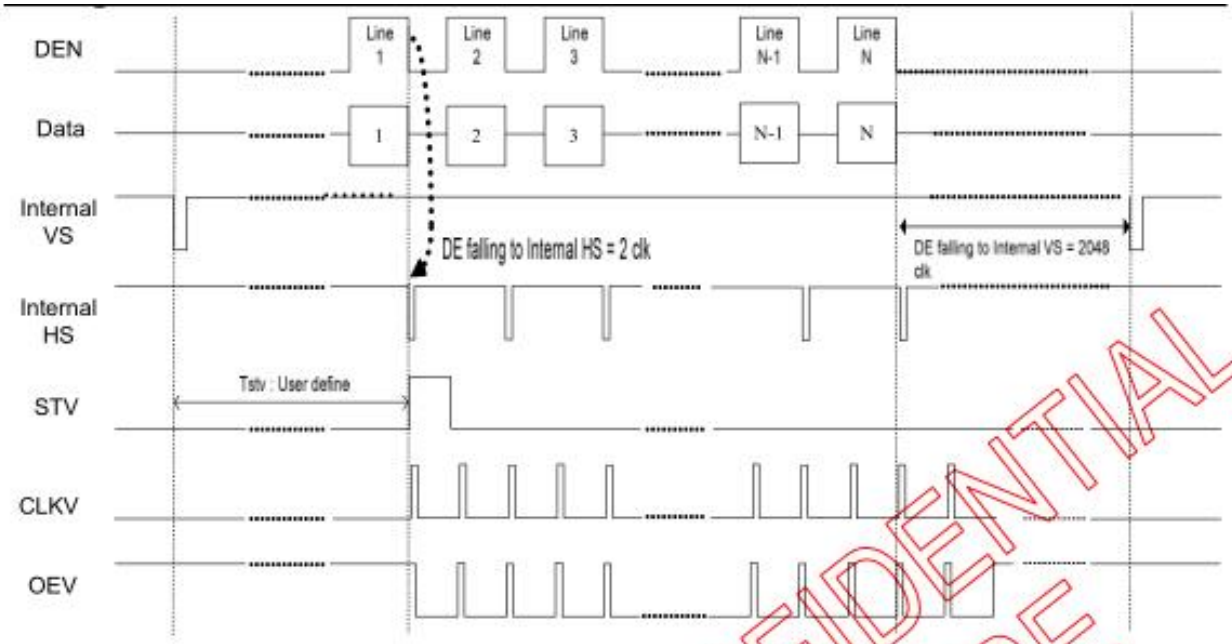


Figure 17. Vertical Timing Diagram DE (Dual Gate)

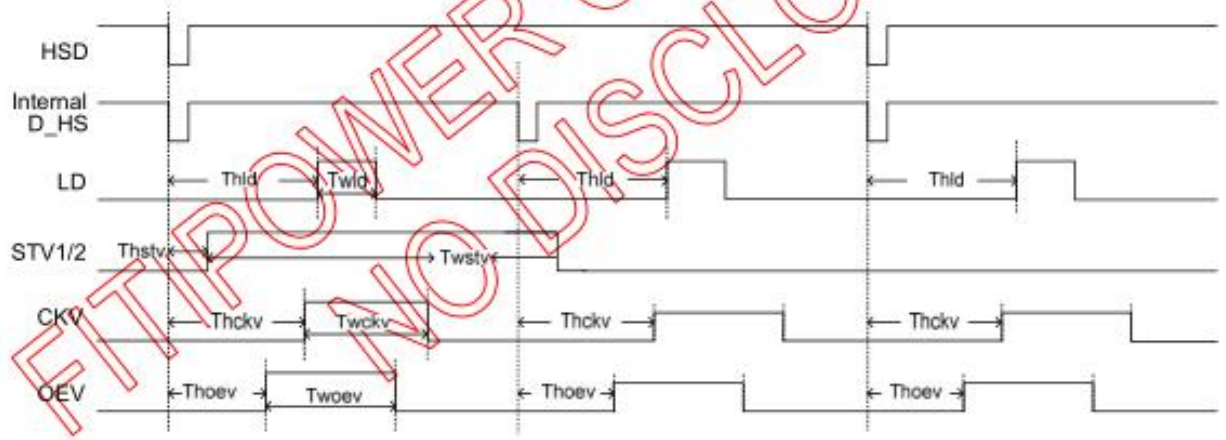
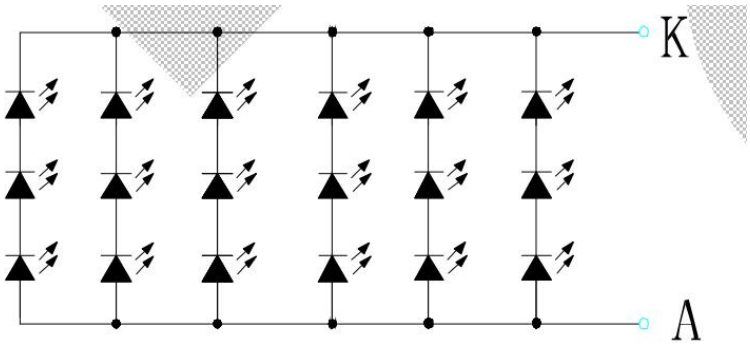


Figure 18. Gate Output Timing Diagram (Dual Gate)

8. Electro-Optical Characteristics

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time		Tr +Tf	θx = θy =0	---	TBD	TBD	ms	Note 1
Contrast Ratio		CR		---	500	---	---	Note 2
Transmittance		T%		5	5.5	---	%	
Color Chromaticity (CIE1931)	White	W x	θx = θy =0	0.276	0.306	---	---	
		W y		0.314	0.344	---	---	
Viewing angle	θ_T		CR > 10	60	70	---	Deg.	Note 3
	θ_B			60	70	---		
	θ_L			50	60	---		
	θ_R			60	70	---		
Luminance (I_F = 120mA)		L		300	350	---	cd/m2	Note4

Note(4) Backlight circuit



LED 电路图

IF=120mA VF=9.6V

9.Records Of Version

Version	Revise Date	Page	Content
00	2024-3-15	ALL	New released