PRODUCT SPECIFICATION FOR LCD MODULE

Revision: 1.0

Model No: LS070I17-MP-V1

Module Type: COG+FPC+B/L

APPROVED SIGNATURE

■ Approved Product Specification only

□ Approved Product Specification and Samples

Prepared By	Checked By	Approved By

REVISION RECORD

REV NO	REV DATE	CONTENTS	REMARKS
V.0	2024.10.14	First Release	

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1.0 General description

1.1 Introduction

LS070I17-MP-V1 **is model a color active matrix thin film transistor (TFT) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. This model is composed of a TFT LCD panel, a driving circuit and a back light system. This TFT LCD has a 7.0 inch diagonally measured active display area with WSVGA (1024 horizontal by 600 vertical pixel array) resolution. The TFT-LCD panel used for this module is adapted for a low reflection and higher color type.**

1.2 Features

- **4 lanes MIPI Interface**
- Low driving voltage and low power consumption
- ROHS Compliant

1.3 General information

Item	Specification	Unit	Remarks
Outline Dimension	164.10(H) x 97 (V) x2.6(body)	mm	Tolerance:±0.2mm
Display area	154.2144(W) x85.92(H)	mm	
Number of Pixel	1024(H) x RGB x600(V)	pixels	
Pixel pitch	0.1506(H) x 0.1432(V)	mm	
Pixel arrangement	Pixels RGB stripe arrangement		
Display mode	Normally Black		
Surface treatment	IPS		
Back-light	Single LED (Side-Light type)		

2.0 ABSOLUTE MAXIMUM RATINGS

2.1 Electrical Absolute Rating

2.1.1 TFT LCD Module

Item		Specification	Unit
Outline Dimension		164.10(H) x 97 (V) x2.6(body)	mm
Display area		154.2144(W) x85.92(H)	mm
Number of Pixel		1024(H) x RGB x600(V)	pixels
Pixel pitch		0.1506(H) x 0.1432(V)	mm
Pixel arrangement		Pixels RGB stripe arrangement	
Display mode		Normally Black	
Surface treatment		IPS Film	
Weight		TBD (Typ.)	gram
Back-light		Single LED (Side-Light type)	
Power Consumption	B/L System	TBD(Max.)	watt

2.1.2 Back-Light Unit

Item	Symbol	Typ	MIN.	TYP.	MAX.	Unit	Note
Forward voltage	Vf	--	--	--	9.9	V	
Forward current	If	--	--	--	180	mA	
Power Consumption	PBL	--	--	--	--	mW	

Note:

(1) Permanent damage may occur to the LCD module if beyond this specification. Functional operation should be restricted to the conditions described under normal operating conditions.

(2) Ta =25±2℃

(3) Test Condition: LED current 140 mA

3.0 OPTICAL CHARACTERISTICS

3.1 Optical Specifications

Item	Symbol	Temp	Condition	Min	Typ	Max	Unit	Remark
Viewing Angle range	Horizontal	θ	CR > 10	80	85	--	Deg	Note 1
	Vertical	θ		80	85	--	Deg	
Luminance Contrast ratio		CR	θ = 0°	600：1	800	--	--	Note 2
Brightness		YL		250	300	--	Cd/cm2	
Transmittance		T(%)	θ = 0°	--	50	--	%	Note 3
Color Gamut (C light)				45	50	--	%	
White chromaticity		Wx	Θ=0°	TYP. -0.02	0.300	TYP. +0.02		Note 4
		Wy			0.340			
Reproduction of color （C-light）	Red	Rx			0.615			
		Ry			0.320			
	Green	Gx			0.296			
		Gy			0.569			
	Blue	Bx			0.142			
		By			0.174			
Response Time (Rising + Falling)	Trt		Ta= 25°C θ = 0°	--	25	40	ms	Note 5

3.2 Measuring Condition

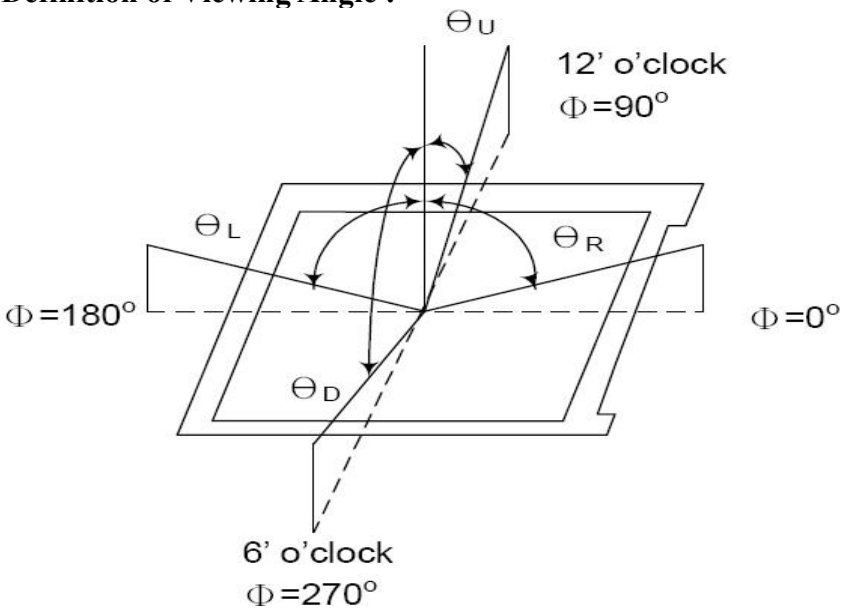
Measuring surrounding: dark room ,LED current IL : 140mA

Ambient temperature: 25±2℃ 15min. warm-up time.

3.3 Measuring Equipment

FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics. Measuring spot size: 20 ~ 21 mm

Note (1) Definition of Viewing Angle :

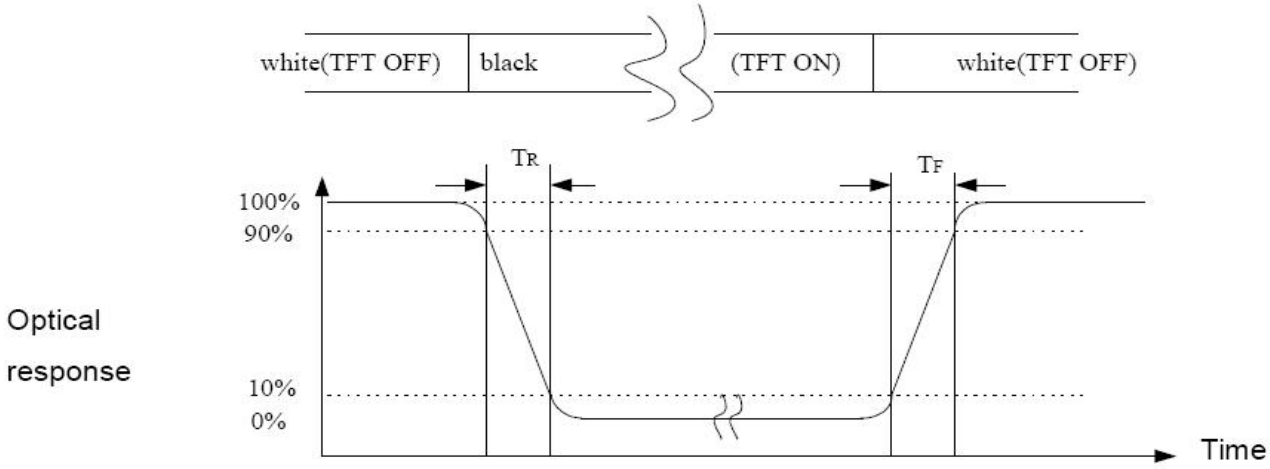


Note (2) Definition of Contrast Ratio (CR):

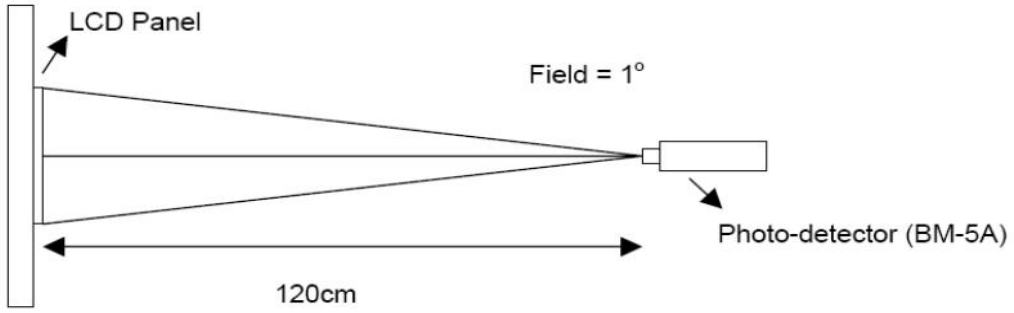
Measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

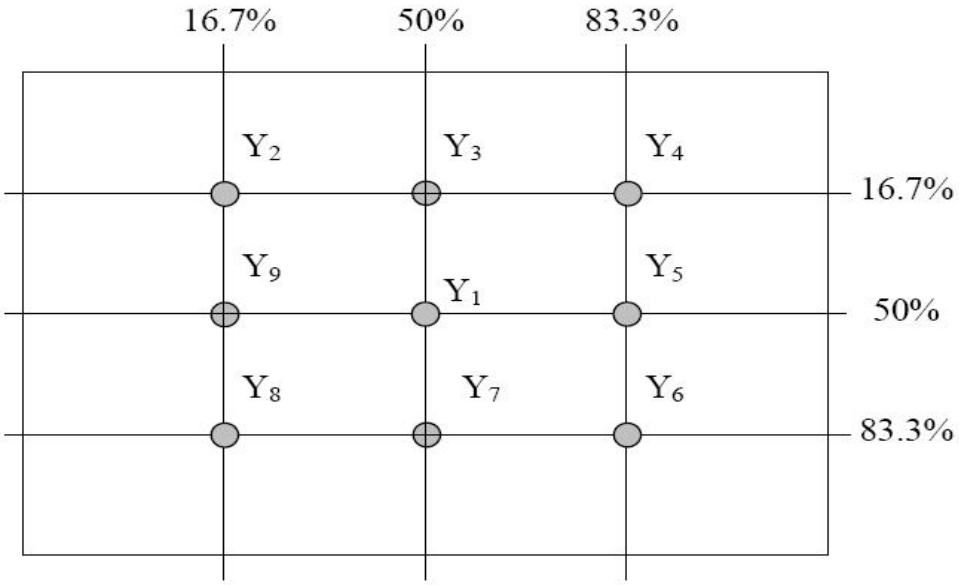
Note (3) Definition of Response Time: Sum of TR and TF



Note (4) Definition of optical measurement setup



Note (5) Definition of brightness uniformity



$$\text{Luminance uniformity} = \frac{\text{(Min Luminance of 9 points)}}{\text{(Max Luminance of 9 points)}} \times 100\%$$

4.0 INTERFACE PIN CONNECTION

4.1 Signal of interface

Terminal No.	Symbol	I/O	Functions
1--2	VLED+	P	Power for LED backlight (Anode)
3	VGH	P	Gate ON Voltage
4	VGL	P	Gate OFF Voltage
5	UPDN	I	Up/down selection
6	SHLR	I	Left / right selection
7--8	VLED-	P	Power for LED backlight (Cathode)
9	AVDD	P	Power for Analog Circuit
10	GND	P	Ground
11	MIPI_D3+	I	Positive MIPI differential data inputs3+
12	MIPI_D3-	I	Negative MIPI differential data inputs3-
13	GND	P	Ground
14	MIPI_D2+	I	Positive MIPI differential data inputs2+
15	MIPI_D2-	I	Negative MIPI differential data inputs2-
16	GND	P	Ground
17	MIPI_CLK+	I	Positive MIPI differential clock inputs+
18	MIPI_CLK-	I	Negative MIPI differential clock inputs-
19	GND	P	Ground
20	MIPI_D1+	I	Positive MIPI differential data inputs1+
21	MIPI_D1-	I	Negative MIPI differential data inputs1-
22	GND	P	Ground
23	MIPI_D0+	I	Positive MIPI differential data inputs0+
24	MIPI_D0-	I	Negative MIPI differential data inputs0-
25	GND	P	Ground
26	STBYB	I	Standby mode, normally pull high STBYB="1", normally operation STBYB="0", timing control, source driver will turn off
27	RESET	P	Global reset pin.
28	DVDD	P	Power for Digital Circuit
29	DVDD	P	Power for Digital Circuit
30	VCOM	P	Common voltage

5.0 FUNCTION DESCRIPTION

3.4 POWER SEQUENCE

In order to prevent IC from power on reset fail, the rising time(TPOR) of the digital power Supply VDD should be maintained within the given specifications. Refer to “AC Characteristics” for more detail on timing.

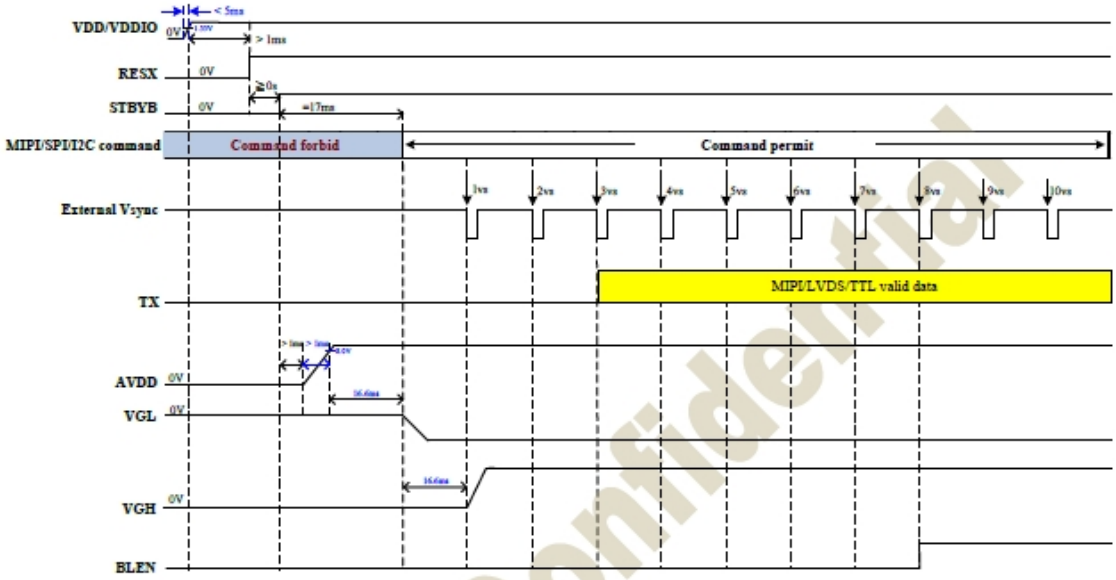


Figure 5.1: Power On timing chart

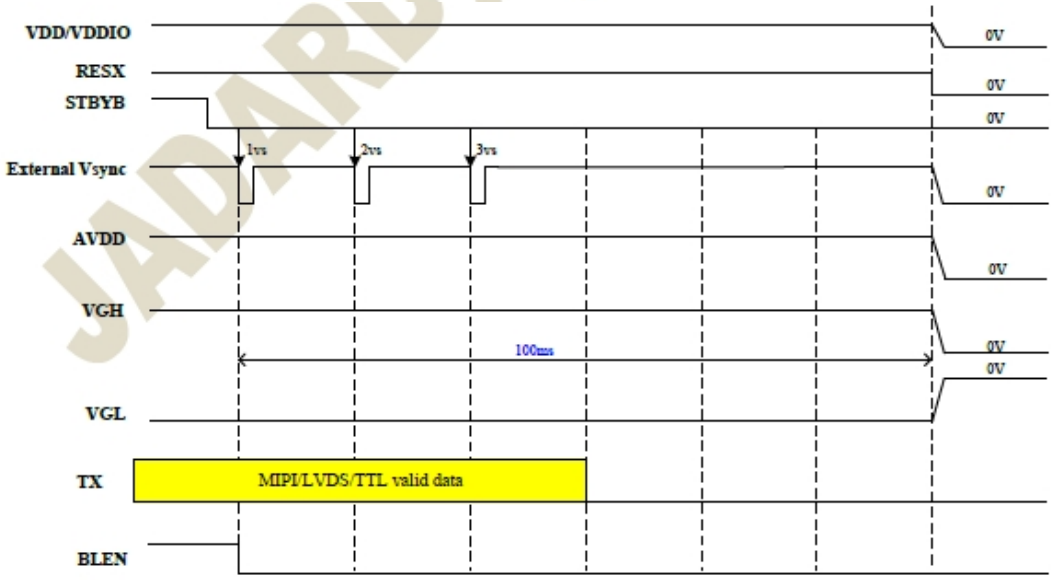


Figure 5.2: Power Off timing chart

6.0 ELECTRICAL CHARACTERISTICS

6.1 TFT LCD Module

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VDD	1.71	1.8	1.89	V
	VGH	18	19	20	V
	VGL	-8.5	-8	-7.5	V
	AVDD	9.4	10	11	V
VCOM	VCOM	3.0	(3.6)	3.8	V

Note:

(1) VGH is TFT Gate operating voltage.

(2) VGL is TFT Gate operating voltage. The low voltage level of VGH signal must be fluctuates with same phase as Vcom.

6.2 Back-Light Unit

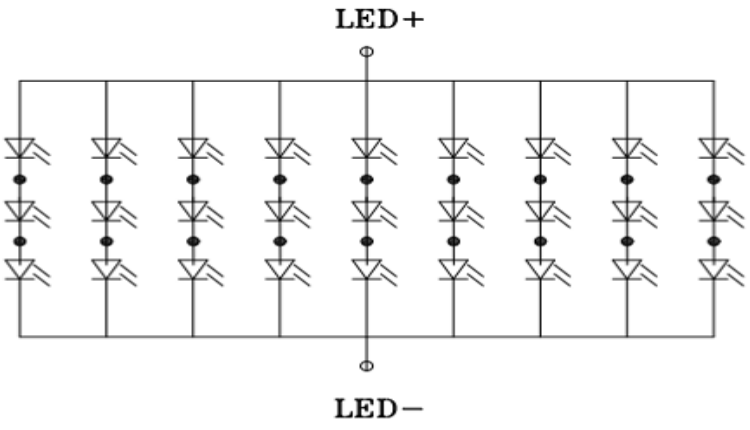
The backlight system is an edge-lighting type with 21 LED. The characteristics of the LED are shown in the following tables.

Item	Symbol	Min.	Typ.	Max.	Unit	Note
LED current	IL			180	mA	(2)
LED Voltage	VL			9.9	V	
Operating LED life time	Hr	15000	20000	--	Hour	(1)(2)

Note (1) LED life time (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25±3℃, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note (2) The "LED life time" is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL=140mA. The LED lifetime could be decreased if operating IL is larger than 140mA. The constant current driving method is suggested.

LED CIRCUIT DIAGRAM： 3 x 9 = 27LED



3串9并， 3*3. 3=9. 9V (MAX)，20*9=180mA

6.3 DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
MIPI Characteristics for High Speed Receiver					
Single-ended input low voltage	V_{ILHS}	-40	-	-	mV
Single-ended input high voltage	V_{IHHS}	-	-	460	mV
Common-mode voltage	V_{CMRXDC}	70	-	330	mV
Differential input impedance	Z_{ID}	80	100	120	ohm
HS transmit differential voltage($V_{OD}=V_{DP}-V_{DN}$)	$\|V_{OD}\|$	100	200	250	mV
MIPI Characteristics for Low Power Mode					
Pad signal voltage range	V_I	-50	-	1350	mV
Ground shift	V_{GNDSH}	-50	-	50	mV
Logic 0 input threshold	V_{IL}	0	-	550	mV
Logic 1 input threshold	V_{IH}	1000	-	1350	mV
Input hysteresis	V_{HYST}	25	-	-	mV
Output low level	V_{OL}	-50	-	50	mV
Output high level	V_{OH}	1.1	1.2	1.3	V
Output impedance of Low Power Transmitter	ZOLP	110			ohm
Logic 0 contention threshold	$V_{ILCD,MAX}$	-	-	200	mV
Logic 1 contention threshold	$V_{IHCD,MIN}$	450	-	-	mV
MIPI Digital Operating Current	$I_{VDDMIPI}$	-	15	20	mA
MIPI Digital Stand-by Current	I_{STMIPI}	-	-	250	uA

Note: MIPI Digital Operating and Stand-by Current is at RT 25℃ condition.

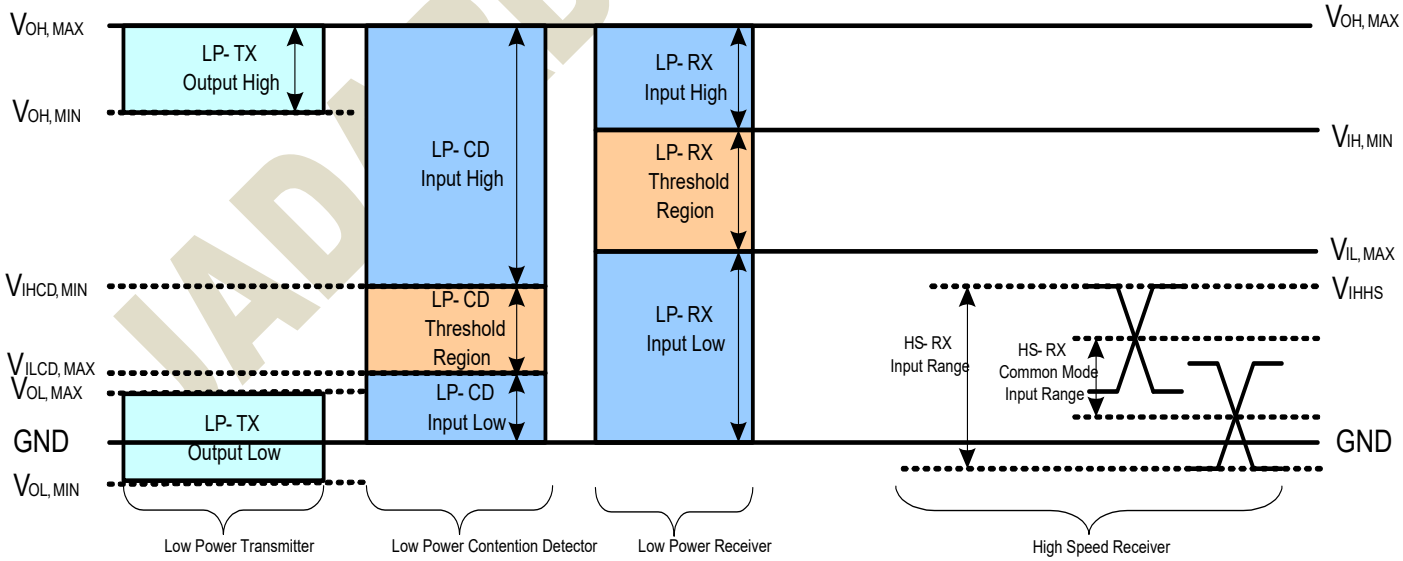


Figure 8.7: MIPI signaling and contention voltage levels

6.3.1 Absolute maximum ratings

Parameter	Symbol	Spec.			Unit	Note
		Min.	Typ.	Max.		
Supply power voltage	VDD	-0.30	-	3.96	V	
IO supply voltage	VDDIO	-0.30		3.96	V	
AVDD voltage	AVDD	-0.30	-	12	V	
VGH voltage	VGH	-0.30	-	VGL+32V	V	
VGL voltage	VGL	VGH-32V	-	0.30	V	
VMID voltage	VMID	-0.30	-	6.6	V	
VCOM voltage	VCOM_OP	-0.30	-	5.43	V	
VOTP **(OTP power)**	VOTP	-	-	9	V	
Operating Temperature	TOPR	-20	-	+85	℃	
Storage temperature	TSTG	-55	-	125	℃	

6.3.2Typical operating condition

Parameter	Symbol	Spec.			Unit	Note
		Min.	Typ.	Max.		
Supply power voltage	VDD	1.8	3.3	3.6	V	TTL mode condition
I/O power voltage	VDDIO	1.8	3.3	3.6	V	
Supply power voltage	VDD	1.8	3.3	3.6	V	LVDS mode condition
I/O power voltage	VDDIO	1.8	3.3	3.6	V	
Supply power voltage	VDD	1.71	1.8	2.0	V	MIPI mode condition
I/O power voltage	VDDIO	1.71	1.8	2.0	V	
AVDD voltage	AVDD	9	10	11	V	
VGH voltage	VGH	15	18	20	V	
VGL voltage	VGL	-12	-8	-6	V	
VMID voltage	VMID	4.5	5	5.5	V	
VMID_OP voltage	VMID_OP	4.5	5	5.5	V	
VQHO voltage	VQHO	-	0.7AVDD	-	V	
VQLO voltage	VQLO	-	0.3AVDD	-	V	
VCOM voltage	VCOM_OP	2.7	3.8	4.94	V	
VOTP	VOTP	7.5	7.75	8	V	

6.3.3 VDD power on slew time

Be sure that VDD input can't result automatically in power on sequence.

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max	
VDD power on skew time	T_{POR}	From 0V to 1.35V	0.05	-	5	ms

6.3.4 Timing requirements for RESX

When RESX of the reset pin equals to Low, it will be in the condition of reset.
When it is in the condition of reset, it will make the device recover the initial set.

However, in order to avoid the reset noise cause reset, there is a mechanism to judge about whether the reset is needed or not.

The closed interval of Low can be shown as the following.

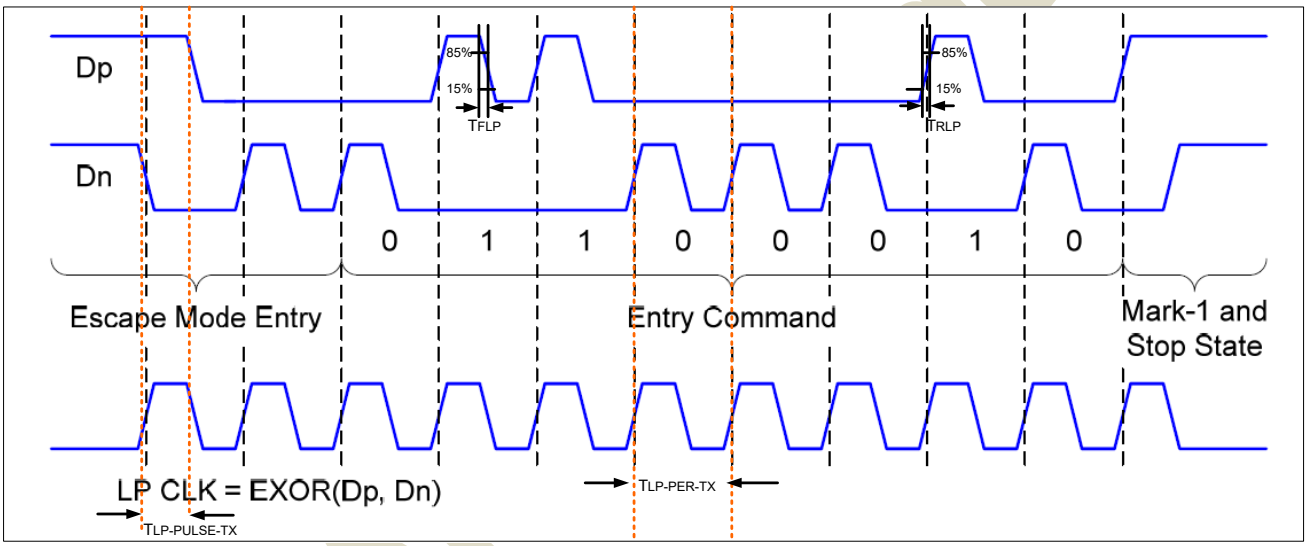
(Test condition: VDD=1.8V~3.3V, VSS=0V, T_A=-20 ~+85)

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max	
Reset low pulse width	Trst		6	-	-	μs

6.5 AC Characteristics

6.5.1 LP Transmitter AC Specification

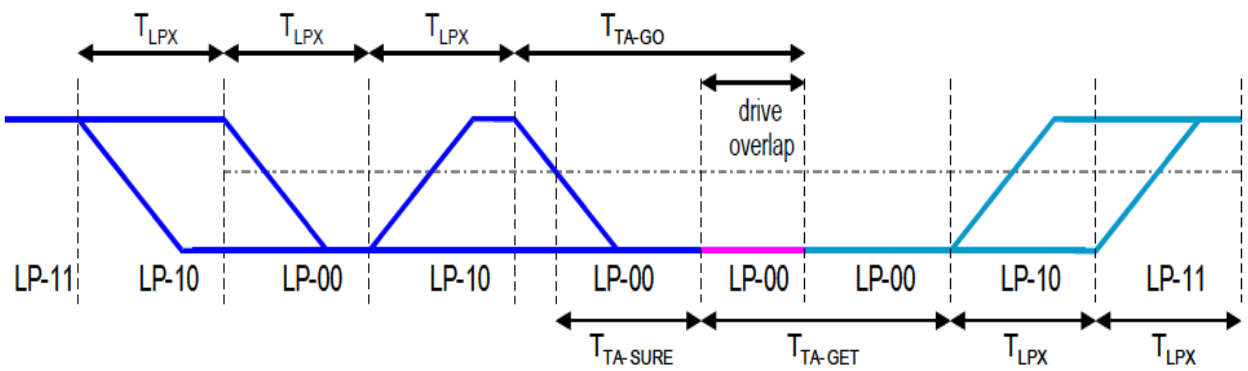
Parameter		Symbol	Min	Typ	Max	Units	Notes
15%~85% rising time and falling time		T_{RLP} /T_{FLP}	-	-	25	ns	-
30%~85% rising time and falling time		T_{REOT}	-	-	35	ns	-
Pulse width of LP exclusive-OR clock	First LP EXOR clock pulse after STOP state or Last pulse before stop state	$T_{LP-PULSE-TX}$	100	-	-	ns	-
	All other pulses		100	-	-	ns	-
Period of the LP EXOR clock(LP Speed)		$T_{LP-PER-TX}$	200	-	-	ns	-
Slew Rate @CLOAD =0pF		δ V/δ t_{SR}	20	-	500	mV/ns	-
Slew Rate @CLOAD =5pF			20	-	200	mV/ns	-
Slew Rate @CLOAD =20pF			20	-	150	mV/ns	-
Slew Rate @CLOAD =70pF			20	-	100	mV/ns	-
Load Capacitance		T_{RLP}	-	-	70	pF	-



6.5.2 Turnaround Procedure

●Turnaround Procedure Operation Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
Length of any Low-Power state period	T_{LPX}	100	-	-	ns
Time-out before new TX side start driving	$T_{TA-Sure}$	T_{LPX}	-	2T_{LPX}	ns
Time to drive LP-00 by new TX	T_{TA-GET}	-	5T_{LPX}	-	ns
Time to drive LP-00 after Turnaround Request	T_{TA-GO}	-	4T_{LPX}	-	ns



6.5.3 High Speed Clock and Data Transmission Procedure

Parameter	Descript	Spec.			Unit
		Min.	Typ.	Max.	
T_{REOT}	30%-85% rise time and fall time	-	-	35	ns
$T_{CLK-MISS}$	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.	-	-	60	ns
$T_{CLK-POST}$*1	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	60 ns + 52*UI	-		ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8	-		UI
$T_{CLK-SETTLE}$	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of $T_{CLK-PRE}$.	95	-	300	ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach VTERM-EN	-	38	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of $T_{HSPREPARE}$.	85 ns + 6*UI	-	145 ns + 10*UI	ns
T_{EOT}	Time from start of $T_{HS-TRAIL}$ or $T_{CLK-TRAIL}$ period to start of LP-11 state	-	-	105ns+n*12*UI	-
$T_{HS-EXIT}$(1)	time to drive LP-11 after HS burst	100	-	-	ns
$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40ns + 4*UI	-	85ns+6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + Time to drive HS-0 before the Sync sequence	145ns + 10*UI	-	-	ns
$T_{HS-SKIP}$	Time-out at RX to ignore transition period of EoT	40	-	55ns+4*UI	ns
$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60 + 4*UI	-	-	ns
T_{LPX}	Length of any Low-Power state period	100	-	-	ns
Ratio T_{LPX}	Ratio of $T_{LPX(MASTER)}/T_{LPS(SLAVE)}$ between Master and Slave side	2/3	-	3/2	-
T_{TA-GET}	Time to drive LP-00 by new TX	$5*T_{LPX}$			ns
T_{TA-GO}	Time to drive LP-00 after Turnaround Request	$4*T_{LPX}$			ns
$T_{TA-SURE}$	Time-out before new TX side starts driving	T_{LPX}	-	$2*T_{LPX}$	ns

Note: (1) For $T_{CLK-POST}$ example:
$T_{CLK-POST}$ min value =164UI when MIPI max frequency per lane = 0.5Gbps.
$T_{CLK-POST}$ min value =112UI when MIPI max frequency per lane = 1Gbps
(2) For T_{EOT}:
When n = 1 for Forward-direction HS mode and n=4 for Reverse-direction HS mode.

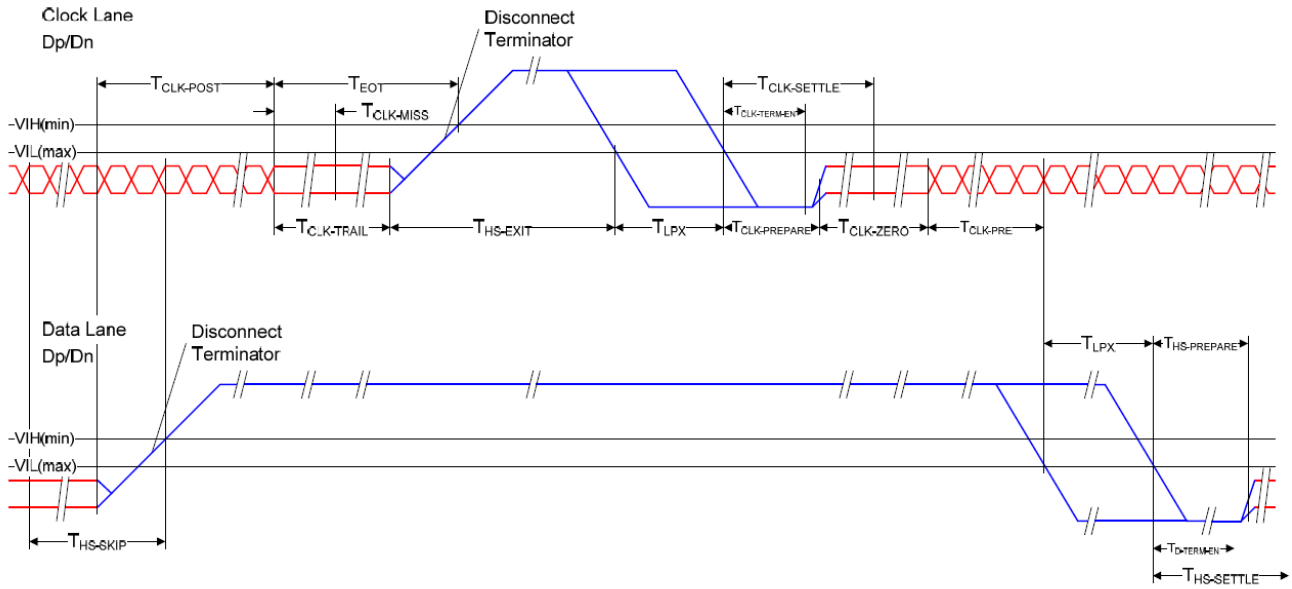


Figure 8.8: Switching the clock lane between clock transmission and low-power mode

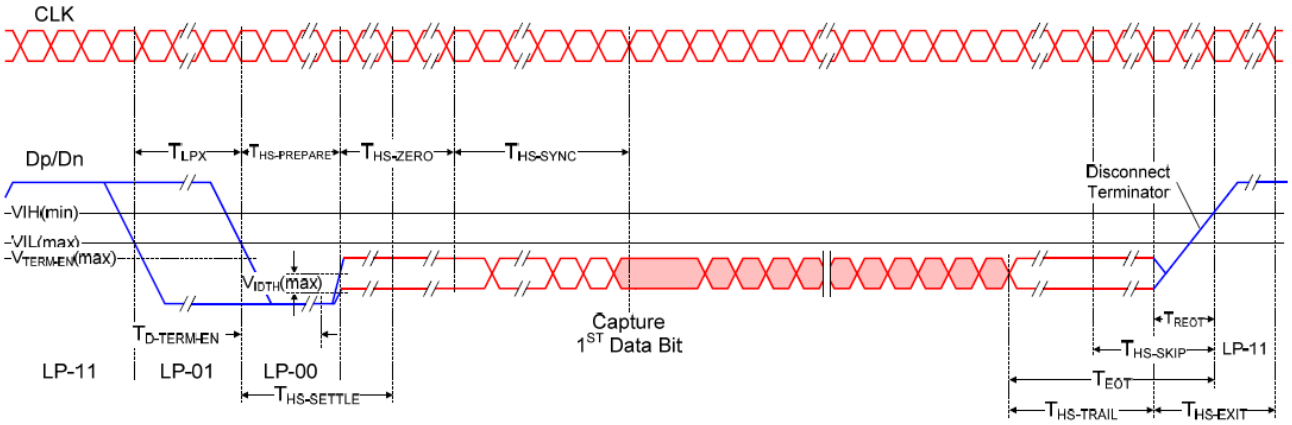
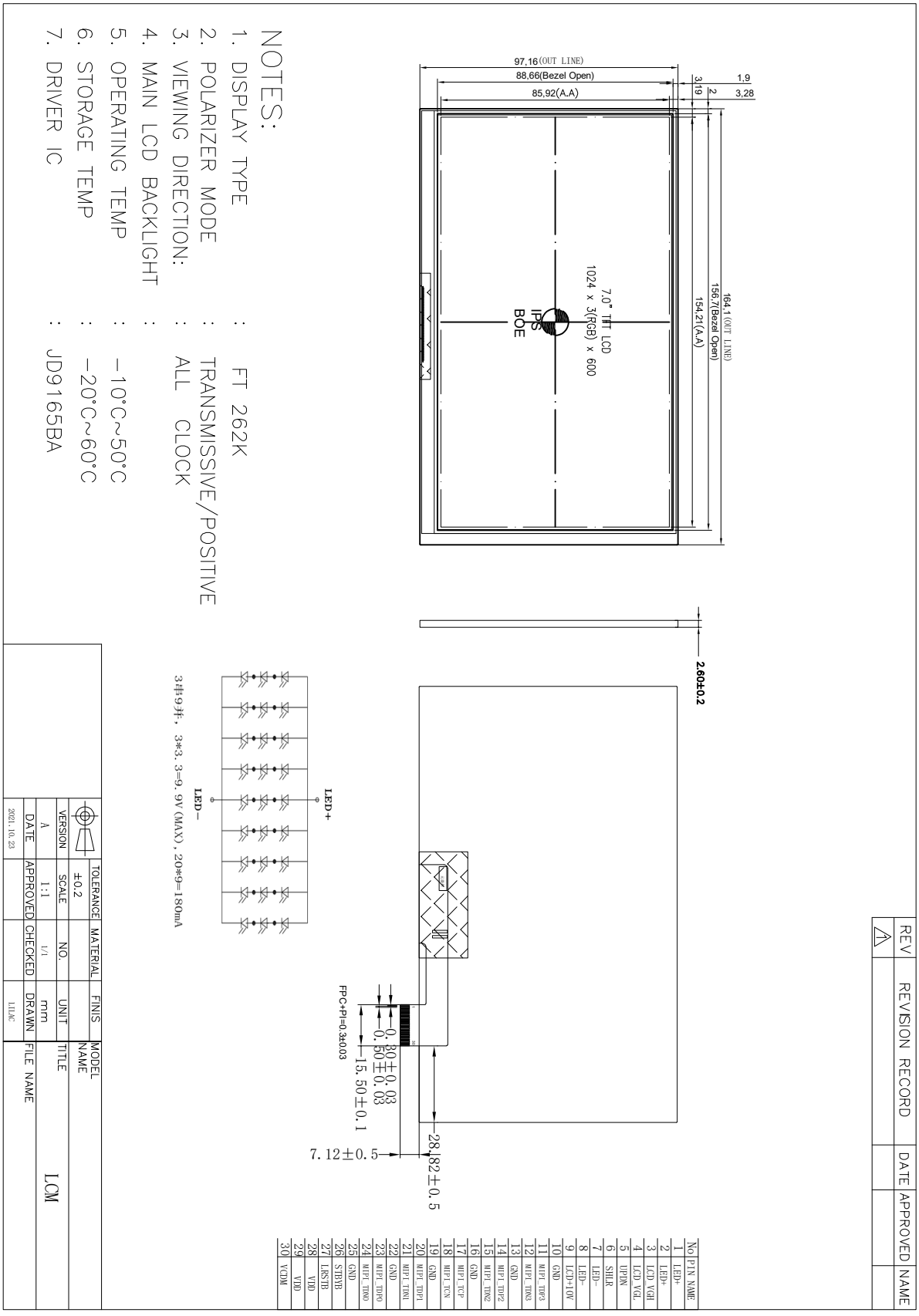


Figure 8.9: Timing of high-speed data transmission in bursts

7.0 Reliability test items

Test Item	Test Conditions	Notes
High temperature Operation	Ta= +50℃, 96hrs	
Low temperature Operation	Ta= -10℃, 96hrs	
High Temperature Storage	Ta= +60℃, 96hrs	
Low Temperature Storage	Ta= -20℃, 96hrs	
Humidity Test	50℃±3℃, 90%±3%RH, 24H;	
Thermal Shock Test	-20℃/0.5H～+60℃/0.5H (24 cycle)	
Vibration Test(Packing)	Sine Wave 1.04G, 10Hz~55Hz~10Hz, XYZ 30min/each direction	
ESD test	±2KV, Human Body Mode, 150pF/330Ω; ±8KV, Air Mode, 150pF/330Ω;	

8.0 OUTLINE DIMENSION



9.0 General precaution

9.1 Use Restriction

This product is not authorized for use in life supporting systems, aircraft navigation control systems, military systems and any other application where performance failure could be life threatening or otherwise catastrophic.

9.2 Disassembling or Modification

Do not disassemble or modify the module. It may damage sensitive parts inside LCD module, and may cause scratches or dust on the display. We does not warrant the module, if customers disassemble or modify the module.

9.3 Breakage of LCD Panel

9.3.1.If LCD panel is broken and liquid crystal spills out, do not ingest or inhale liquid crystal, and do not contact liquid crystal with skin.

9.3.2. If liquid crystal contacts mouth or eyes, rinse out with water immediately.

9.3.3. If liquid crystal contacts skin or cloths, wash it off immediately with alcohol and rinse thoroughly with water.

9.3.4. Handle carefully with chips of glass that may cause injury, when the glass is broken.

9.4 Electric Shock

9.4.1. Disconnect power supply before handling LCD module.

9.4.2. Do not pull or fold the LED cable.

9.4.3. Do not touch the parts inside LCD modules and the fluorescent LED's connector or cables in order to prevent electric shock.

9.5 Absolute Maximum Ratings and Power Protection Circuit

9.5.1. Do not exceed the absolute maximum rating values, such as the supply voltage variation, input voltage variation, variation in parts' parameters, environmental temperature, etc., otherwise LCD module may be damaged.

8.5.2. Please do not leave LCD module in the environment of high humidity and high temperature for a long time.

8.5.3. It's recommended to employ protection circuit for power supply.

9.6 Operation

9.6.1 Do not touch, push or rub the polarizer with anything harder than HB pencil lead.

9.6.2 Use finger stalls of soft gloves in order to keep clean display quality, when persons handle the LCD module for incoming inspection or assembly.

9.6.3 When the surface is dusty, please wipe gently with absorbent cotton or other soft material.

9.6.4 Wipe off saliva or water drops as soon as possible. If saliva or water drops contact with polarizer for a long time, they may causes deformation or color fading.

9.6.5 When cleaning the adhesives, please use absorbent cotton wetted with a little petroleum benzine or other adequate solvent.

9.7 Mechanism

Please mount LCD module by using mouting holes arranged in four corners tightly.

9.8 Static Electricity

9.8.1 Protection film must remove very slowly from the surface of LCD module to prevent from electrostatic occurrence.

9.8.2. Because LCD module use CMOS-IC on circuit board and TFT-LCD panel, it is very weak to electrostatic discharge. Please be careful with electrostatic discharge. Persons who handle the module should be grounded through adequate methods.

9.9 Strong Light Exposure

The module shall not be exposed under strong light such as direct sunlight. Otherwise, display characteristics may be changed.

9.10 Disposal

When disposing LCD module, obey the local environmental regulations.