PRODUCT SPECIFICATION FOR LCD MODULE

Revision: 1.0

Model No: LS0144T10-M-V1

Module Type: COG+FPC+B/L

APPROVED SIGNATURE

■ Approved Product Specification only

□ Approved Product Specification and Samples

Prepared By	Checked By	Approved By

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1. General Description

LS0144T10-M-V1 is a transmissive type a-Si TFT-LCD (amorphous silicon thin film transistor liquid crystal display) module, which is composed of a TFT-LCD panel, a driver circuit and a backlight unit. The panel size is 1.44 inch and the resolution is 128(RGB)*128, the panel can display up to 262k colors.

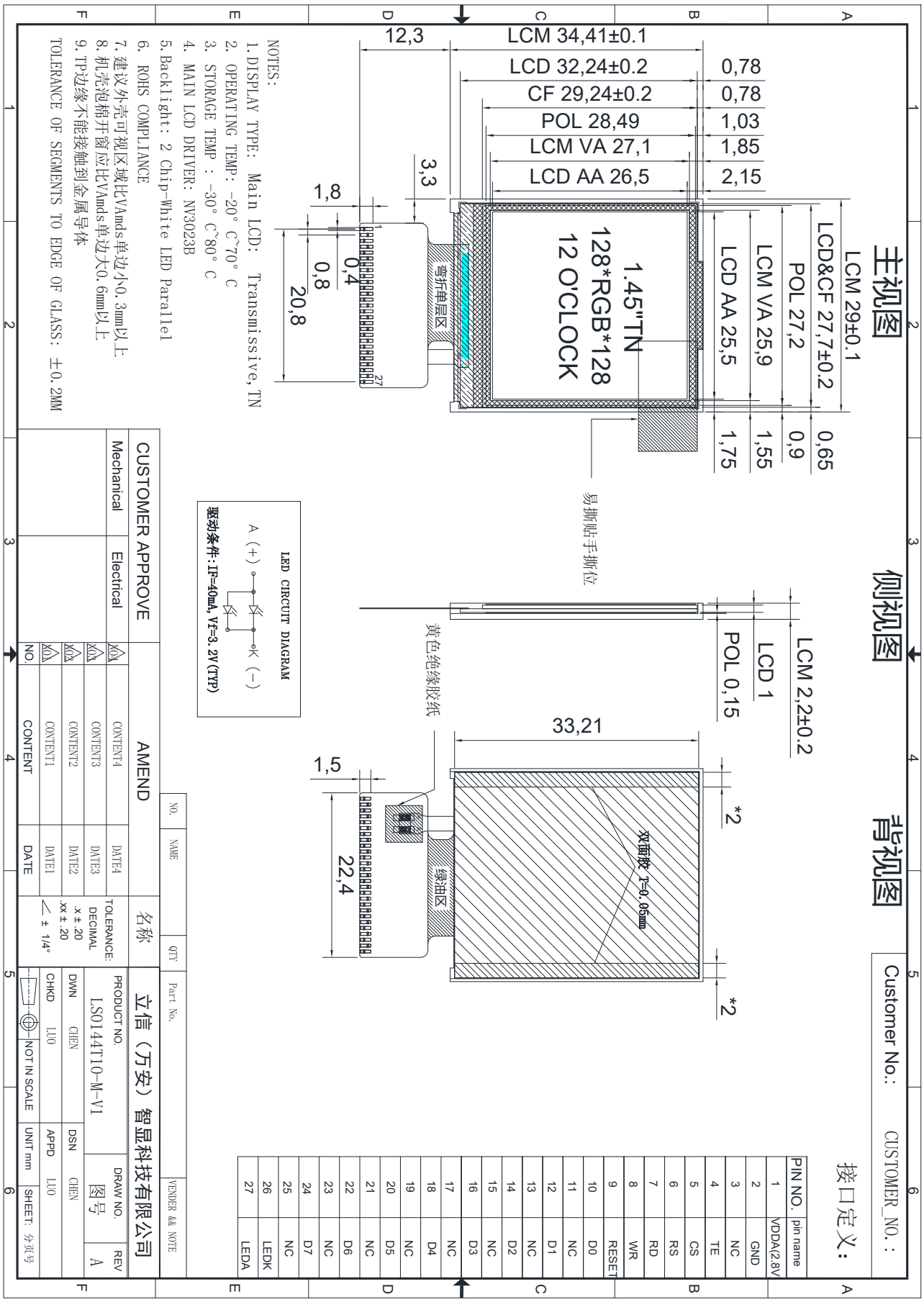
2. Physical Features

Display Mode	TFT-LCD Module
	Active matrix TFT, Transmissive type
Display Format	Graphic 128(RGB)×128 Dot-matrix
Input Data	8bit 8080
Viewing Direction （Grayscale Inversion）	TN
Drive	NV3023B

3. Mechanical Specification

Item	Specification	Unit
Module size (H×V×D)	29.00 ×34.41 ×2.2	mm
Number of dots	128(RGB) ×128	pixel
Active area (H×V)	25.5×26.5	mm

4. Outline Dimension



5. Absolute Maximum Ratings

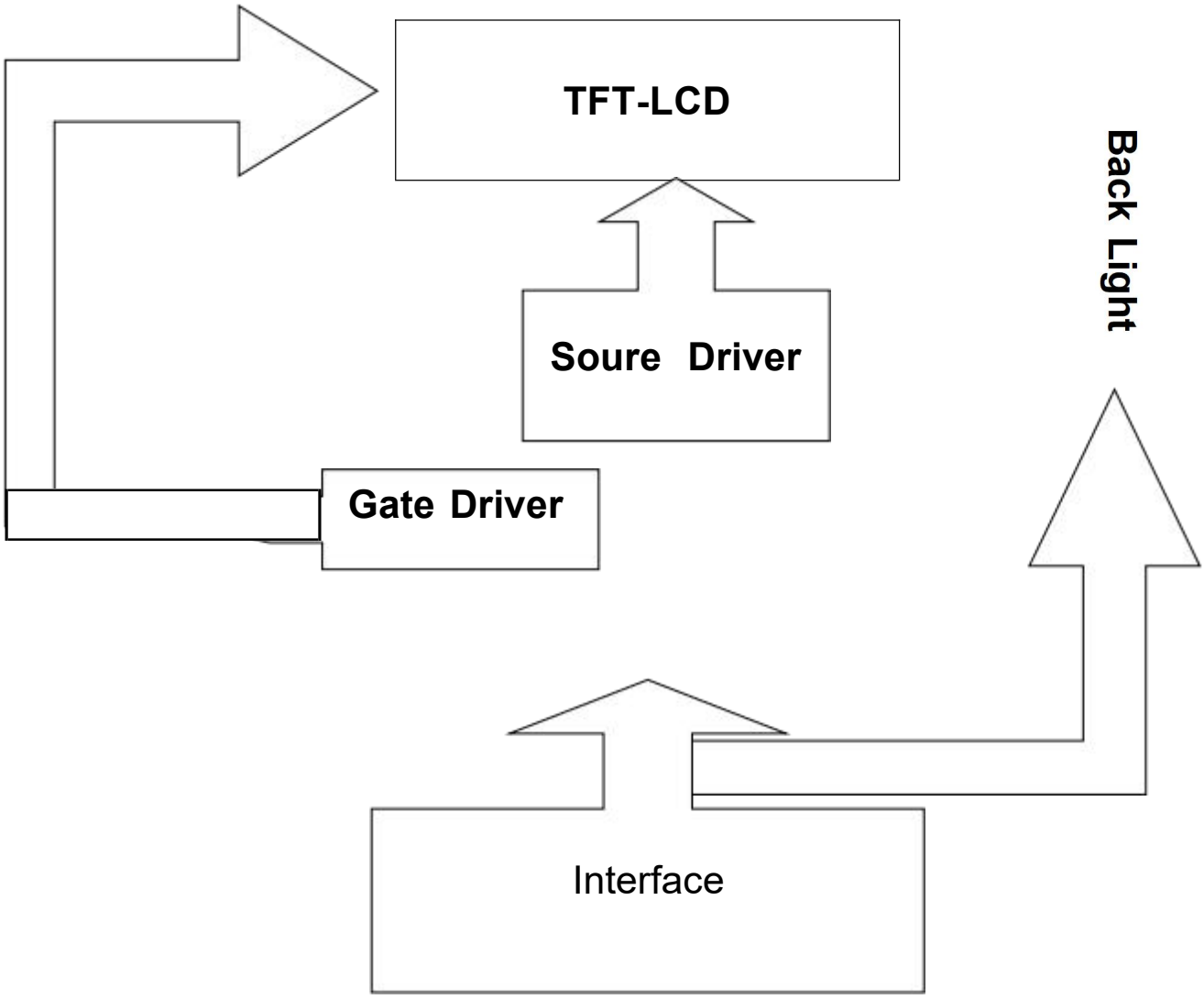
Item	Symbol	Min	Max	Unit	Remark
Supply voltage	VCC	-0.3	4.8	V	Note1 Note2
Supply voltage	IOVCC	-0.3	3.6	V	
Operating temperature	TOPR	-20	70	℃	
Storage temperature	TSTR	-30	80	℃	

6. Electrical Characteristics

Item		Symbol	Rating			Unit	Remark
			Min	Typ	Max		
Supply voltage		VCC	2.5	2.75	4.8	V	Note1
Supply voltage		IOVCC	1.65	1.8	3.6	V	
Input Voltage	L level	VIL	0	---	0.3*IOVCC	V	
	H level	VIH	0.7*IOVCC	---	IOVCC	V	

7. Module Function Description

7-1. Block Diagram Of LCM



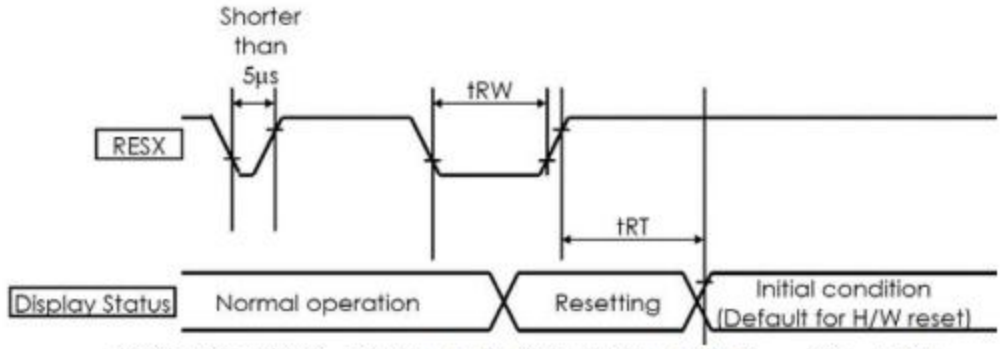
7-2. Pin Description

PIN NO.	Symbol	I/O	Description
1	VDD	P	Power supply
2	GND	P	Ground
3	NC		
4	TE	O	Tearing effect output pin to synchronize MCU to frame writing
5	CS	I	Chip Select Pin（“Low Active”） Pull down when chip accessable
6	RS	I	Reuse Pin according parallel and serial interface: MCU Interface: Distinguish Data (‘1’) or Command (‘0’). SPI Interface: Used as ‘SCL’ clock pin. If not used, please connect this pin to VSS.
7	RD	I	8080-parallel interface: used as ‘Read’ enable.
8	WR	I	8080-parallel interface, used as write enable. SPI 4-wire interface, used as D/CX. 2 Data Line SPI used as data input.
9	RESET	I	
10	D0	I	data bus
11	NC		
12	D1	I	data bus
13	NC		
14	D2	I	data bus
15	NC		
16	D3	I	data bus
17	NC		
18	D4	I	data bus
19	NC		
20	D5	I	data bus
21	NC		
22	D6	I	data bus
23	NC		
24	D7	I	data bus

25	NC		
26	LEDK	P	Power for LED backlight cathode
27	LEDA	P	Power for LED backlight anode

7-3 Timing Characteristics

10.2. Reset Timing



(VSS=0V, IOVCC=1.65V to 3.6V, VCI=2.5V to 3.6V, Ta = -30 to 85℃)

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
tRW	Valid Reset low pulse width	RESX	10	-	-	-	us
tRT	Valid Reset Complete width	RESX	-	-	5	When reset applied during Sleep in mode	ms
		RESX	-	-	120	When reset applied during Sleep out mode	ms

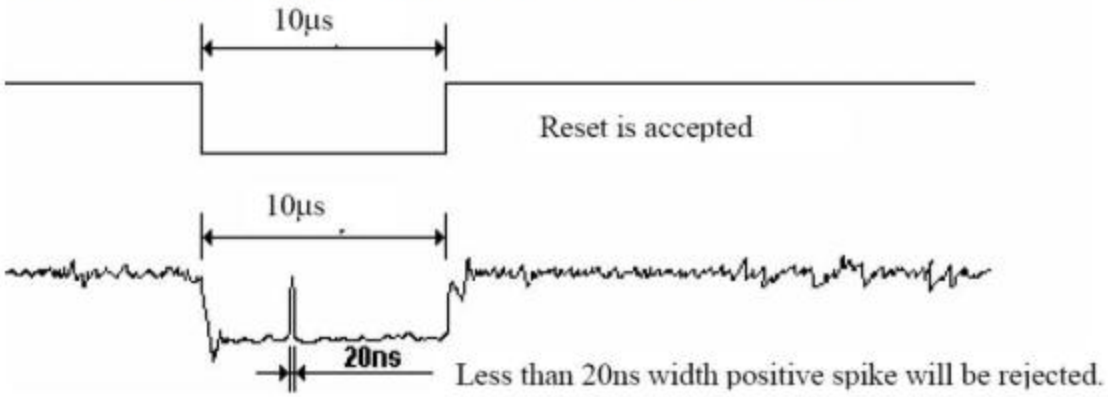
Note:

1> Spike due to an electrostatic discharge on RESX line does not cause system reset according to the table below.

RESX Pulse	Action
Shorten than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts(It depends on voltage and temperature condition)

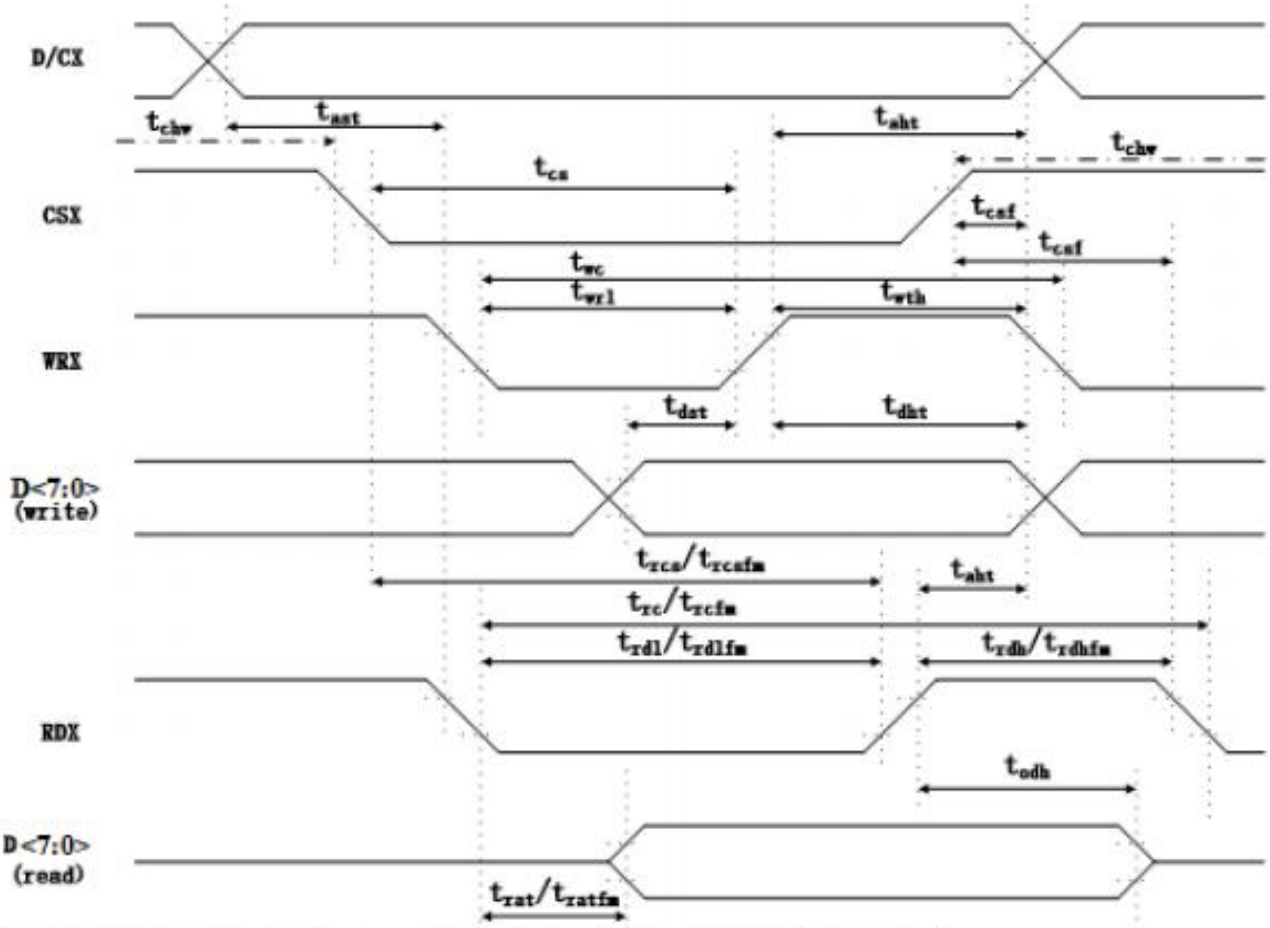
2> During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In mode) and then return to Default condition for Hardware Reset.

3> Spike Rejection also applies during a valid reset pulse as shown below:



4> It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

15.3.1 Parallel MCU 8-bit BUS



Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Table 15.3.1 AC characteristics of parallel MCU I/F in asynchronous mode

Signal	Symbol	Parameter	MIN	MAX	UNIT	Description
D/CX	TAST	Address Setup Time	0		ns	
	THAT	Address Hold Time (W/R)	10		ns	
CSX	TCHW	"S" "H" Pulse Width	0		ns	
	TCS	Chip Select Setup Time(W)	10		ns	
	TRCS	Chip Select Setup Time (Read ID)	45		ns	
	TRCSFM	Chip Select Setup Time (Read FM)	355		ns	
	TCSF	Chip Select Wait Time (W/R)	10		ns	
WRX	TWC	Write Cycle	80		ns	
	TWRH	Control Pulse H Duration	40		ns	
	TWRL	Control Pulse L Duration	40		ns	
RDX	TRC	Read Cycle(ID)	160		ns	When Read ID
	TRDH	Control Pulse H Duration(ID)	90		ns	
	TRDL	Control Pulse L Duration(ID)	45		ns	

RDX	TRCFM	Read Cycle(FM)	450		ns	When Read From Frame Memory
	TRDHFM	Control Pulse H Duration(FM)	90		ns	
	TRDLFM	Control Pulse L Duration(FM)	355		ns	
D<7:0>	TDST	Data Setup Time	10		ns	CLmax=30pF Clmin=8pF
	TDHT	Data Hold Time	10		ns	
	TRAT	Read Access Time(ID)		40	ns	
	TRATFM	Read Access Time(FM)		340	ns	
	TODH	Output Disable Time	20	80	ns	

Note 1: IOVCC 1.65 to 3.6V, VCI=2.6 to 3.6V, AGND=GND=0V, Ta=-30 to 70 °C (to +85℃ no damage)
Note 2: This input signal rise time and fall time (tr, tf) is specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of IOVCC for input signals

8. Electro-Optical Characteristics

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time		Tr +Tf	θx = θy =0	---	25	30	ms	Note 1
Contrast Ratio		CR		300	600	---	---	Note 2
Transmittance		T%		3.9	5.5	---	%	
Color Chromaticity (CIE1931)	White	W x	θx = θy =0	---	0.301	---	---	
		W y		---	0.327	---	---	
Viewing angle	θ_T		CR > 10	---	70	---	Deg.	Note 3
	θ_B			---	60	---		
	θ_L			---	75	---		
	θ_R			---	75	---		

FIG. 2 The definition of Response Time

The response time is defined as the following figure and shall be measured by switching the input signal for "black" and "white". This definition is valid for a normally black display. For a normally white display the opposite definition applies.

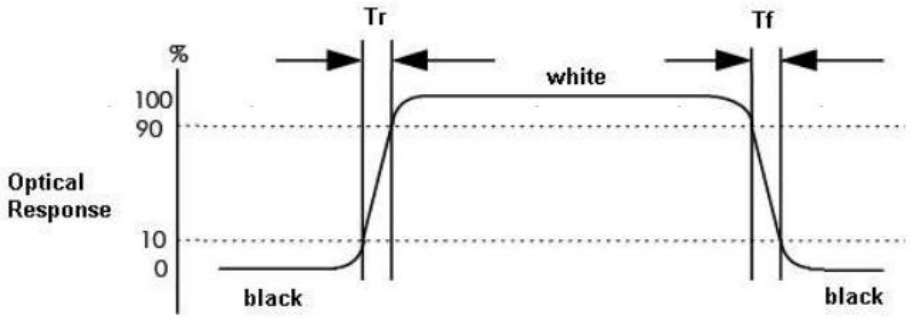
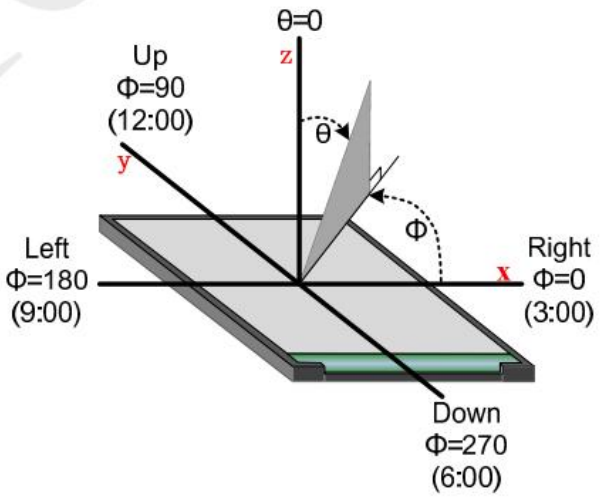
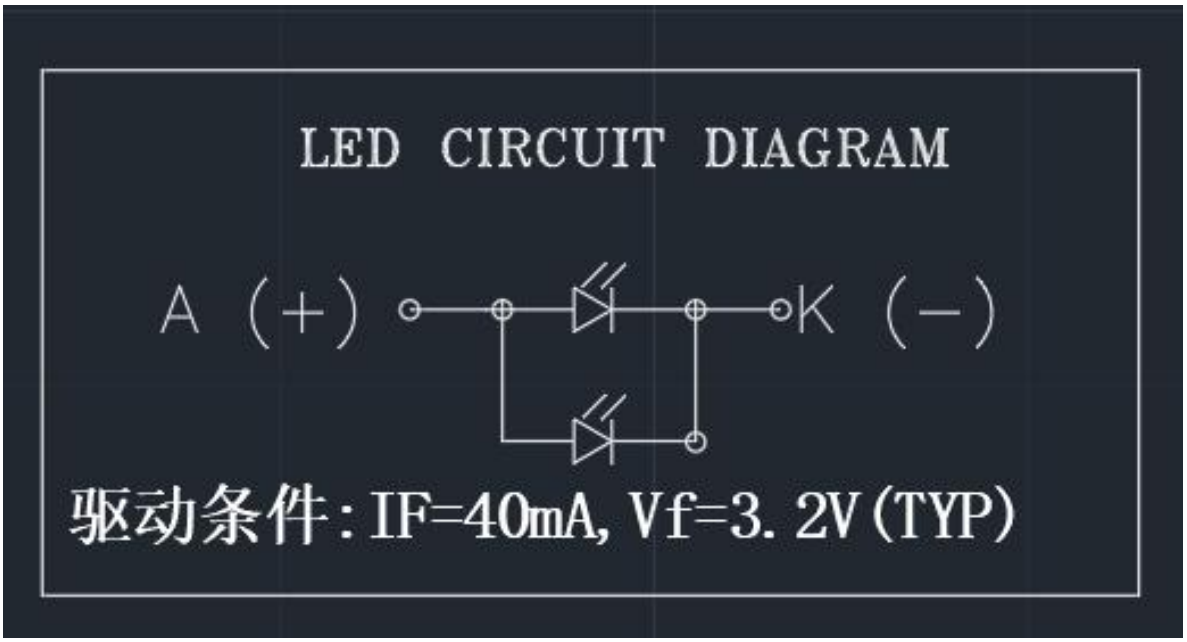


FIG. 3 The definition of viewing angle



Note(4) Backlight circuit



9.Records Of Version

Version	Revise Date	Page	Content
00	2026-1-17	ALL	New released