PRODUCT SPECIFICATION FOR LCD MODULE

Revision: 1.0

Model No: LSC101I43-MP-V1

Module Type: COG+FPC+B/L+LENS

APPROVED SIGNATURE

■ Approved Product Specification only

□ Approved Product Specification and Samples

Prepared By	Checked By	Approved By

REVISION STATUS

Version	Revise Date	Page	Content	Modified by
V1.0	2025.04.02	-	First Issued.	
V1.1	2025.10.25	5	修改模组暗码喷码内容	

TABLE OF CONTENTS

1. GENERAL DESCRIPTION

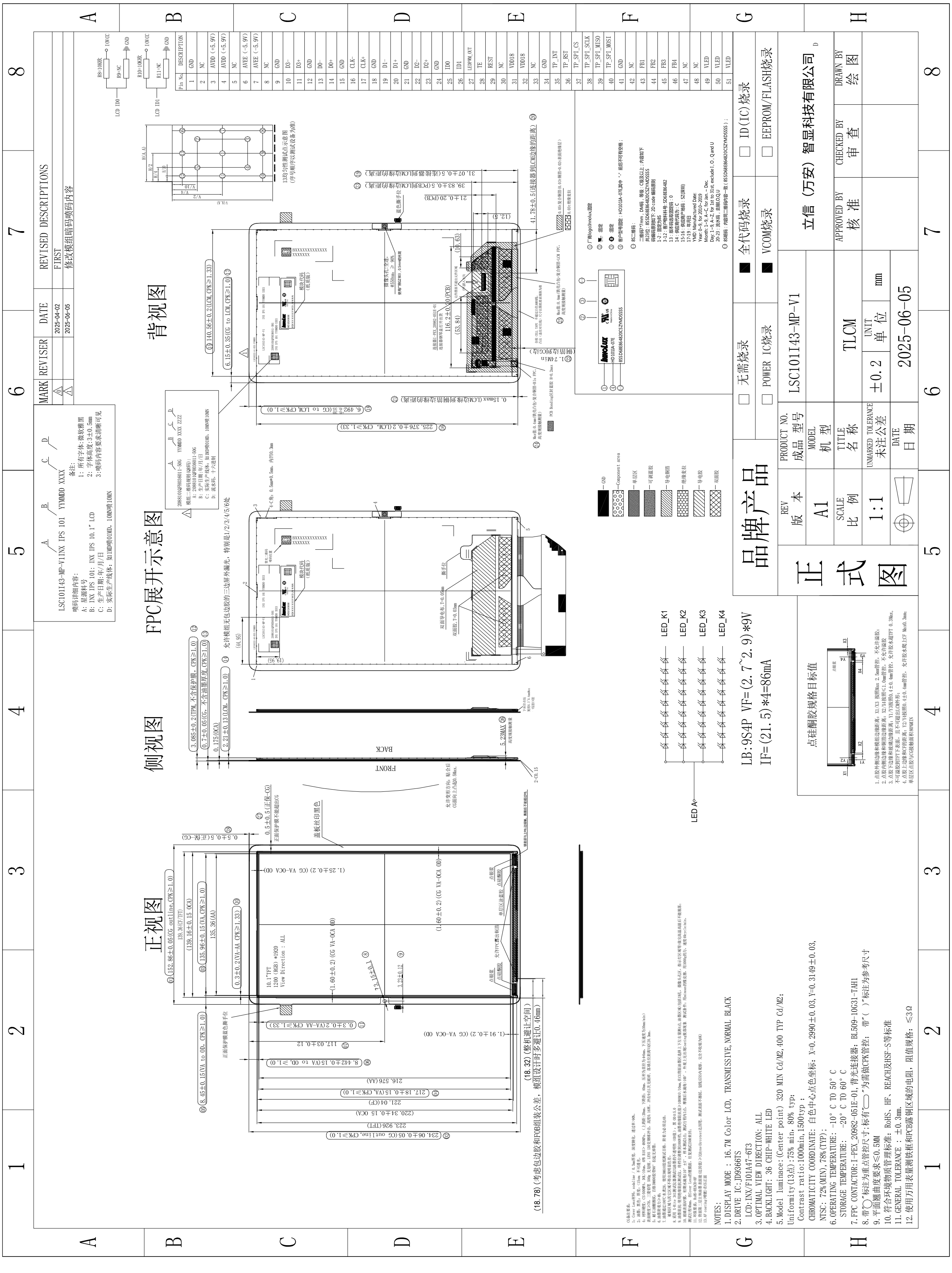
1.1 DESCRIPTION

This LCM is a color active matrix thin film transistor (TFT) IPS liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. It is composed of a TFT LCD panel, Driver IC, FPC and Backlight, This TFT LCD has a 10.1-inch diagonally measured active display area with high resolution (1200 horizontal by 1920 vertical pixel array).

1.2 FEATURES:

No.	Item	Specification	Unit
1	Panel Size	10.1”	inch
2	Number of Pixels	1200×RGB×1920	pixels
3	Active Area	135.36(H) × 216.576(V)	mm
4	Pixel Pitch	37.6(H) × 112.8(V)	um
5	TLCM Outline Dimension	152.86(H) x234.06(V) x 3.085 (T)	mm
6	Number of Colors	16.7M	-
7	Display Mode	Transmission mode, normally black	-
8	Viewing Direction	Full viewing	-
9	Display Format	RGB-stripe	-
10	Driving Inversion	Column inversion	-
11	Interface	4L-MIPI	-
12	Backlight	White lED	-
13	Weight	198±10	g
14	Driver IC	JD9366TS	-
15	Touch FW	V05	-

TLCM:


正视图
侧视图
背视图
FPC展开示意图
LB:9S4P VF=(2.7~2.9)*9V
IF=(21.5)*4=86mA
品牌产品
正式图
LSC101I43-MP-V1
TLCM
2025-06-05
立信（万安）智显科技有限公司

3. PIN DESCRIPTION

3.1 51PIN DESCRIPTION

Pin No.	Symbol	Type	Description
1	GND		Ground
2	NC		No connect
3	AVDD		Positive input power
4	AVDD		Positive input power
5	NC		No connect
6	AVEE		Negative input power
7	AVEE		Negative input power
8	NC		No connect
9	GND		Ground
10	D3-		Negative MIPI differential data input
11	D3+		Positive MIPI differential data input
12	GND		Ground
13	D0-		Negative MIPI differential data input
14	D0+		Positive MIPI differential data input
15	GND	-	Ground
16	CLK-		Negative MIPI differential clock input
17	CLK+		Positive MIPI differential clock input
18	GND		Ground
19	D1-		Negative MIPI differential data input
20	D1+		Positive MIPI differential data input
21	GND		Ground
22	D2-		Negative MIPI differential data input
23	D2+		Positive MIPI differential data input
24	GND		Ground
25	ID0		ID 10K to VDD18
26	ID1		ID 10K to VDD18
27	LEDPWM-OUT		PWM Signal
28	TE		M-Tearing Effect) output pin.
29	REST		LCD RESET PIN
30	NC		No connect
31	VDD18		Logic power input(1.8V)

32	VDD18		Logic power input(1.8V)
33	NC		No connect
34	GND		Ground
35	TP_INT		TP INT PIN
36	TP_RST		TP RST PIN
37	TP_SPI_CS		SPI slave chip select input
38	TP_SPI_SCLK		SPI slave clock input
39	TP_SPI_MISO		SPI DATA INPUT PIN (MISO)
40	TP_SPI_MOSI		SPI DATA OUTPUT PIN PIN (MOSI)
41	GND		Ground
42	NC		No connect
43	FB1		Power for LED backlight (Cathode)
44	FB2		Power for LED backlight (Cathode)
45	FB3		Power for LED backlight (Cathode)
46	FB4		Power for LED backlight (Cathode)
47	NC		No connect
48	NC		No connect
49	VLED		Power for LED backlight (Anode)
50	VLED		Power for LED backlight (Anode)
51	VLED		Power for LED backlight (Anode)

4. ELECTRICAL CHARACTERISTICS

4.1 ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit
Digital Supply Voltage	VDDI8	-0.3	2.1	V
Negative input power	AVEE	-6.6	0.3	V
Positive input power	AVDD	-0.3	6.6	V

4.2 TFT LCD MODULE

4.2.1 OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Digital Power Supply Voltage	VDD18	1.7	1.8	1.9	V
Negative Analog Power Supply Voltage	AVEE	-6.1	-5.9	-5.7	V
Positive Analog Power Supply Voltage	AVDD	5.7	5.9	6.1	V

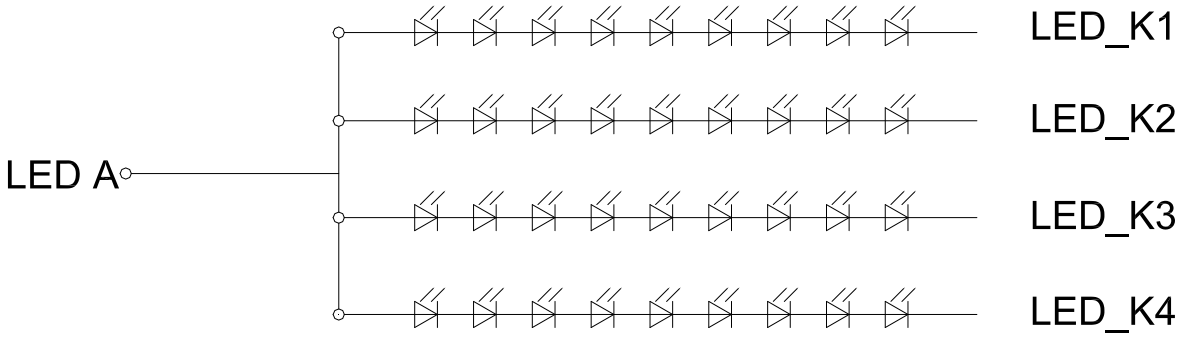
4.3 CURRENT CONSUMPTION

Item	Symbol	Condition	Values			Unit
			Min.	Typ.	Max.	
Digital Current	IVDDI	VDD18 = 1.8 @white 60HZ pattern	35	50	65	mA
Negative input power Current	IAVDD	AVDD=5.8 @white 60HZ pattern	17.5	25	32.5	mA
Positive input power Current	IAVEE	AVEE=-5.8 @white 60HZ pattern	13.3	19	24.7	mA

4.4 BACK LIGHT UNIT

Ta=25℃

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
LED current	ILED	-	86	-	mA	Total LED
Forward voltage	VF	-	25.2	-	V	IF=86 mA
Reverse current	IR	-	50	-	μA	VR=5V,1LED
Power dissipation	Pd	2167.2			mW	Total LED
Peak forward current	IFP	100			mA	1LED
Reverse Voltage	VR	5			V	1LED



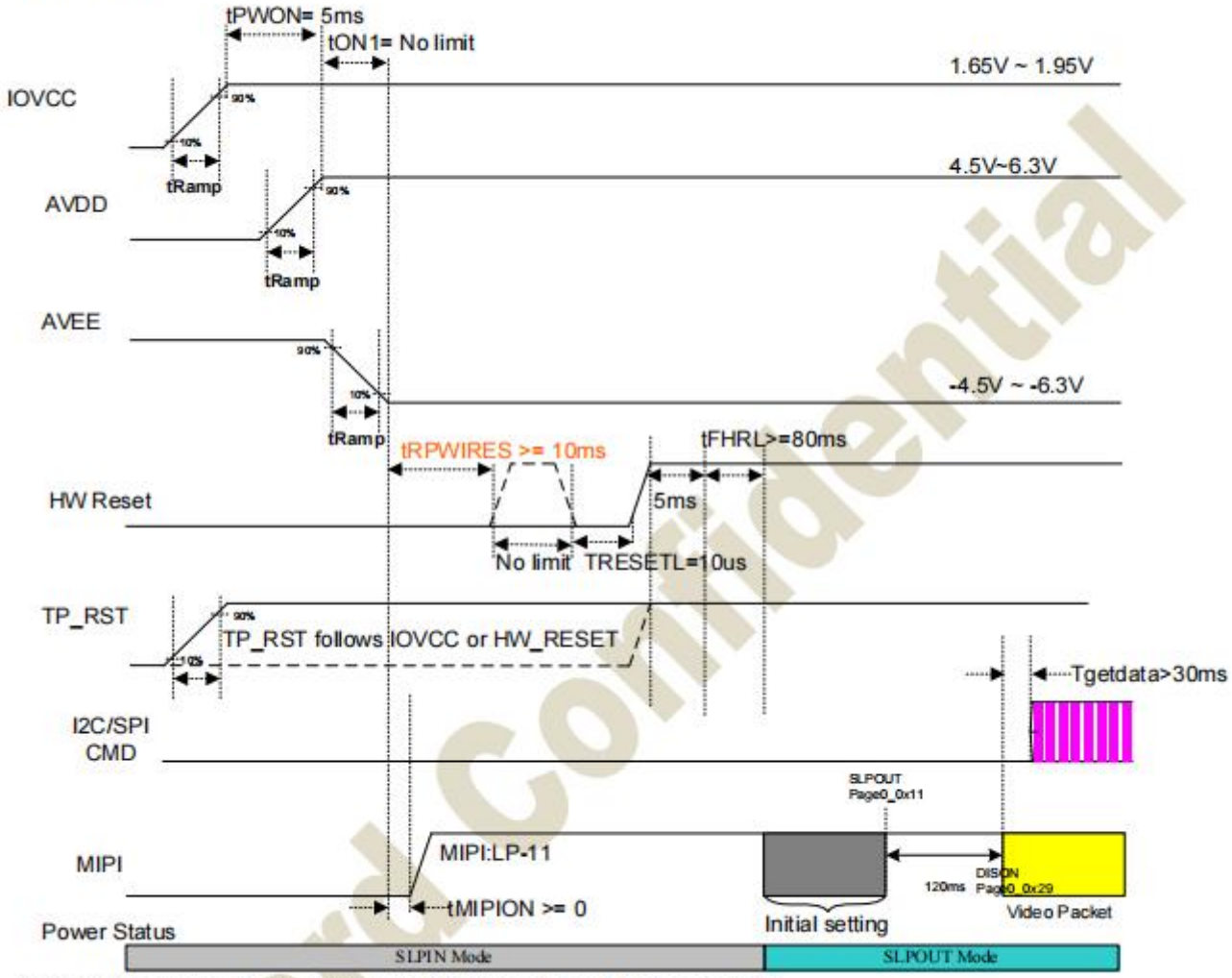
LB:9S4P VF=(2.7~2.9)*9V

IF=(21.5)*4=86mA

4.5POWER ON/OFF

SEQUENCE

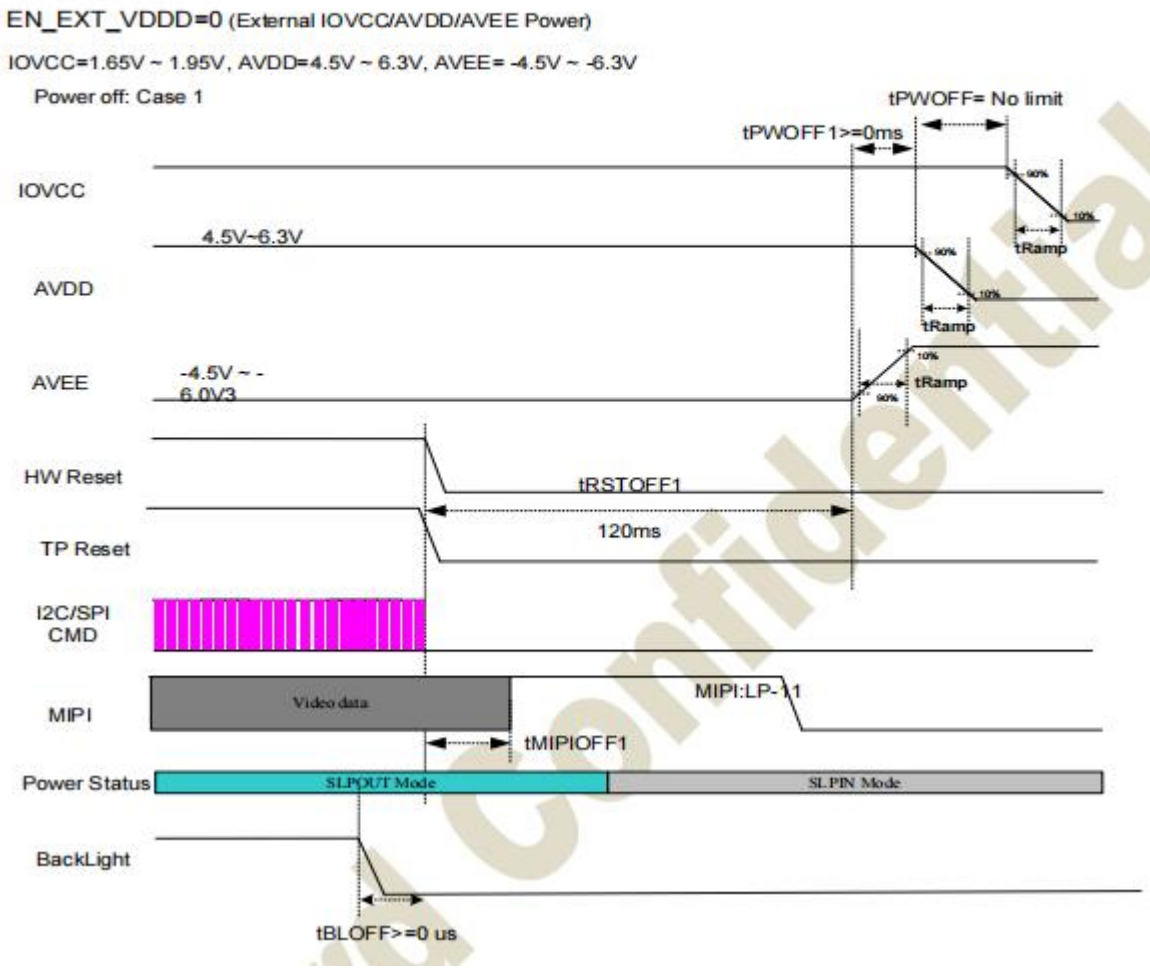
EN_EXT_VDDD=0 (External AVDD/AVEE/IOVCC Power)
IOVCC=VCCH=1.65V ~ 1.95V, AVDD=4.5V ~ 6.3V, AVEE= -4.5V ~ -6.30V, VCI/VCIP will come from internal AVDD.

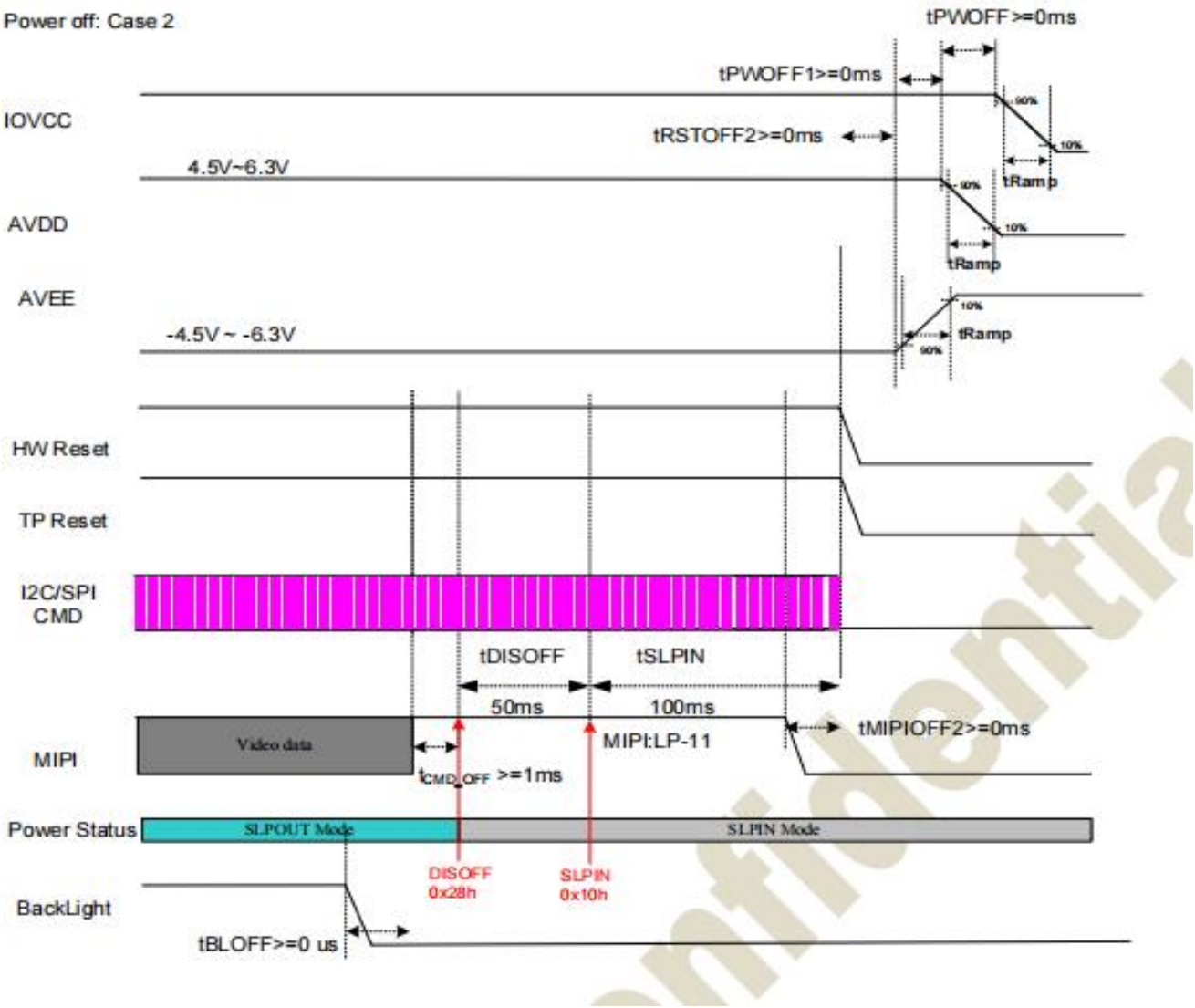


Note: tON1: The space time between AVDD Power On and AVEE Power On.
tON2: The space time between Power On ready and MIPI:LP-11.

4.5.2Power off Sequence

For the power off case2, DISOFF command and tDISOFF are optional. That means t_{CMD_OFF} could be followed by the SLPIN command and tSLPIN , without DISOFF command and tDISOFF.




Power off: Case 2
tPWOFF>=0ms
tPWOFF1>=0ms
IOVCC
tRSTOFF2>=0ms
4.5V~6.3V
AVDD
tRamp
tRamp
AVEE
-4.5V ~ -6.3V
tRamp
HW Reset
TP Reset
I2C/SPI CMD
tDISOFF
tSLPIN
50ms
100ms
tMIPIOFF2>=0ms
MIPI
Video data
MIPI:LP-11
tCMD_OFF >=1ms
Power Status
SLPOUT Mode
SLPIN Mode
DISOFF 0x28h
SLPIN 0x10h
BackLight
tBLOFF>=0 us

5.INPUT SIGNAL TIMING

5.1 .1MIPI DPHY DC Characteristics

(T_A=-40 ~ 85 °C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
IOVCC	V_{IN}	Interface Supply Voltage	1.65	-	1.95	V
VCIP	V_{IN}	Logic Supply Voltage	2.5	-	3.7	V
VDDD	V_{IN}	Digital Supply Voltage	1.2		1.32	V
Input high voltage	V_{IH}	IOVCC= 1.65 ~ 3.3V	0.7 x IOVCC	-	IOVCC	V
Input low voltage	V_{IL}		0	-	0.3 x IOVCC	V
Output high voltage (SDO, LEDPWM)	V_{OH1}	I_{OH} = -1.0 mA	0.8 x IOVCC	-	IOVCC	V
Output low voltage (SDO, LEDPWM)	V_{OL1}	IOVCC= 1.65 ~ 2.4V I_{OL} = 1.0 mA	0	-	0.2 x IOVCC	V
Logic High level input current	I_{IH}	VSYNC, HSYNC	-	-	1	µA
		RESX, DCX_SCL, CSX, RDX, WRX_SCL	-	-	1	µA
	I_{IHD}	DB[7:0], SDI, DCX	-	-	1	µA
		DB[7:0]	-	-	1	µA
Logic Low level input current	I_{IL}	VSYNC, HSYNC	-1	-		µA
		RESX, DCX, CSX, RDX, WRX_SCL	-1	-		µA
	I_{ILD}	DB[7:0], SDI, DCX	-1	-		µA
		DB[7:0]	-1	-		µA
Current consumption standby mode (VCIP/VCI-VSSD)	$I_{ST(VDD)}$	IOVCC=1.8V T_A =25°C	-	TBD	-	µA
Current consumption standby mode (IOVCC– VSSD)	$I_{ST(IOVCC)}$		-	TBD	-	mA
Current consumption during Deep-standby mode (VCIP/VCI-VSSD)	$I_{DP-ST(VDD)}$	IOVCC=1.8V T_A =25°C	-	TBD	-	µA
Current consumption during Deep-standby mode (IOVCC– VSSD)	$I_{DP-ST(IOVCC)}$		-	TBD	-	µA

Table 11.2: DC characteristic

5.2AC CHARACTERISTICS

11.3. AC characteristics

11.3.1.Reset input timings

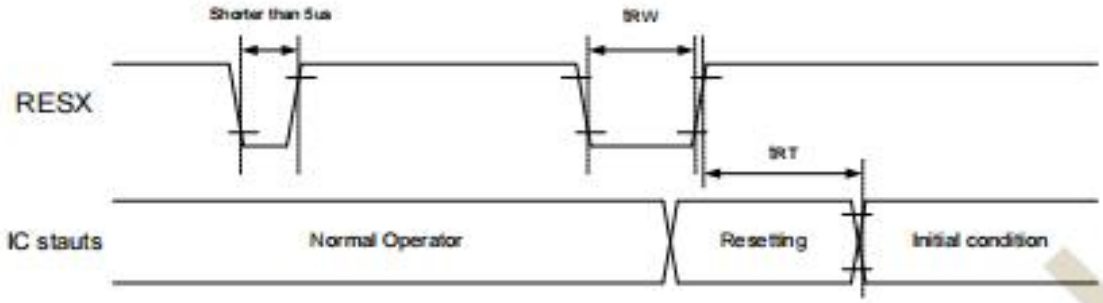


Figure 11.1: Reset input timings

Symbol	Parameter	Related pins	Min.	Max.	Unit
t_{RW}	Reset pulse width(2)	RESX	10	-	µs
t_{RT}	Reset complete time(3)	-	-	5 (Note 5)	ms
		-	-	120 (Note 6, 7)	ms

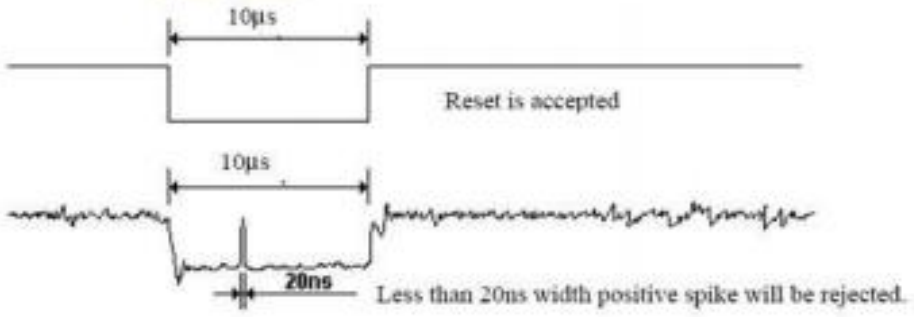
Note: (1) The reset complete time also required time for loading ID bytes from OTP to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

(2) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5 µs	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

(3) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then returns to Default condition for HW reset.

(4) Spike Rejection also applies during a valid reset pulse as shown below:



(5) When Reset is applied during Sleep In Mode.

(6) When Reset is applied during Sleep Out Mode.

(7) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

(8) After Sleep Out command, it is necessary to wait 120msec then send RESX.

Table 11.3: Reset timings

11.3.2. Serial Interface Timing Characteristics (4-line SPI)

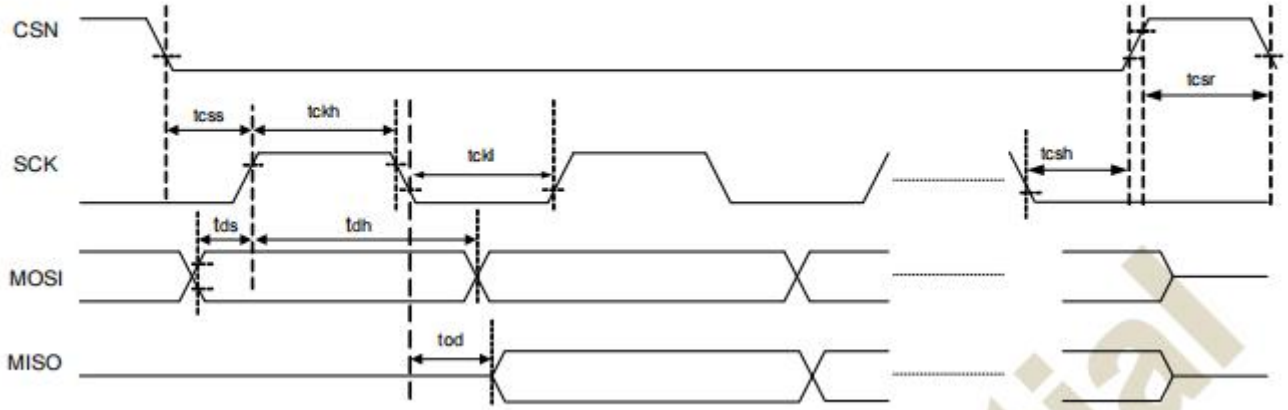


Figure 11.2: 4-line Serial Interface Timing Characteristics

Symbol	Parameter	Min.	Max.	Unit	Note
tcss	Chip select setup time	200		ns	
tcsh	Chip select hold time	200		ns	
tcsr	Chip select recovery time	1000		ns	
tckh	Control pulse "H" duration	31.25		ns	Up to 16MHz
tckl	Control pulse "L" duration	31.25		ns	
tds	Data setup time	25		ns	
tdh	Data hold time	25		ns	
tod	Output delay time	-	50	ns	

11.3.3.DSI D-PHY electronic characteristics

The Description of D-PHY Layer

In general, the DSI - PHY may contain the following electrical functions: Low-Power Receiver (LP-RX), High-Speed Receiver (HS-RX), the Low-Power Contention Detector (LP-CD), and Low Power Transmitter (LP-TX). Figure 13.2 shows the complete set of electronic functions required for a fully featured PHY transceiver.

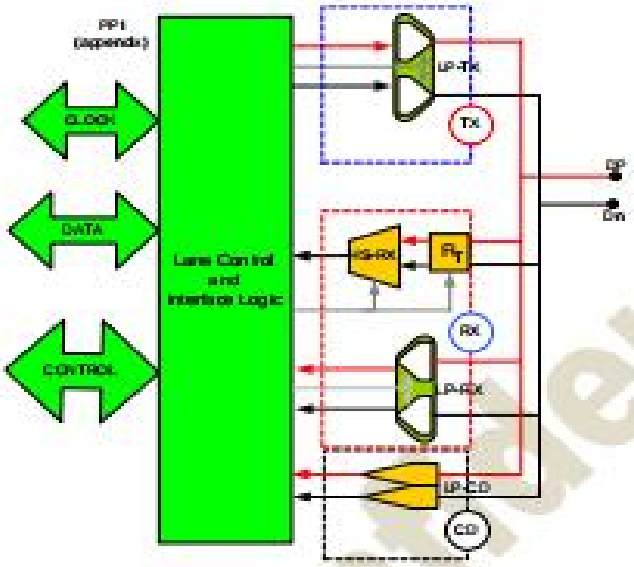


Figure 11.3: Electronic functions of a D-PHY transceiver

Figure13.3 shows both the HS and LP signal levels of electronic characteristics, respectively. Where, the HS receiver utilizes low-voltage swing differential signaling. The LP transmitter and LP receiver utilize low-voltage swing single signaling. Because the HS signaling levels are below the LP low-level input threshold, Lane switches between Low-Power and High-Speed mode during normal operation.

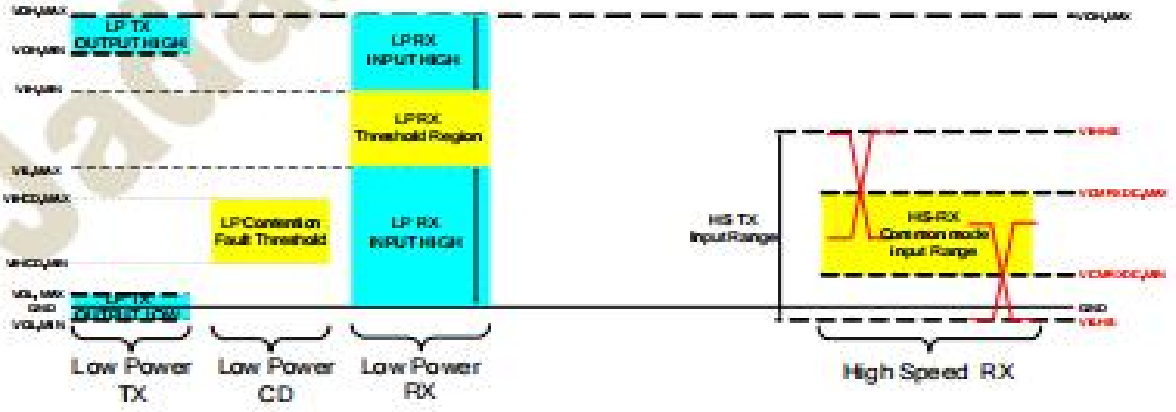


Figure 11.4: HS and LP signal levels

The Electronic Characteristics of Low-Power Transmitter (TX)

The Low-Power TX shall be a slew-rate controlled push-pull driver. It is used for driving the Lines in all Low-Power modes. Hence, it is important to keep static power consumption of a LP TX be as low as possible. Under tables list DC and AC characteristic for Low power transmitter.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{OH}	Thevenin output high level	1.1	1.2	1.3	V	-
V_{OL}	Thevenin output low level	-50	-	50	mV	
Z_{OLP}	Output impedance of LP-TX	110	-	-	Ω	(1)

Note: (1) Though no maximum value for Z_{OLP} is specified, the LP transmitter output impedance shall ensure the t_{RLP}/t_{FLP} specification is met.

Table 11.4: LP-TX DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
t_{RLP}/t_{FLP}	15%-85% rise time and fall time	-	-	25	ns	(1)
$T_{LP-PER-TX}$	Period of the LP exclusive-OR clock	90			ns	
$\delta V/\delta t_{SR}$	Slew rate @ CLOAD = 0pF	30	-	500	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 5pF	-	-	300	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 20pF	-	-	250	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 70pF	-	-	150	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 0 to 70pF (Rising Edge Only)	30	-	-	mV/ns	(1),(3),(7)
	Slew rate @ CLOAD = 0 to 70pF (Rising Edge Only)	30-0.075 * (VO, INST-700)	-	-	mV/ns	(1),(8),(9)
	Slew rate @ CLOAD = 0 to 70pF (Falling Edge Only)	30	-	-	mV/ns	(1),(2),(3)
C_{LOAD}	Load capacitance	-	-	70	pF	-

Note: (1) CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.
(2) When the output voltage is between 400 mV and 930 mV.
(3) Measured as average across any 50 mV segment of the output signal transition.
(4) This parameter value can be lower than TLPX due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters.
(5) This value represents a corner point in a piecewise linear curve.
(6) When the output voltage is in the range specified by VPIN(absmax).
(7) When the output voltage is between 400 mV and 700 mV.
(8) Where VO,INST is the instantaneous output voltage, VDP or VDN, in millivolts.
(9) When the output voltage is between 700 mV and 930 mV.

Table 11.5: LP-TX AC Specifications

The Electronic Characteristics of Receiver (RX)

This part includes two parts which Low-Power RX and High-Speed RX. Because they have differential DC and AC characteristic, first to describe LP-RX then describe HS-RX.

Low-Power Receiver (RX)

The low power receiver is an un-terminated, single-ended receiver circuit. The LP receiver is used to detect the Low-Power state on each pin. For high robustness, the LP receiver shall filter out noise pulses and RF interference. It is recommended the implementer optimize the LP receiver design for low power. The LP receiver shall reject any input glitch when the glitch is smaller than eSPIKE. The filter shall allow pulses wider than TMIN to propagate through the LP receiver. The Figure 13.4 shows Input Glitch Rejection of Low-Power RX. In addition, under tables list DC and AC characteristic for LP-RX.

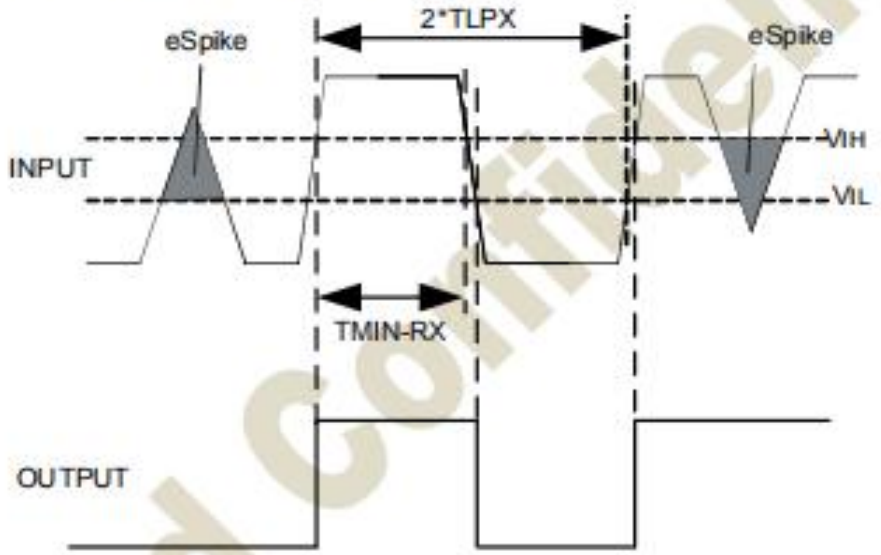


Figure 11.5: Input Glitch Rejections of Low-Power Receivers

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{IH}	Logic 1 input threshold	880	-	-	mV	-
V_{IL}	Logic 0 input threshold, not in ULP state	-	-	550	mV	-

Table 11.6: LP-RX DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
e_{SPIKE}	Input pulse rejection	-	-	300	V.ps	1, 2, 3
T_{MIN}	Minimum pulse width response	20	-	-	ns	4
V_{INT}	Peak-to-peak interference voltage	-	-	200	mV	-
f_{INT}	Interference frequency	450	-	-	MHz	-

Note: (1) Time-voltage integration of a spike above VIL when being in LP-0 state or below VIH when being in LP-1 state
(2) An impulse less than this will not change the receiver state.
(3) In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.
(4) An input pulse greater than this shall toggle the output.

Table 11.7: LP-RX AC Specifications

Line Contention Detection

Contention can be inferred by following conditions:

1. Detect an LP high fault when the LP transmitter is driving high and the pin voltage is less than VIL.

2. Detect an LP low fault shall be detected when the LP transmitter is driving low and the pad pin voltage is greater than VIHCD.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{IHCD}	Logic 1 contention threshold	450	-	-	mV	-
V_{ILCD}	Logic 0 contention threshold	-	-	200	mV	-

Table 11.8: Contention Detector DC Specifications

High-Speed Receiver (RX)

The HS receiver is a differential line receiver. It contains a switch-able parallel input termination, ZID, between the positive input pin Dp and the negative input pin Dn. Under Tables list DC and AC characteristic for HS-RX.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{CMRXDC}	Common-mode voltage HS receive mode	70	-	330	mV	(1),(2)
V_{IDTH}	Differential input high threshold	-	-	70	mV	-
V_{IDTL}	Differential input low threshold	-70	-	-	mV	-
V_{IHHS}	Single-ended input high voltage	-	-	460	mV	(1)
V_{ILHS}	Single-ended input low voltage	-40	-	-	mV	(1)
Z_{ID}	Differential input impedance	80	100	125	Ω	-

Note: (1) Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.
(2) This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz

Table 11.9: HS Receiver DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
$\Delta V_{CMRX(HF)}$	Common mode interference beyond 450 MHz	-	-	100	mV_{PP}	(1)
C_{CM}	Common mode termination	-	-	60	pF	(2)

Note: (1) ΔVCMRX(HF) is the peak amplitude of a sine wave superimposed on the receiver inputs.
(2) For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.

Table 11.10: HS Receiver AC Specifications

High-Speed Data-Clock Timing

This section specifies the required timings on the high-speed signaling interface independent of the electrical characteristics of the signal. The PHY is a source synchronous interface in the Forward direction. In either the Forward or Reverse signaling modes there shall be only one clock source. In the Reverse direction, Clock is sent in the Forward direction and one of four possible edges is used to launch the data.

The Master side of the Link shall send a differential clock signal to the Slave side to be used for data sampling. This signal shall be a DDR (half-rate) clock and shall have one transition per data bit time. All timing relationships required for correct data sampling are defined relative to the clock transitions. Therefore, implementations may use frequency spreading modulation on the clock to reduce EMI.

The DDR clock signal shall maintain a quadrature phase relationship to the data signal. Data shall be sampled on both the rising and falling edges of the Clock signal. The term "rising edge" means "rising edge of the differential signal, i.e. CLKP – CLKN, and similarly for "falling edge". Therefore, the period of the Clock signal shall be the sum of two successive instantaneous data bit times. This relationship is shown in Figure 13.5.

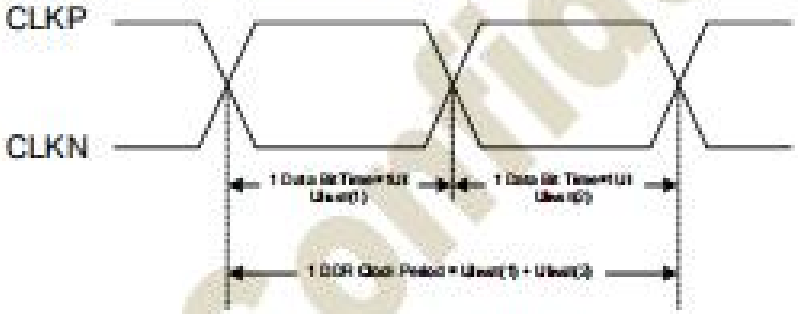


Figure 11.6: DDR Clock Definition

The same clock source is used to generate the DDR Clock and launch the serial data. Since the Clock and Data signals propagate together over a channel of specified skew, the Clock may be used directly to sample the Data lines in the receiver. Such a system can accommodate large instantaneous variations in UI.

The allowed instantaneous UI variation can cause large, instantaneous data rate variations. Therefore, devices shall either accommodate these instantaneous variations with appropriate FIFO logic outside of the PHY or provide an accurate clock source to the Lane Module to eliminate these instantaneous variations.

The UIINST specifications for the Clock signal are summarized in following Table.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
UI instantaneous	UI_{INST}	-	-	3.33	ns	(1), (2), (3)

Note: (1) This value corresponds to a minimum 150 Mbps data rate.
(2) The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.
(3) Maximum total bit rate is 3.92Gbps of 4 data lanes 24-bit data format/ 2.94Gbps of 4 data lane 18-bit data format/ 2.613Gbps of 4 data lane 16-bit data format.

Table 11.11: Reverse HS Data Transmission Timing Parameters

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 8.13. Data is launched in a quadrature relationship to the clock such that the Clock signal edge may be used directly by the receiver to sample the received data.

The transmitter shall ensure that a rising edge of the DDR clock is sent during the first payload bit of a transmission burst such that the first payload bit can be sampled by the receiver on the rising clock edge, the second bit can be sampled on the falling edge, and all following bits can be sampled on alternating rising and falling edges.

All timing values are measured with respect to the actual observed crossing of the Clock differential signal. The effects due to variations in this level are included in the clock to data timing budget.

Receiver input offset and threshold effects shall be accounted as part of the receiver setup and hold parameters.

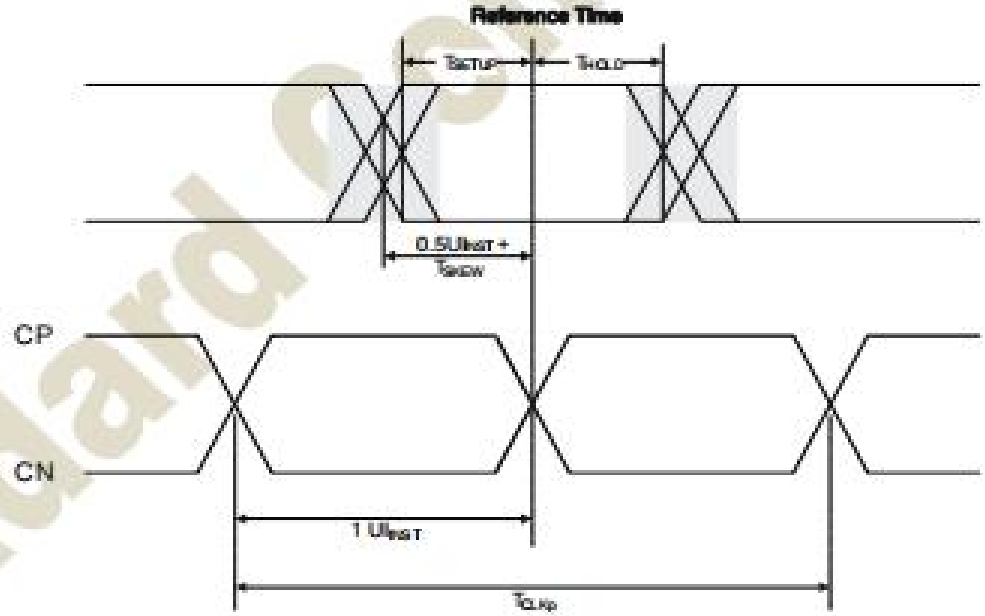


Figure 11.7: Data to Clock Timing Definitions

Data-Clock Timing Specifications

The Data-Clock timing specifications are shown in Table 13.12. Implementers shall specify a value $UI_{INST,MIN}$ that represents the minimum instantaneous UI possible within a High-Speed data transfer for a given implementation. Parameters in Table 13.12 are specified as a part of this value.. The setup and hold times, $T_{SETUP[RX]}$ and $T_{HOLD[RX]}$, respectively, describe the timing relationships between the data and clock signals. $T_{SETUP[RX]}$ is the minimum time that data shall be present before a rising or falling clock edge and $T_{HOLD[RX]}$ is the minimum time that data shall remain in its current state after a rising or falling clock edge. The timing budget specifications for a receiver shall represent the minimum variations observable at the receiver for which the receiver will operate at the maximum specified acceptable bit error rate.

The intent in the timing budget is to leave $0.4*UI_{INST}$, i.e. $\pm 0.2*UI_{INST}$ for degradation contributed by the interconnect.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Data to Clock Setup Time [RX]	$T_{SETUP[RX]}$	0.15	-	-	UIINST	1
Clock to Data Hold Time [RX]	$T_{HOLD[RX]}$	0.15	-	-	UIINST	1

Note: (1) Total setup and hold window for receiver of 0.3*UIINST.

Table 11.12: Data to Clock Timing Specifications

5.3 HIGH-SPEED DATA TRANSMISSION IN BURSTS

Burst Mode Data Transmission

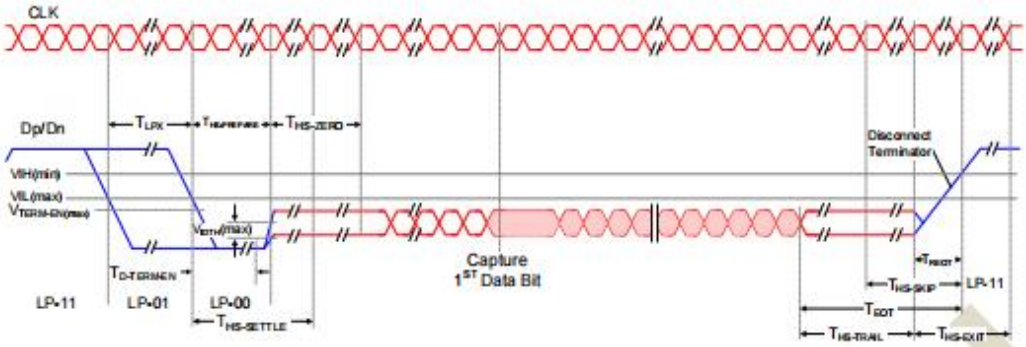


Figure 11.8: High-Speed Data Transmission in Bursts

Parameter	Description	Min	Typ	Max	UNIT
T_{LPX}	Transmitted length of any Low-Power state period	50	-	-	ns
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40 + 4*UI	-	85 + 6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145 + 10*UI	-	-	ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination.	-	-	35 + 4*UI	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions.	85 + 6*UI	-	145 + 10*UI	ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	Max(n*8*UI, 60+n*4*UI)	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns

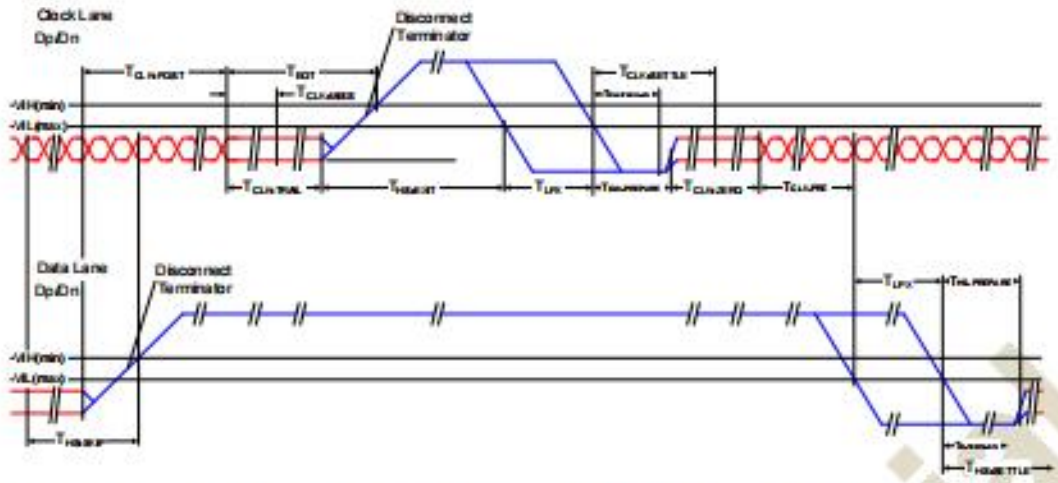


Figure 11.9: Switching the Clock Lane between Clock Transmission and Low-Power Mode

Parameter	Description	Min	Typ	Max	UNIT
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode.	60 + 52*UI	-	-	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8*UI	-	-	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38	-	95	ns
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300	-	-	ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination.	-	-	38	ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns

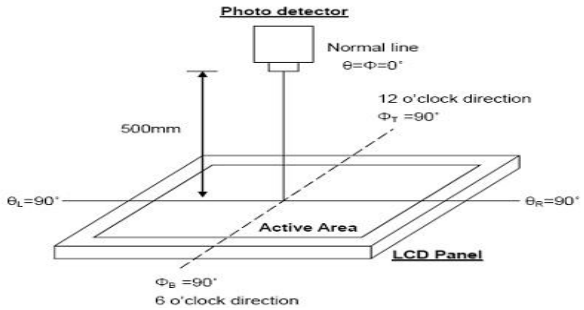
5.4 input timing table

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
DCLK Frequency	fclk	-	166.32	-	MHz
Horizontal valid data	thd		1200		DCLK
Hsync pulse Width	thpw	-	20	-	DCLK
Hsync back porch	thbp	-	80	-	DCLK
Hsync front porch	thfp	-	86	-	DCLK
1 horizontal line	th	-	1386	-	DCLK
Vertical valid data	tvd		1920		T_H
Vsync pulse width	tvpw	-	2	-	T_H
Vsync back porch	tvbp	-	18	-	T_H
Vsync front porch	tvfp	-	60	-	T_H
1 vertical field	tv	-	2000	-	T_H
Frame rate	FR	-	60	-	Hz

6.OPTICAL CHARACTERISTICSTa=25±2℃

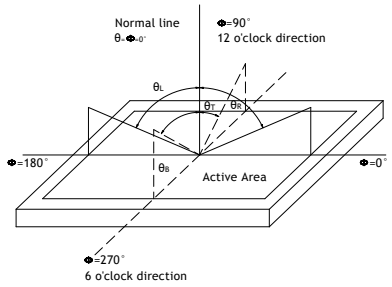
Item		Symbol	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	1000	1500	-		Note1 Note3
Luminance(center)		L	320	400	-	cd/m2	Note1 Note5 Note7
Luminance uniformity		YU	75	80	-	%	Note7
Response Time		$T_{R+}T_F$	-	-	30	ms	Note1 Note4
Color temperature		c	-	7160	-	k	
Viewing Angle K=Contrast Ratio>10	Horizontal	θx^+	75	80	-	degree	Note2
		θx^-	75	80	-		
	Vertical	θy^+	75	80	-		
		θy^-	75	80	-		
Color Chromaticity (CIE1931)	Red	x	Typ-0.03	0.6653	Typ+0.03		Note1 Note5 Note7
		y		0.3156			
	Green	x		0.2629			
		y		0.6024			
	Blue	x		0.1323			
		y		0.0755			
	White	x		0.2990			
		y		0.3149			
Colorgamut (NTSC ratio)			-	64.7		%	

Note1: Definition of optical measurement system (BM-7)



Note2: Definition of viewing angle range and measurement system

Viewing angle is measured at the center point of the LCD by CONOSCOPE (ergo-80).



Note3: Definition of Response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (TON) is the time between photo detector outputintensity changed from 90% to 10%. And fall time (TOFF) is the time between photodetector output intensity changed from 10% to 90%.

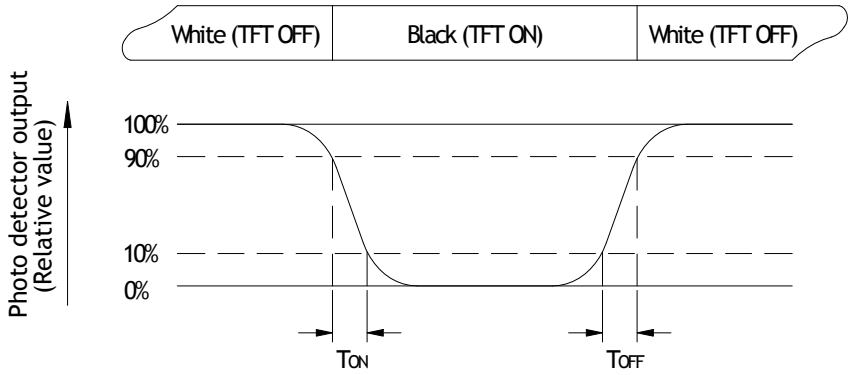


Fig. Definition of response time

Note4: Definition of contrast ratio

$$\text{Contrast ratio(CR)}=\frac{\text{Luminance measured when LCD on the Whitestate}}{\text{Luminance measured when LCD on the Blackstate}}$$

"White state ": The state is that the LCD should drive by Vwhite.

"Black state": The state is that the LCD should drive by Vblack.

Vwhite: To be determined Vblack: To be determined.

Note5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

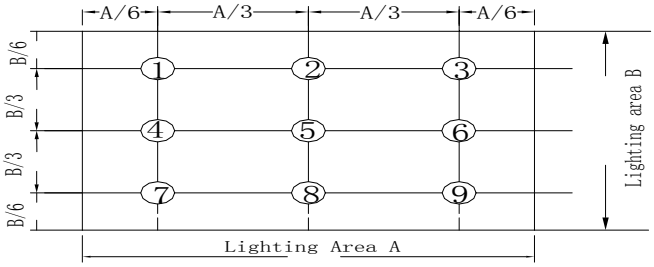
Note6: All input terminals LCD panel must be ground while measuring the center area of the

panel. The LED driving condition is IL=86mA

Note7: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas.Everymeasuring point is placed at the center of each measuring area.

Luminance Uniformity (U) = Lmin/ Lmax L----Active area length, W---- Active area width



Bmax: The measured maximum luminance of all measurement position.

Bmin: The measured minimum luminance of all measurement position.

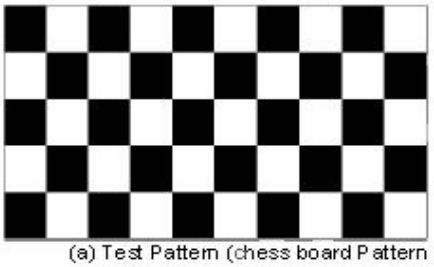
7.RELIABILITY TEST ITEMS

7.1 TEMPERATURE AND HUMIDITY

Test Item	Test Condition	Remark
HighTemperatureStorage	Ta=80℃; 240hrs	IEC60068-2-1：2007 GB2423.2-2008
Low Temperature Storage	Ta=-40℃;240hrs	IEC60068-2-1：2007 GB2423.1-2008
High Temperature Operation	Ta=60℃，240Hrs	IEC60068-2-1：2007 GB2423.2-2008
LowTemperatureOperation	Ta=-20℃; 240hrs	IEC60068-2-1：2007 GB2423.1-2008
HighTemperatureHighHumidity Operation	Ta=60℃，90%RH 240Hrs	IEC60068-2-78：2001 GB/T2423.3-2006
Thermal Shock	-40℃(0.5h) ~ 60℃(1h) / 50 cycles	Start with cold temperature ， End with high temperature， IEC60068-2-14:1984,GB2423.22-2002
Image Sticking	25℃ ; 0.5hrs	Note1

Note1:Condition of image sticking test :25℃±2℃

Operation with test pattern sustained for 0.5hrs,then change to 50% gray pattern immediately.after30s,themura must be disappeared completely



(a) Test Pattern (chess board Pattern)

(b) Gray Pattern

7.2 VIBRATION SHOCK

Test item	Conditions	Remark
Packing Shock (non-operation)	980m/s2,6ms, ±x,y,z 3times for direction	IEC60068-2-27：1987 GB/T2423.5-1995
Packing Vibration (non-operation)	Frequency range:10 HZ~50HZ Stroke:1.0mm,sweep:10 HZ ~50HZ x,y,z 2 hours for each direction	IEC60068-2-32：1990 GB/T2423.8-1995

7.3ESD

Test item	Conditions	Remark	
Electro Static Discharge Test (non-operation)	150pF，330Ω， Contact:±4KV,Air:±8KV	1	参考 Lenovo TFTL CD test plann
	200pF，0Ω，±200V contact test	2	

8. GENERAL PRECAUTION

8.1 SAFETY

1. Do not swallow any liquid crystal, even if there is no proof that liquid crystal ispoisonous.
2. If the LCD panel breaks, be careful not to get liquid crystal to touch your skin.
3. If skin is exposed to liquid crystal, wash the area thoroughly with alcohol or soap.

8.2 STORAGE CONDITIONS

1. Store the panel or module in a dark place where the temperature is 23±5°C andThehumidity is below 50±20%RH.
2. Store in anti-static electricity container.
3. Store in clean environment, free from dust, active gas, and solvent.
4. Do not place the module near organics solvents or corrosive gases.
5. Do not crush, shake, or jolt the module.

8.3 HANDLING PRECAUTIONS

1. Avoid static electricity which can damage the CMOS LSI.
2. The polarizing plate of the display is very fragile. So, please handle it verycarefully.
3. Do not give external shock.
4. Do not apply excessive force on the surface.
5. Do not wipe the polarizing plate with a dry cloth, as it may easily scratch the Surface of plate.
6. Do not use ketonics solvent Aromatic solvent, use with a soft cloth soaked witha cleaning naphtha solvent.
7. Do not operate it above the absolute maximum rating.
8. Do not remove the panel or frame from the module.
9. When the module is assembled, it should be attached to the system firmly,Be careful not to twist and bend the module.
10. Wipe off water droplets or oil immediately. If you leave the droplets for a long time,staining and discoloration may occur.
11. If the liquid crystal material leaks from the panel, it should be kept away from the

eyesormouth in case of contact with hands, legs or clothes, it must be washedawaythoroughly with soap.

8.4 WARRANTY

1.The period is within twelve months since the date of shipping out under normal using and storage conditions.

2. Do not repaired or modified the LCM. It may cause function to lose efficacy,Starry does not warrant the LCM.

3. All process and material comply ROHS.

9. PACKAGE DRAWING