☐ Preliminary Specification
■ Final Specification

Customer Approve：

QC 品 质 ：_____

R&D 研 发 ：_____

Approved 批准：_____

产品型号(Description)： LS101I22-MP-V1

Compile by 编制	Quality/Engineer 品质/工程	Checked 审核	Approved 批准

SPECIFICATION FOR

LCM

REVISION RECORD

REV NO	REV DATE	CONTENTS	REMARKS
V.0	2021-09-20	First Release	

Table of contents

LCM

1.0 General description

1.1 Introduction

LS101I22-MP-V1 is model a color active matrix thin film transistor (TFT) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. This model is composed of a TFT LCD panel, a driving circuit and a back light system. This TFT LCD has a 10.1 inch diagonally measured active display area with WXGA (800 horizontal by 1280 vertical pixel array) resolution. The TFT-LCD panel used for this module is adapted for a low reflection and higher color type.

1.2 Features

- 4 lanes MIPI Interface
- Low driving voltage and low power consumption
- ROHS Compliant

1.3 General information

Item	Specification	Unit	Remarks
Outline Dimension	143(H) x 228.6(V) x 2.65(body)	mm	Tolerance:±0.2mm
Display area	135.36(W) x216.58(H)	mm	
Number of Pixel	800(H) x RGB x1280(V)	pixels	
Pixel pitch	169.2(H) x 169.2(V)	μm	
Pixel arrangement	Pixels RGB stripe arrangement		
Display mode	Normally Black		
Surface treatment	IPS Film		
Driver IC	--		
Back-light	Single LED (Side-Light type)		

1.4 Mechanical Information

Item		Min.	Typ.	Max.	Unit
Module Size	Horizontal(H)	142.8	143	143.2	mm
	Vertical(V)	228.4	228.6	228.8	mm
	Depth(D)	2.45	2.65	2.85	mm

2.0 ABSOLUTE MAXIMUM RATINGS

2.1 Electrical Absolute Rating

2.1.1 TFT LCD Module

Item		Specification	Unit
Outline Dimension		143(H) x 228.6(V) x 2.65(body)	mm
Display area		135.36(W) x216.58(H)	mm
Number of Pixel		800(H) x RGB x1280(V)	pixels
Pixel pitch		169.2(H) x 169.2(V)	μ m
Pixel arrangement		Pixels RGB stripe arrangement	
Display mode		Normally Black	
Surface treatment		IPS Film	
Weight		TBD (Typ.)	gram
Back-light		Single LED (Side-Light type)	
Power Consumption	B/L System	TBD(Max.)	watt

2.1.2 Back-Light Unit

Item	Symbol	Typ	MIN.	TYP.	MAX.	Unit	Note
Forward voltage	Vf	24	21.6	24	26.4	V	(1)(2)
Forward current	If	80	--	80	--	mA	(1)(2) (3)
Power Consumption	PBL	--	--	--	--	mW	

Note:

(1) Permanent damage may occur to the LCD module if beyond this specification. Functional operation should be restricted to the conditions described under normal operating conditions.

(2) Ta =25±2℃

(3) Test Condition: LED current 80mA

3.0 OPTICAL CHARACTERISTICS

3.1 Optical Specifications

Item	Symbol	Temp	Condition	Min	Typ	Max	Unit	Remark
Viewing Angle Range	Horizontal	θ	CR > 10	80	85	--	Deg	Note 1
	Vertical	θ		80	85	--	Deg	
Luminance Contrast ratio		CR	θ = 0°	600	800	--	--	Note 2
Brightness		YL		400	450	--	Cd/cm2	
Transmittance		T(%)	θ = 0°	--	6.1	--	%	Note 3
Color Gamut (C light)				50	60	--	%	
White chromaticity		Wx	Θ=0°	TYP. -0.05	0.397	TYP. +0.05		Note 4
		Wy			0.311			
Reproduction of color （C-light）	Red	Rx			--			
		Ry			--			
	Green	Gx			--			
		Gy			--			
	Blue	Bx			--			
		By			--			
Response Time (Rising + Falling)	Trt		Ta= 25°C θ = 0°	--	30	40	ms	Note 5

3.2 Measuring Condition

Measuring surrounding: dark room ,LED current IL : 80mA

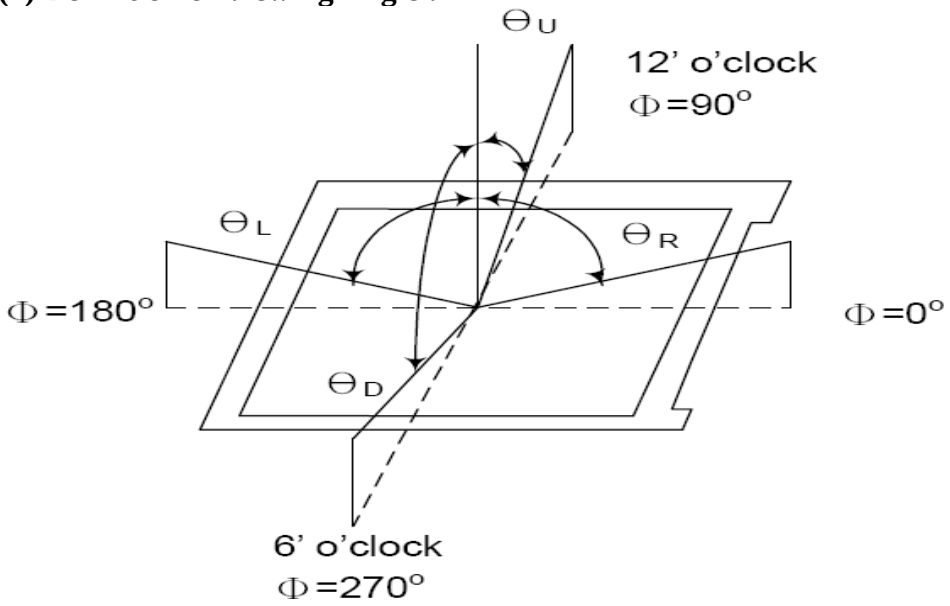
Ambient temperature: 25±2℃

15min. warm-up time.

3.3 Measuring Equipment

FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics. Measuring spot size: 20 ~ 21 mm

Note (1) Definition of Viewing Angle :

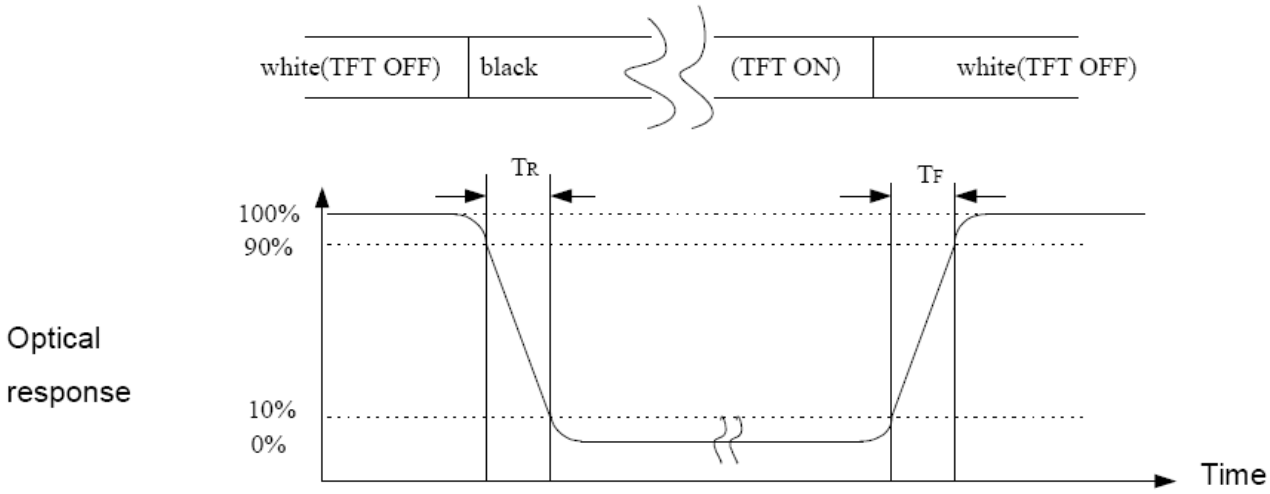


Note (2) Definition of Contrast Ratio (CR):

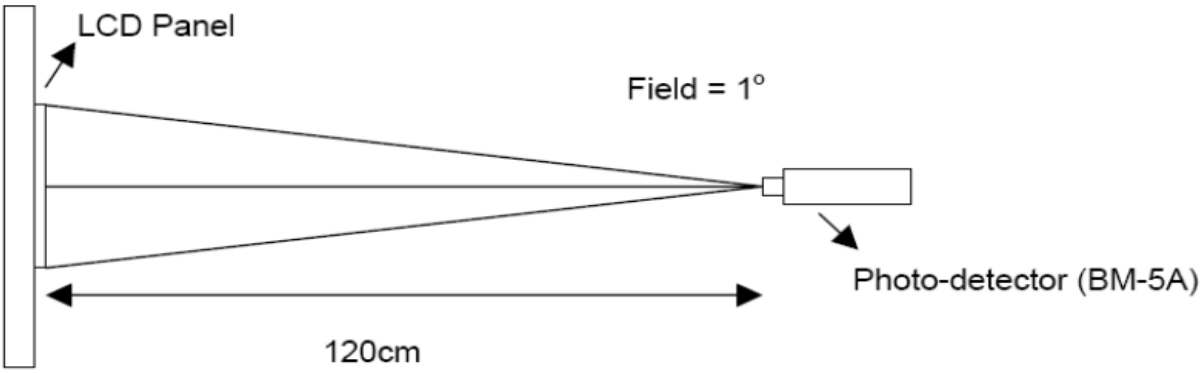
Measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

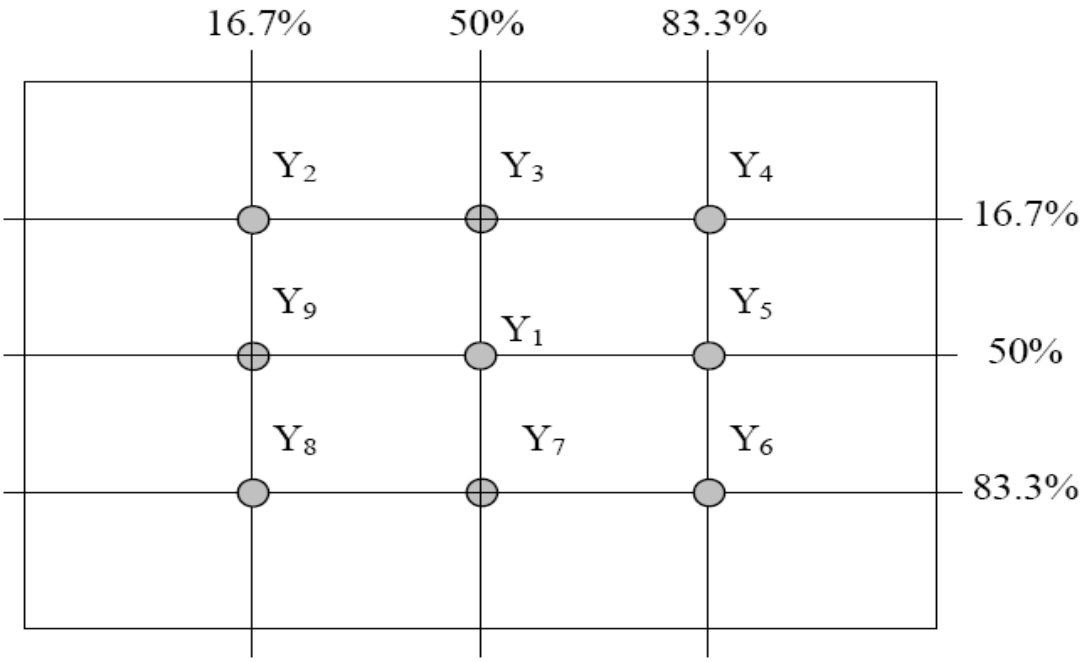
Note (3) Definition of Response Time: Sum of TR and TF



Note (4) Definition of optical measurement setup



Note (5) Definition of brightness uniformity



$$\text{Luminance uniformity} = \frac{\text{(Min Luminance of 9 points)}}{\text{(Max Luminance of 9 points)}} \times 100\%$$

4.0 INTERFACE PIN CONNECTION

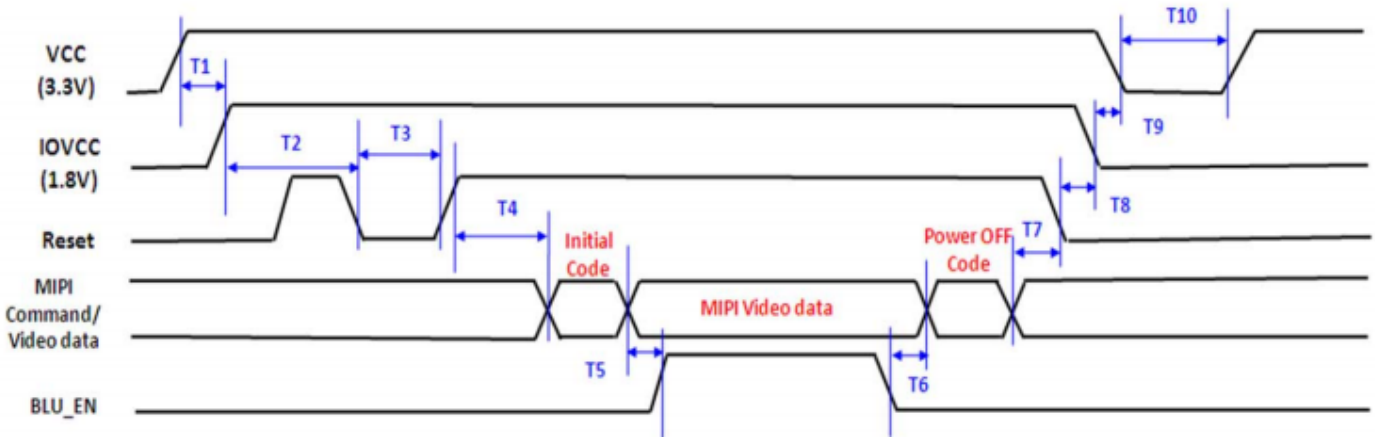
4.1 Signal of interface

Terminal No.	Symbol	I/O	Functions
1	LEDA	P	Power for LED backlight (Anode)
2	LEDA	P	Power for LED backlight (Anode)
3	LEDA	P	Power for LED backlight (Anode)
4	NC	N	No connection
5	LEDK	P	Power for LED backlight input (cathode)
6	LEDK	P	Power for LED backlight input (cathode)
7	LEDK	P	Power for LED backlight input (cathode)

8	LEDK	P	Power for LED backlight input (cathode)
9	GND	P	Ground
10	GND	P	Ground
11	MIPI_D2+	I	Positive MIPI differential data inputs2+
12	MIPI_D2-	I	Negative MIPI differential data inputs2-
13	GND	P	Ground
14	MIPI_D1+	I	Positive MIPI differential data inputs1+
15	MIPI_D1-	I	Negative MIPI differential data inputs1-
16	GND	P	Ground
17	MIPI_CLK+	I	Positive MIPI differential clock inputs
18	MIPI_CLK-	I	Negative MIPI differential clock inputs
19	GND	P	Ground
20	MIPI_D0+	I	Positive MIPI differential data inputs0+
21	MIPI_D0-	I	Negative MIPI differential data inputs0-
22	GND	P	Ground
23	MIPI_D3+	I	Positive MIPI differential data inputs3+
24	MIPI_D3-	I	Negative MIPI differential data inputs3-
25	GND	P	Ground
26	IOVCC 1V8	O	Logic Power supply(+1.8V)
27	RESET	P	Global reset pin.
28	GND	P	Ground
29	IOVCC 1V8	P	Logic Power supply(+1.8V)
30	VDD3V3	P	Power for Digital block（+3.3V）
31	VDD3V3	P	Power for Digital block（+3.3V）

5.0 Power On/Off Sequence

To prevent the device damage from latch up,the power on/off sequence shown Below must be followed.



Power ON/OFF			
Parameter	Value		
	min.	max.	Unit
T1	0.5	–	ms
T2	1	–	
T3	0.02	–	
T4	5	–	
T5	200	–	
T6	40	–	
T7	0	–	
T8	1	–	
T9	No Limit	–	
T10	500	–	

6.0 ELECTRICAL CHARACTERISTICS

6.1 TFT LCD Module

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	IOVCC	1.65	1.8	3.3	V
	VDD	3.0	3.3	3.6	V
	IVDD	--	120	--	mA

6.2 Back-Light Unit

The backlight system is an edge-lighting type with 32 LED.

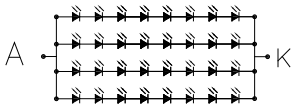
The characteristics of the LED are shown in the following tables.

Item	Symbol	Min.	Typ.	Max.	Unit	Note
LED current	IL	-	80	-	mA	(2)
LED Voltage	VL	-	24	-	V	
Operating LED life time	Hr	10000	20000	-	Hour	(1)(2)

Note (1) LED life time (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25±3℃, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note (2) The "LED life time" is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL=80mA. The LED lifetime could be decreased if operating IL is larger than 80mA. The constant current driving method is suggested.

LED CIRCUIT DIAGRAM： 8 x 4 = 32 LED



6.3 DC Characteristics

6.3.1 Absolute Maximum Rating (GND=AGND=0V)

Parameter	Symbol	Spec.			Unit	Note
		Min.	Typ.	Max.		
Interface Supply Voltage	IOVCC	-0.3	-	+3.6	V	Note (3) (4)
Logic Supply Voltage	VCI	-0.3	-	+6.6	V	Note (3) (5)
Analog Supply Voltage	VCIP	-0.3	-	+6.6	V	Note (3) (6)
High speed interface Supply Voltage	VCCH	-0.3	-	+6.6	V	Note (3) (7)
Positive Voltage input	AVDD	-0.3	-	AVDD+0.5	V	Note (8)
Negative Voltage input	AVEE	0	-	-6.6	V	Note (9)
Power Supply Voltage	VGH	-0.3	-	+25	V	Note (10)
Power Supply Voltage	VGL	0	-	-16	V	Note (11)
Operation Temperature	TOPR	-10	-	+60	℃	
Storage Temperature	TSTG	-20	-	+60	℃	

Note: (1) All of the Voltages listed above are with respective to GND=0V.

(2) Device is subject to be damaged permanently if stresses beyong those absolute maximum ratings listed above.

(3) IOVCC, VSSD must be maintained.

(4) To make sure IOVCC ≥ VSSD.

(5) To make sure VCIP ≥ AVSS.

(6) To make sure VCI ≥ AVSS.

(7) To make sure VCCH ≥ VSSH.

(8) To make sure AVDD ≥ AVSS.

(9) To make sure AVSS ≥ AVEE.

（10）To make sure VGH ≥ AVSS.

（11）To make sure AVSS ≥ VGL , VGH+|VGL|＜30V.

6.3.2 DC electrical characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
IOVCC	V_{IN}	Interface Supply Voltage	1.65	-	3.6	
VCIP	V_{IN}	Logic Supply Voltage	2.5	-	6.0	
VCI	V_{IN}	Analog Supply Voltage	2.5	-	6.0	
VCCH	V_{IN}	High speed interface Supply Voltage	1.65	-	3.6	
Input high voltage	V_{IH}	IOVCC= 1.65 ~ 3.3V VCIP= 2.5 ~ 3.3V VCI= 2.5 ~ 3.3V	0.7 $_{IOVCC}$	-	IOVCC	V
Input low voltage	V_{IL}		0	-	0.3 $_{IOVCC}$	V
VPP	V_{IH}	VPP	7.25V	7.5V	7.75V	V
	V_{IL}					
Output high voltage (SDO, LEDPWM)	V_{OH1}	I_{OH} = -1.0 mA	0.8 $_{IOVCC}$	-	IOVCC	V
Output low voltage (SDO, LEDPWM)	V_{OL1}	IOVCC= 1.65 ~ 2.4V I_{OL} = 1.0 mA	0	-	0.2 $_{IOVCC}$	V
Logic High level input current	I_{IH}	VSYNC, HSYNC	-	-	1	μA
		RESX, DCX_SCL, CSX, RDX, WRX_SCL	-	-	1	μA
	I_{IHD}	DB[23…0], SDI, DCX	-	-	1	μA
		DB[23…0]	-	-	1	μA
Logic Low level input current	I_{IL}	VSYNC, HSYNC	-1	-		μA
		RESX, DCX, CSX, RDX, WRX_SCL	-1	-		μA
	I_{ILD}	DB[23…0], SDI, DCX	-1	-		μA
		DB[23…0]	-1	-		μA
Current consumption standby mode (VCIP/VCI-VSSD)	$I_{ST(VDD)}$	VCIP/VCI=2.8V, IOVCC=1.8V T_A =25°C	-	TBD	-	μA
Current consumption standby mode (IOVCC– VSSD)	$I_{ST(IOVCC)}$		-	TBD	-	μA
Current consumption during Deep-standby mode (VCIP/VCI-VSSD)	$I_{DP-ST(VDD)}$	VCIP/VCI=2.8V, IOVCC=1.8V T_A =25°C	-	TBD	-	μA
Current consumption during Deep-standby mode (IOVCC– VSSD)	$I_{DP-ST(IOVCC)}$		-	TBD	-	μA

Note: 1. The VOTP pin is open on normal mode and in used white OTP programming condition.
2. The GRAM data is eliminated under the Deep standby mode.

6.4 AC Characteristics

6.4.1 Reset input timing

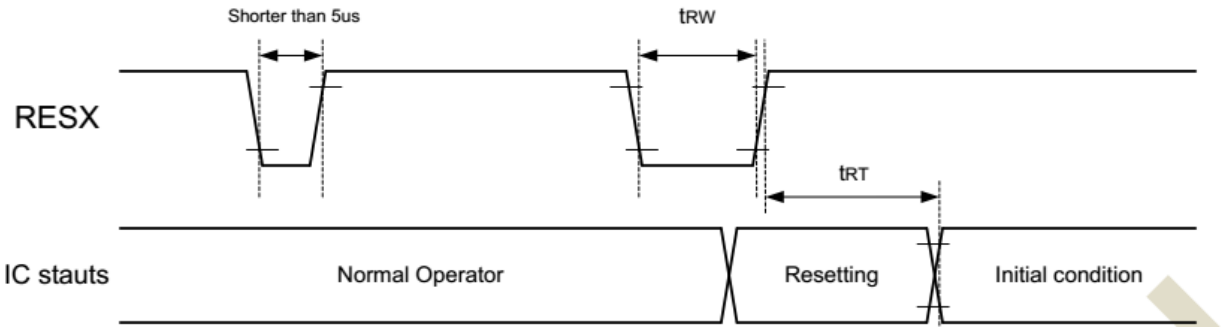


Figure: Reset input timings

Symbol	Parameter	Related pins	Min.	Max.	Unit
t_{RW}	Reset pulse width(2)	RESX	10	-	µs
t_{RT}	Reset complete time(3)	-	-	5 (Note 5)	ms
		-	-	120 (Note 6, 7)	ms

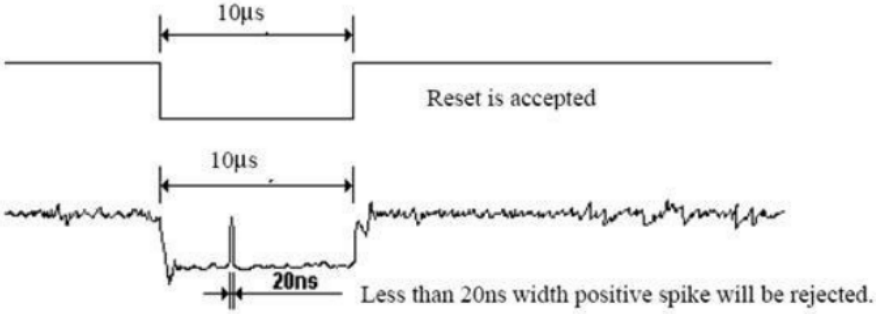
Note: (1) The reset complete time also required time for loading ID bytes from OTP to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

(2) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5 µs	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

(3) During the resetting period, the display will be blanked (The display is entering blanking sequence,which maximum time is 120 ms, when Reset Starts in Sleep Out-mode. The display remains the blank state in Sleep In-mode) and the returns to Default condition for H/W reset.

(4) Spike Rejection also applies during a valid reset pulse as shown below:



(5) When Reset is applied during Sleep In Mode.

(6) When Reset is applied during Sleep Out Mode.

(7) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

Figure: Reset timings

6.4.2 DSI D-PHY electrical characteristics

MIPI Receiver Differential input （DC characteristics）						
Symbol	Description	Parameter	Min.	Typ.	Max.	Unit
LP_CD	Logic 1 contention threshold	VIH	450	--	--	mV
	Logic 0 contention threshold	VIL	--	--	200	mV
HS_RX	Common-mode voltage（HS RX mode）	VCMRX(DC)	70	--	330	mV
	Differential input high threshold（HS Rx mode）	VIDTH	--	--	70	mV
	Differential input low threshold（HS Rx mode）	VIDTL	-70	--	--	mV
	Single-end input high voltage（HS Rx mode）	VIHHS	--	--	460	mV
	Single-end input low voltage（HS Rx mode）	VILHS	-40	--	--	mV
	Single-ended threshold for HS termination enable	VTERM-EN	--	--	450	mV
	Differential input impedance	ZID	80	100	125	Ω
LP_RX	Logic 1 input voltage （LP Rx mode）	VIH	880	--	--	mV
	Logic 0 input voltage （LP Rx mode）	VIL	--	--	550	mV
	Input hysteresis	VHYST	25	--	--	mV
LP_TX	Output high level（LP Tx mode）	VOH	1.1	1.2	1.3	V
	Output low level（LP Tx mode）	VOL	-50	--	50	mV
	Output impedance of LP transmitter	ZOLP	110	--	--	Ω

- High-Speed Data-Clock Timing

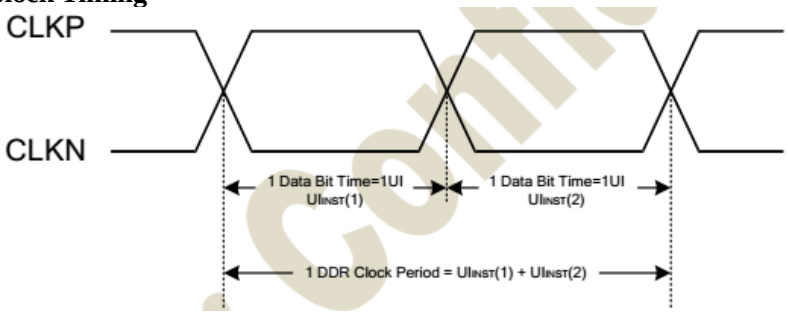


Figure: DDR Clock Definition

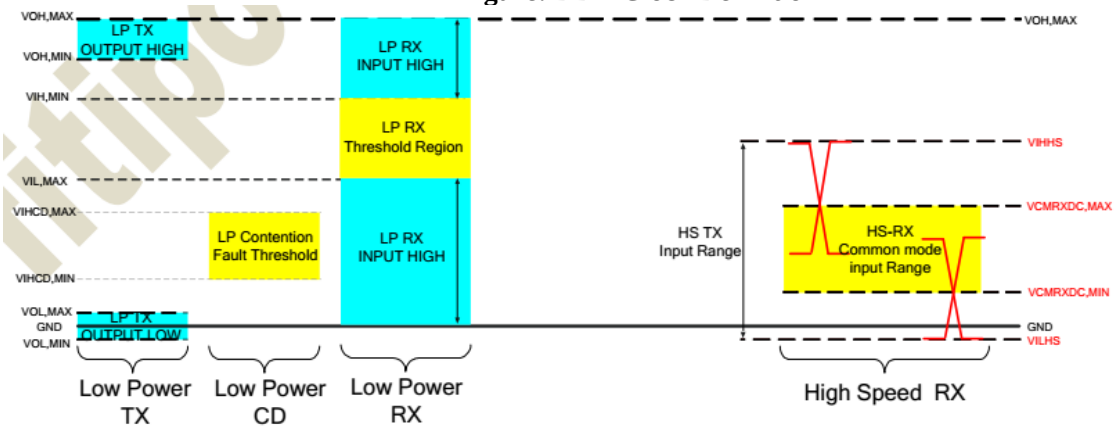


Figure: HS and LP single levels

- The UIINST specifications for the Clock signal are summarized in following Table:

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
UI_{INST}	UI instantaneous	--	--	12.5	ns	(2),(3)

Note: (1) This max value corresponds to a minimum 80 Mbps data rate per lane

(2) The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst

- Host sends a differential clock signal to the IC for data sampling. This signal is a DDR (half-rate) clock and has one Transition per data bit time. The timing relationship of the DDR Clock differential MIPI data to clock timing definitions.

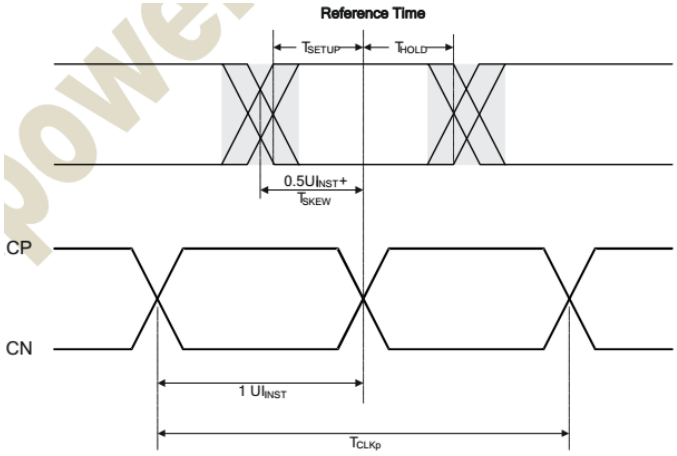


Figure: Data to clock Timing Definition

- MIPI Data Clock Timing Specification

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
T_{SKEW}[TX]	Data to Clock Skew (mesured at transmitter)	-0.15	--	0.15	--	(1)
T_{SETUP}[RX]	Data to Clock Setup Time (receiver)	0.15	--	--	UIINST	(2),(3)
T_{HOLD}[RX]	Data to Clock Hold Time (receiver)	0.15	--	--	UIINST	(2),(3)

Note: (1) Total silicon and package delay budget of 0.3*UIINST

(2) Total setup and hold window for receiver of 0.3*UIINST

(3) T_{SETUP}[RX] and T_{HOLD}[RX] without FPCB and connector and guaranteed by design

- Bursts Mode Data Transmission

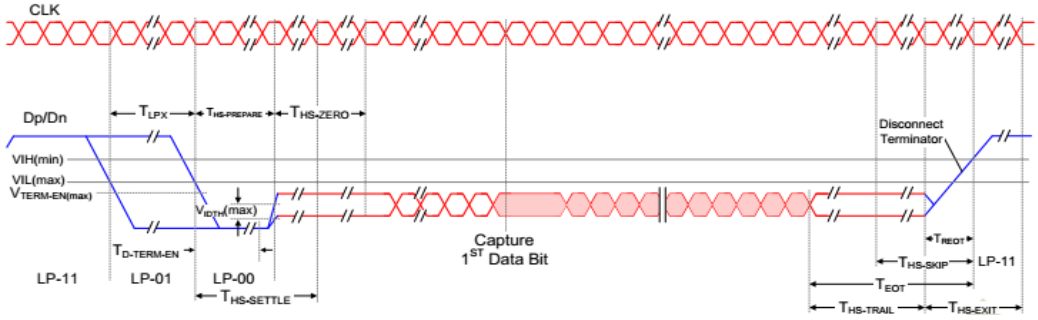


Figure: High-Speed Data Transmission in Bursts

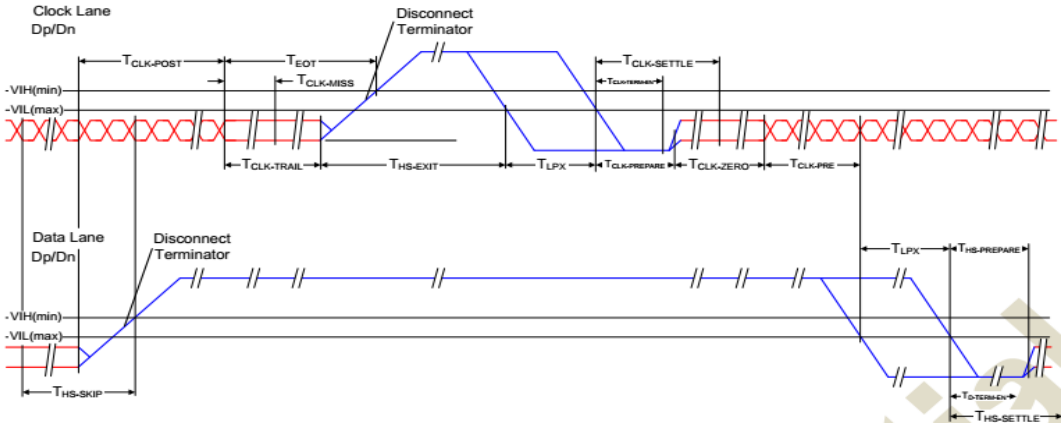


Figure: Switching the Clock Lane between Clock Transmission and Low-Power Mode

6.4.3 Timing for DSI Video mode

➢ **MIPI Clock: 205MHz(410Mbps),Refresh rate 60Hz**

- **Vertical timings**

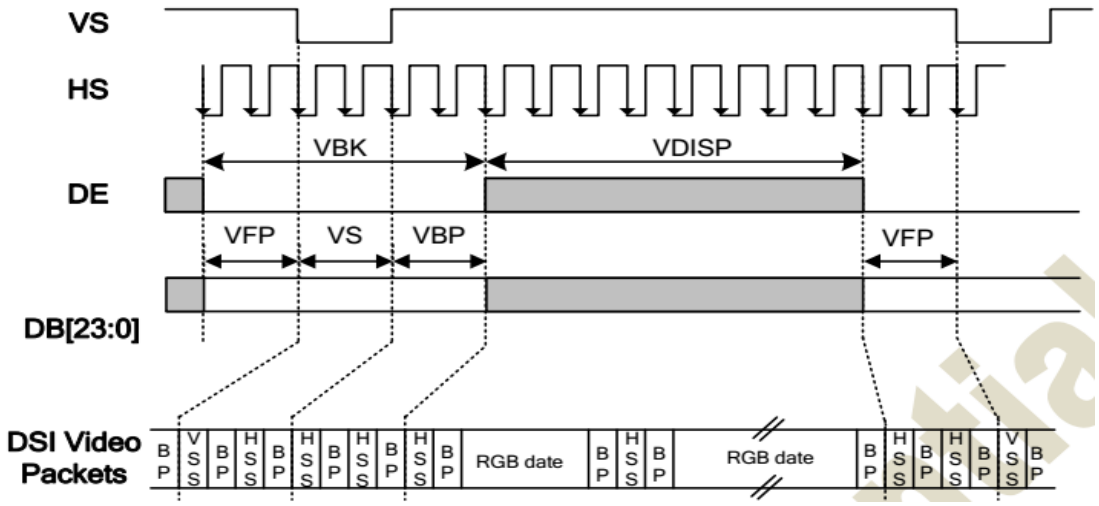


Figure: Vertical Timing for DPI I/F

(Ta=25℃，IOVCC=1.8V,VCIP=3.3V,VCI=3.3V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical low pulse width	VS	--	2	4	200 Note(1)	Line
Vertical front porch	VFP	--	4	30	200	Line
Vertical back porch	VBP	--	2	8	200 Note(1)	Line
Vertical active area	--	VDISP	--	1280	--	Line
Vertical Refresh rate	VRR	--	--	60	--	Hz

Note: (1) The VS and VBP pulse width are related to GIP start pulse and GIP clock pulse timing. The GIP start pulse and GIP clock pulse mast be set at corresponding position for LCD normal display.

- **Horizontal Timing**

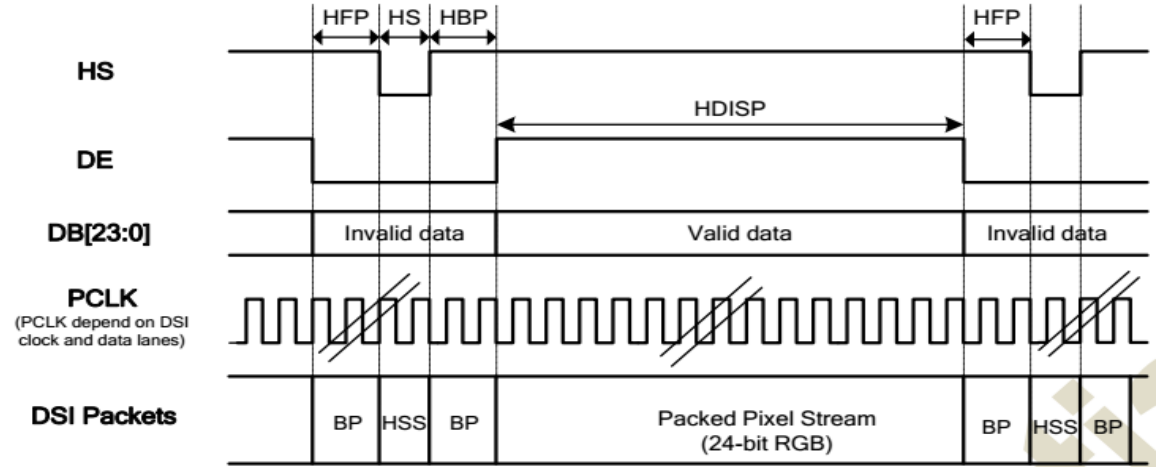


Figure: Horizontal Timing for DPI I/F

(Ta=25℃，IOVCC=1.8V,VCIP=VCI=VCCH=2.8V)

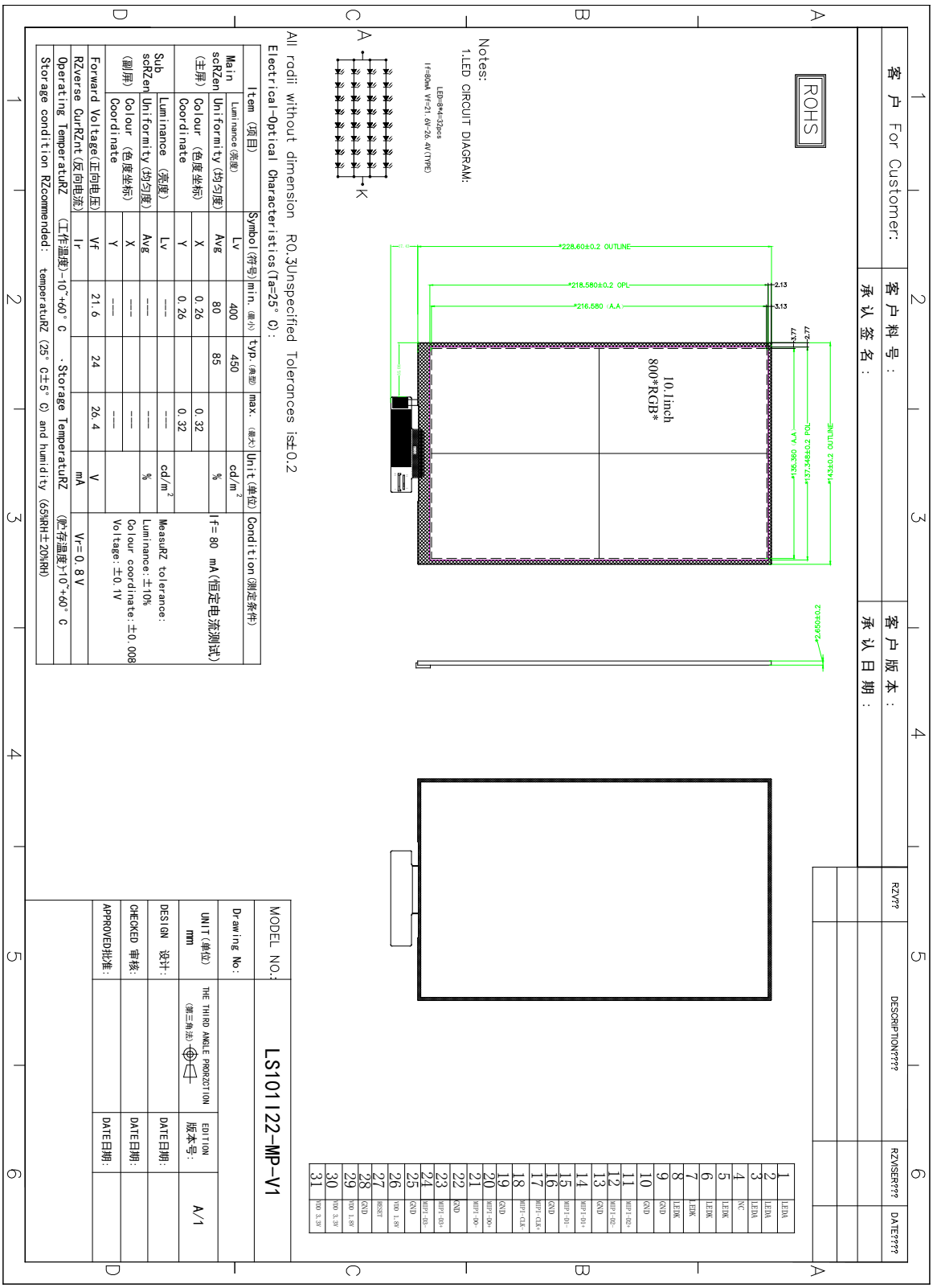
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HS low pulse width	HS	--	6	20	78	DCLK
Horizontal front porch	HFP	--	5	20	78	DCLK
Horizontal back porch	HBP	--	5	20	78	DCLK
Horizontal active area	HDISP	--	--	800	--	DCLK
Vertical Refresh rate	PCLK	--		60 Note(2)		MHz

7.0 Reliability test items

Test Item	Test Conditions	Notes
High temperature Operation	Ta= +60℃, 120hrs	
Low temperature Operation	Ta= -10℃, 120hrs	
High Temperature Storage	Ta= +60℃, 120hrs	
Low Temperature Storage	Ta= -20℃, 120hrs	
Humidity Test	60℃ ,Humidity 90% ,96hrs	
Thermal Shock Test	-10℃,60min～+60℃,60min (30 cycle)	
Vibration Test(Packing)	Frequency: 10Hz~55Hz~10Hz Amplitude:1.5mm, 2 hours for each direction of X, Y, Z	

8.0 OUTLINE DIMENSION

LCM



9.0 Driver IC code

```
REGISTER,FF,03,98,81,03

//GIP_1

REGISTER,01,01,00
REGISTER,02,01,00
REGISTER,03,01,53      //STVA
REGISTER,04,01,00      //STVB
REGISTER,05,01,00      //STVC
REGISTER,06,01,08      //STVA_Rise
REGISTER,07,01,00      //STVB_Rise
REGISTER,08,01,00      //STVC_Rise
REGISTER,09,01,00      //FTI1R(A)
REGISTER,0a,01,00      //FTI2R(B)
REGISTER,0b,01,00      //FTI3R(C)
REGISTER,0c,01,00      //FTI1F(A)
REGISTER,0d,01,00      //FTI2F(B)
REGISTER,0e,01,00      //FTI2F(C)
REGISTER,0f,01,26   //08      //CLW1(ALR) 45%
REGISTER,10,01,26   //08      //CLW2(ARR) 45%
REGISTER,11,01,00
REGISTER,12,01,00
REGISTER,13,01,00      //CLWX(ATF)
REGISTER,14,01,00
REGISTER,15,01,00      //GPMRi(ALR)
REGISTER,16,01,00      //GPMRii(ARR)
REGISTER,17,01,00      //GPMFi(ALF)
REGISTER,18,01,00      //GPMFii(AFF)
REGISTER,19,01,00
REGISTER,1a,01,00
REGISTER,1b,01,00
```

REGISTER,1c,01,00
REGISTER,1d,01,00
REGISTER,1e,01,40 //CLKA`40 笆は C0 も笆は(X8 把σCLKB)
REGISTER,1f,01,C0 //C0
REGISTER,20,01,06 //CLKA_Rise
REGISTER,21,01,01 //CLKA_Fall
REGISTER,22,01,07 //CLKB_Rise(keep toggle 惠昧 CLKA□□□)
REGISTER,23,01,00 //CLKB_Fall
REGISTER,24,01,8A //CLK keep toggle(AL) 8X ┗オ□
REGISTER,25,01,8A //CLK keep toggle(AR) 8X ┗オ□
REGISTER,26,01,00
REGISTER,27,01,00
REGISTER,28,01,33 //3B //CLK Phase
REGISTER,29,01,33 //CLK overlap
REGISTER,2a,01,00
REGISTER,2b,01,00
REGISTER,2c,01,08 //GCH R
REGISTER,2d,01,08 //GCL R
REGISTER,2e,01,0B //GCH F
REGISTER,2f,01,0B //GCL F
REGISTER,30,01,00
REGISTER,31,01,00
REGISTER,32,01,42 //GCH/L ext2/1≪□ 5E 01:31 5E 00:42
REGISTER,33,01,00
REGISTER,34,01,00 //VDD1&2 non-overlap 04:2.62us
REGISTER,35,01,0A //GCH/L 跋丁 00:VS 玾 01:VS□ 10:阁 VS 11:frame い
REGISTER,36,01,00
REGISTER,37,01,08 //GCH/L

```
REGISTER,38,01,3C   //VDD1&2 toggle 1sec
REGISTER,39,01,00
REGISTER,3a,01,00
REGISTER,3b,01,00
REGISTER,3c,01,00
REGISTER,3d,01,00
REGISTER,3e,01,00
REGISTER,3f,01,00
REGISTER,40,01,00
REGISTER,41,01,00
REGISTER,42,01,00
REGISTER,43,01,08      //GCH/L
REGISTER,44,01,00


//GIP_2
REGISTER,50,01,01
REGISTER,51,01,23
REGISTER,52,01,45
REGISTER,53,01,67
REGISTER,54,01,89
REGISTER,55,01,ab
REGISTER,56,01,01
REGISTER,57,01,23
REGISTER,58,01,45
REGISTER,59,01,67
REGISTER,5a,01,89
REGISTER,5b,01,ab
REGISTER,5c,01,cd
REGISTER,5d,01,ef

//GIP_3
```

```
REGISTER,5e,01,00
REGISTER,5f,01,01   //FW_CGOUT_L[1]   VDS
REGISTER,60,01,01   //FW_CGOUT_L[2]   VDS
REGISTER,61,01,06   //FW_CGOUT_L[3]   STV2
REGISTER,62,01,06   //FW_CGOUT_L[4]   STV2
REGISTER,63,01,06   //FW_CGOUT_L[5]   STV4
REGISTER,64,01,06   //FW_CGOUT_L[6]   STV4
REGISTER,65,01,00   //FW_CGOUT_L[7]   VSD
REGISTER,66,01,00   //FW_CGOUT_L[8]   VSD
REGISTER,67,01,17   //FW_CGOUT_L[9]   GCL
REGISTER,68,01,02   //FW_CGOUT_L[10]
REGISTER,69,01,16   //FW_CGOUT_L[11]  GCH
REGISTER,6a,01,16   //FW_CGOUT_L[12]  GCH
REGISTER,6b,01,02   //FW_CGOUT_L[13]
REGISTER,6c,01,0D   //FW_CGOUT_L[14]  CLK8
REGISTER,6d,01,0D   //FW_CGOUT_L[15]  CLK8
REGISTER,6e,01,0C   //FW_CGOUT_L[16]  CLK6
REGISTER,6f,01,0C   //FW_CGOUT_L[17]  CLK6
REGISTER,70,01,0F   //FW_CGOUT_L[18]  CLK4
REGISTER,71,01,0F   //FW_CGOUT_L[19]  CLK4
REGISTER,72,01,0E   //FW_CGOUT_L[20]  CLK2
REGISTER,73,01,0E   //FW_CGOUT_L[21]  CLK2
REGISTER,74,01,02   //FW_CGOUT_L[22]  VGL

REGISTER,75,01,01   //BW_CGOUT_L[1]
REGISTER,76,01,01   //BW_CGOUT_L[2]
REGISTER,77,01,06   //BW_CGOUT_L[3]
REGISTER,78,01,06   //BW_CGOUT_L[4]
REGISTER,79,01,06   //BW_CGOUT_L[5]
REGISTER,7a,01,06   //BW_CGOUT_L[6]
REGISTER,7b,01,00   //BW_CGOUT_L[7]
REGISTER,7c,01,00   //BW_CGOUT_L[8]
```

```
REGISTER,7d,01,17    //BW_CGOUT_L[9]
REGISTER,7e,01,02    //BW_CGOUT_L[10]
REGISTER,7f,01,16    //BW_CGOUT_L[11]
REGISTER,80,01,16    //BW_CGOUT_L[12]
REGISTER,81,01,02    //BW_CGOUT_L[13]
REGISTER,82,01,0D    //BW_CGOUT_L[14]
REGISTER,83,01,0D    //BW_CGOUT_L[15]
REGISTER,84,01,0C    //BW_CGOUT_L[16]
REGISTER,85,01,0C    //BW_CGOUT_L[17]
REGISTER,86,01,0F    //BW_CGOUT_L[18]
REGISTER,87,01,0F    //BW_CGOUT_L[19]
REGISTER,88,01,0E    //BW_CGOUT_L[20]
REGISTER,89,01,0E    //BW_CGOUT_L[21]
REGISTER,8A,01,02    //BW_CGOUT_L[22]



//CMD_Page 4
REGISTER,FF,03,98,81,04

REGISTER,6E,01,2B        /VGH 15V
REGISTER,6F,01,35     //37              // reg vcl + pumping ratio
VGH=3x VGL=-2.5x
REGISTER,3A,01,A4        //POWER SAVING
REGISTER,8D,01,1A        //VGL -11V
REGISTER,87,01,BA        //ESD
REGISTER,B2,01,D1
REGISTER,88,01,0B
REGISTER,38,01,01
REGISTER,39,01,00
REGISTER,B5,01,07        //gamma bias
REGISTER,31,01,75
```

```
REGISTER,3B,01,98

//CMD_Page 1
REGISTER,FF,03,98,81,01
REGISTER,22,01,0A        //BGR, SS
REGISTER,31,01,00        //Column inversion
REGISTER,53,01,40        //VCOM1
REGISTER,55,01,40        //VCOM2
REGISTER,50,01,95        //VREG1OUT 4.5V
REGISTER,51,01,90        //VREG2OUT -4.5V
REGISTER,60,01,22    //06        //SDT
REGISTER,62,01,20
//============Gamma START=============

//Pos Register
REGISTER,A0,01,00
REGISTER,A1,01,1B
REGISTER,A2,01,2A
REGISTER,A3,01,14
REGISTER,A4,01,17
REGISTER,A5,01,2B
REGISTER,A6,01,1F
REGISTER,A7,01,20
REGISTER,A8,01,93
REGISTER,A9,01,1E
REGISTER,AA,01,2A
REGISTER,AB,01,7E
REGISTER,AC,01,1B
REGISTER,AD,01,19
REGISTER,AE,01,4C
REGISTER,AF,01,22
REGISTER,B0,01,28
```

REGISTER,B1,01,4B
REGISTER,B2,01,59
REGISTER,B3,01,23

//Neg Register
REGISTER,C0,01,00
REGISTER,C1,01,1B
REGISTER,C2,01,2A
REGISTER,C3,01,14
REGISTER,C4,01,17
REGISTER,C5,01,2B
REGISTER,C6,01,1F
REGISTER,C7,01,20
REGISTER,C8,01,93
REGISTER,C9,01,1E
REGISTER,CA,01,2A
REGISTER,CB,01,7E
REGISTER,CC,01,1B
REGISTER,CD,01,19
REGISTER,CE,01,4C
REGISTER,CF,01,22
REGISTER,D0,01,28
REGISTER,D1,01,4B
REGISTER,D2,01,59
REGISTER,D3,01,23

//========== Gamma END==========

//CMD_Page 0
REGISTER,FF,03,98,81,00
REGISTER,11,01,00
Delay,120
REGISTER,29,01,00
REGISTER,35,01,00

10. General precaution

10.1 Use Restriction

This product is not authorized for use in life supporting systems, aircraft navigation control systems, military systems and any other application where performance failure could be life threatening or otherwise catastrophic.

10.2 Disassembling or Modification

Do not disassemble or modify the module. It may damage sensitive parts inside LCD module, and may cause scratches or dust on the display. RFH does not warrant the module, if customers disassemble or modify the module.

10.3 Breakage of LCD Panel

10.3.1.If LCD panel is broken and liquid crystal spills out, do not ingest or inhale liquid crystal, and do not contact liquid crystal with skin.

10.3.2. If liquid crystal contacts mouth or eyes, rinse out with water immediately.

10.3.3. If liquid crystal contacts skin or cloths, wash it off immediately with alcohol and rinse thoroughly with water.

10.3.4. Handle carefully with chips of glass that may cause injury, when the glass is broken.

10.4 Electric Shock

10.4.1. Disconnect power supply before handling LCD module.

10.4.2. Do not pull or fold the LED cable.

10.4.3. Do not touch the parts inside LCD modules and the fluorescent LED's connector or cables in order to prevent electric shock.

10.5 Absolute Maximum Ratings and Power Protection Circuit

10.5.1. Do not exceed the absolute maximum rating values, such as the supply voltage variation, input voltage variation, variation in parts' parameters, environmental temperature, etc., otherwise LCD module may be damaged.

10.5.2. Please do not leave LCD module in the environment of high humidity and high temperature for a long time.

10.5.3. It's recommended to employ protection circuit for power supply.

10.6 Operation

10.6.1 Do not touch, push or rub the polarizer with anything harder than HB pencil lead.

10.6.2 Use finger stalls of soft gloves in order to keep clean display quality, when persons handle the LCD module for incoming inspection or assembly.

10.6.3 When the surface is dusty, please wipe gently with absorbent cotton or other soft material.

10.6.4 Wipe off saliva or water drops as soon as possible. If saliva or water drops contact with polarizer for a long time, they may causes deformation or color fading.

10.6.5 When cleaning the adhesives, please use absorbent cotton wetted with a little petroleum benzine or other

adequate solvent.

10.7 Mechanism

Please mount LCD module by using mouting holes arranged in four corners tightly.

10.8 Static Electricity

10.8.1 Protection film must remove very slowly from the surface of LCD module to prevent from electrostatic occurrence.

10.8.2. Because LCD module use CMOS-IC on circuit board and TFT-LCD panel, it is very weak to electrostatic discharge. Please be careful with electrostatic discharge. Persons who handle the module should be grounded through adequate methods.

10.9 Strong Light Exposure

The module shall not be exposed under strong light such as direct sunlight. Otherwise, display characteristics may be changed.