PRODUCT SPECIFICATION FOR LCD MODULE

Revision: 1.0

Model No: LSC1010I09-MP-V1

Module Type: COG+FPC+B/L+CTP

APPROVED SIGNATURE

■ Approved Product Specification only

□ Approved Product Specification and Samples

Prepared By	Checked By	Approved By

Contents

目录

1. General Description

LSC1010I09-MP-V1 is 10.1" color TFT -LCD (Thin Film Transistor Liquid Crystal Display) module composed of LCD panel , driver ICs ,control circuit, Utilizes a panel with a 16:10 aspect ratio. The 10.1"screen produces a high resolution image that is composed of 2560x1600 pixel elements in a stripe arrangement.

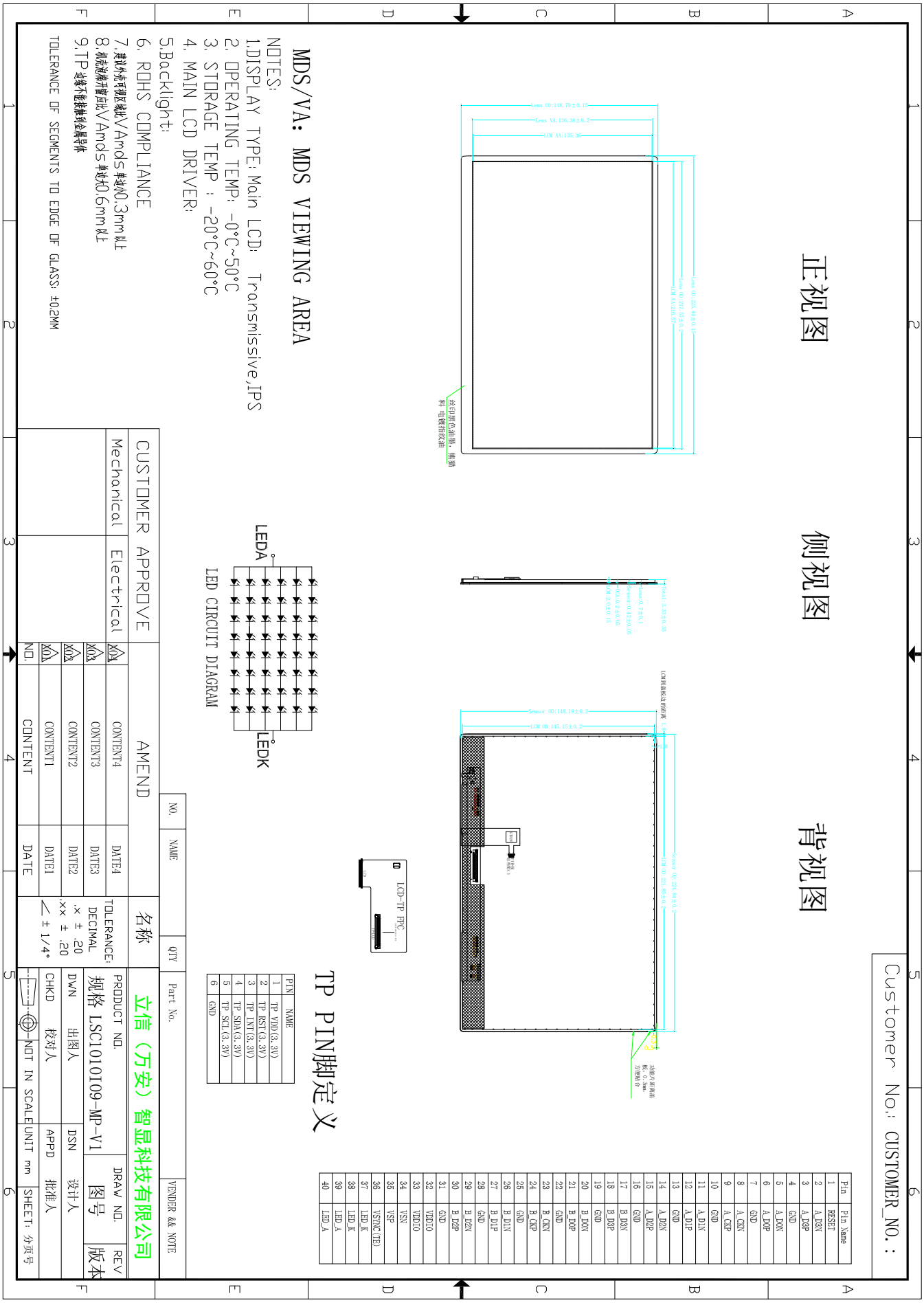
2. Physical Features

Display Mode	TFT-LCD Module
	Active matrix TFT, Transmissive type
Display Format	Graphic 2560(RGB)×1600 Dot-matrix
Input Data	MIPI
Viewing Direction （Grayscale Inversion）	Free（IPS）

3. Mechanical Specification

Item	Specification	Unit
Module size (H×V×D)	225.44 ×148.79 ×3.33	mm
Number of dots	2560(RGB) ×1600	pixel
Active area (H×V)	216.58×135.36	mm

4. Outline Dimension



5. Absolute Maximum Ratings

Item	Symbol	Min	Max	Unit	Remark
Supply voltage	VSP	-0.3	6.5	V	VSP-GND
Supply voltage	VSN	-0.3	6.5	V	GND-VSN
Supply voltage	IOVCC	-0.3	4.6	V	IOVCC-GND
Operating temperature	TOPR	0	50	℃	no dew condition
Storage temperature	TSTR	-20	60	℃	

6. Electrical Characteristics

Parameter	Symbol	Condition	Ratings			Unit	Pins
			Min.	Typ.	Max.		
Power supply voltage	VSP		5.3	5.4	5.5	V	
Power supply voltage	VSN		-5.5	-5.4	-5.3	V	
Power supply voltage	IOVCC		1.7	1.8	1.9	V	
Low-level input voltage	VIL		0	-	0.3 x IOVCC	V	
High-level input voltage	VIH		0.7 x IOVCC	-	IOVCC	V	
Low-level output voltage	VOL	IOUT=+1mA	0.0	-	0.2 x IOVCC	V	
High-level output voltage	VOH	IOUT=-1mA	0.8 x IOVCC	-	IOVCC	V	
Power supply current(CTF)	IVSP		12	17	32	mA	VSP
(RMS)	IVSN		-18	-16	-10	mA	VSN
*2) *3)	IIOVCC		31	34	90	mA	IOVCC

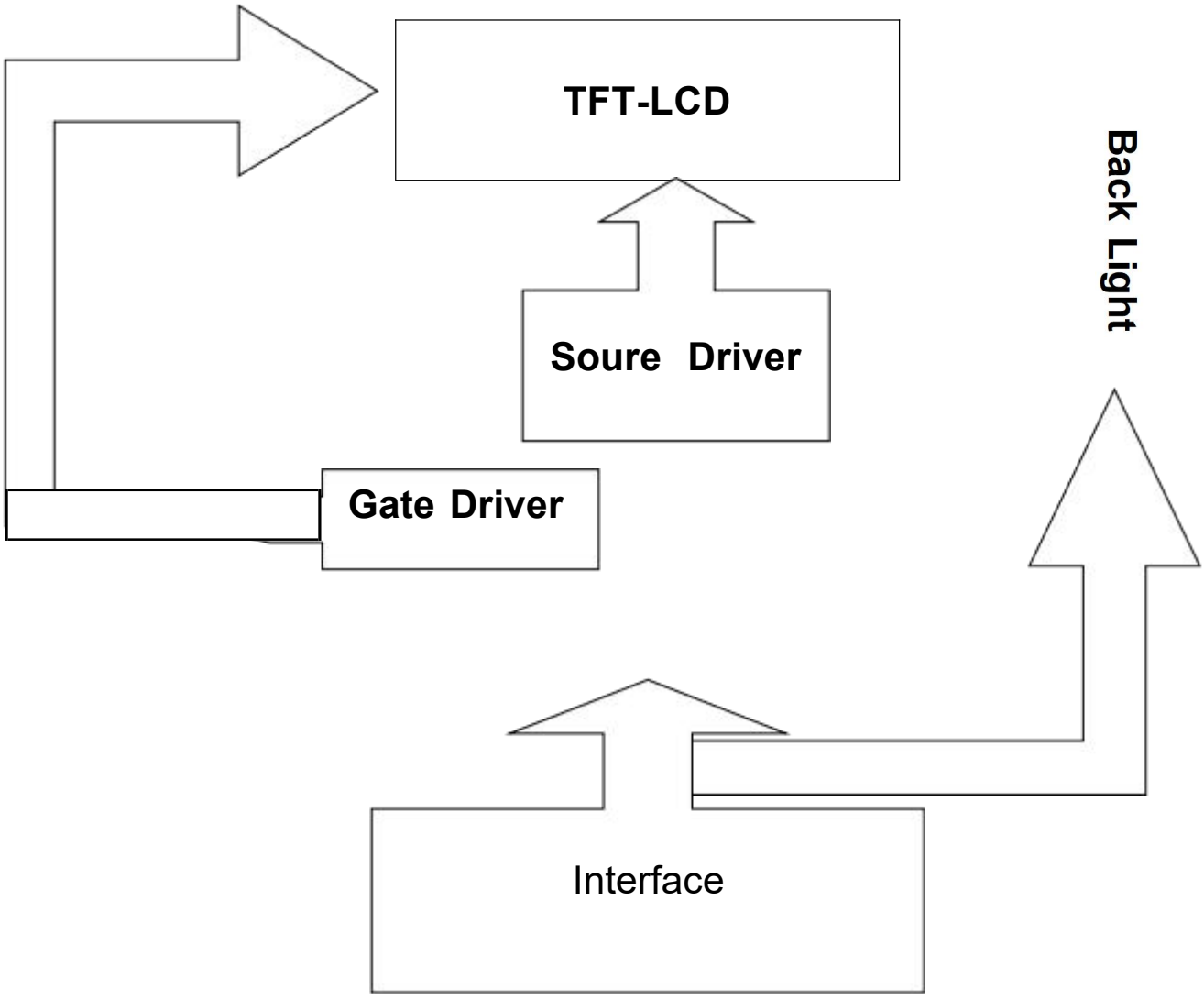
ELECTRICAL CHARACTERISTICS

Ta=25℃

ITEM	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
LED Total Iuput Voltage	VLED	22.4	24	25.6	V	
LED Total Input Current	IBL+	-	120	-	mA	

7. Module Function Description

7-1. Block Diagram Of LCM



7-2. Pin Description

CONNECTOR (FH34SRJ-40S-0.5SH(50))

PIN	SYMBOL	FUNCTION	I/O	REMARKS
1	RESET	Reset Signal	I	Left/Right DSI
2	MIPI_3N_A	MIPI Negative data signal (-)	I	Left DSI
3	MIPI_3P_A	MIPI Positive data signal (+)	I	Left DSI
4	GND	GROUND	P	
5	MIPI_0N_A	MIPI Negative data signal (-)	I/O	Left DSI
6	MIPI_0P_A	MIPI Positive data signal (+)	I/O	Left DSI
7	GND	GROUND	P	
8	MIPI_CKN_A	MIPI Negative data signal (-)	I	Left DSI
9	MIPI_CKP_A	MIPI Positive data signal (+)	I	Left DSI
10	GND	GROUND	P	
11	MIPI_1N_A	MIPI Negative data signal (-)	I	Left DSI
12	MIPI_1P_A	MIPI Positive data signal (+)	I	Left DSI
13	GND	GROUND	P	
14	MIPI_2N_A	MIPI Negative data signal (-)	I	Left DSI
15	MIPI_2P_A	MIPI Positive data signal (+)	I	Left DSI
16	GND	GROUND	P	
17	MIPI_3N_B	MIPI Negative data signal (-)	I	Right DSI
18	MIPI_3P_B	MIPI Positive data signal (+)	I	Right DSI
19	GND	GROUND	P	
20	MIPI_0N_B	MIPI Negative data signal (-)	I/O	Right DSI
21	MIPI_0P_B	MIPI Positive data signal (+)	I/O	Right DSI
22	GND	GROUND	P	
23	MIPI_CKN_B	MIPI Negative data signal (-)	I	Right DSI
24	MIPI_CKP_B	MIPI Positive data signal (+)	I	Right DSI
25	GND	GROUND	P	
26	MIPI_1N_B	MIPI Negative data signal (-)	I	Right DSI
27	MIPI_1P_B	MIPI Positive data signal (+)	I	Right DSI
28	GND	GROUND	P	
29	MIPI_2N_B	MIPI Negative data signal (-)	I	Right DSI
30	MIPI_2P_B	MIPI Positive data signal (+)	I	Right DSI
31	GND	GROUND	P	
32	VDDIO	Power Supply for I/O block	P	
33	VDDIO	Power Supply for I/O block	P	
34	VSN	Power Supply for Analog Circuit	P	
35	VSP	Power Supply for Analog Circuit	P	
36	VSYCN	Tearing Effect Output	O	Right DSI
37	LED_K	LED cathode	P	
38	LED_K	LED cathode	P	
39	LED_A	LED anode	P	
40	LED_A	LED anode	P	

Note) P : Power supply I : Input O : Output

7-3 Timing Characteristics

4.2.1 MIPI DSI characterisitics

Item		Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
HS-RX	Differential input high threshold	VIDTH	mV	VDDIO=1.70V～1.90V	-	-	70	3
	Differential input low threshold	VIDTL	mV	VDDIO=1.70V～1.90V	-70	-	-	3
	Single-ended input low voltage	VILHS	mV	VDDIO=1.70V～1.90V	-40	-	-	
	Single-ended input high voltage	VIHHS	mV	VDDIO=1.70V～1.90V	-	-	460	
	Common-mode voltage HS receive mode	VCMRX(DC)	mV	VDDIO=1.70V～1.90V	70	-	330	1
	Differential input impedance	ZID	Ω	VDDIO=1.70V～1.90V	-	100	-	2
LP-RX	Logic 0 input voltage not in ULP State	VIL	mV	VDDIO=1.70V～1.90V	-50	-	550	
	Logic 1 input voltage	VIH	mV	VDDIO=1.70V～1.90V	880	-	1350	
	I/O leakage current	ILEAK	μA	Vin=-50mV～1350mV	-10	-	10	
LP-TX	Thevenin output low level	VOL	mV	VDDIO=1.70V～1.90V	-50	-	50	
	Thevenin output high level	VOH	V	VDDIO=1.70V～1.90V	1.1	1.2	1.3	
	Output impedance of LP transmitter	ZOLP	Ω	VDDIO=1.80V	110	-	-	2
CD-RX	Logic 0 contention threshold	VILCD	mV	VDDIO=1.70V～1.90V	-	-	200	
	Logic 1 contention threshold	VIHCD	mV	VDDIO=1.70V～1.90V	450	-	-	

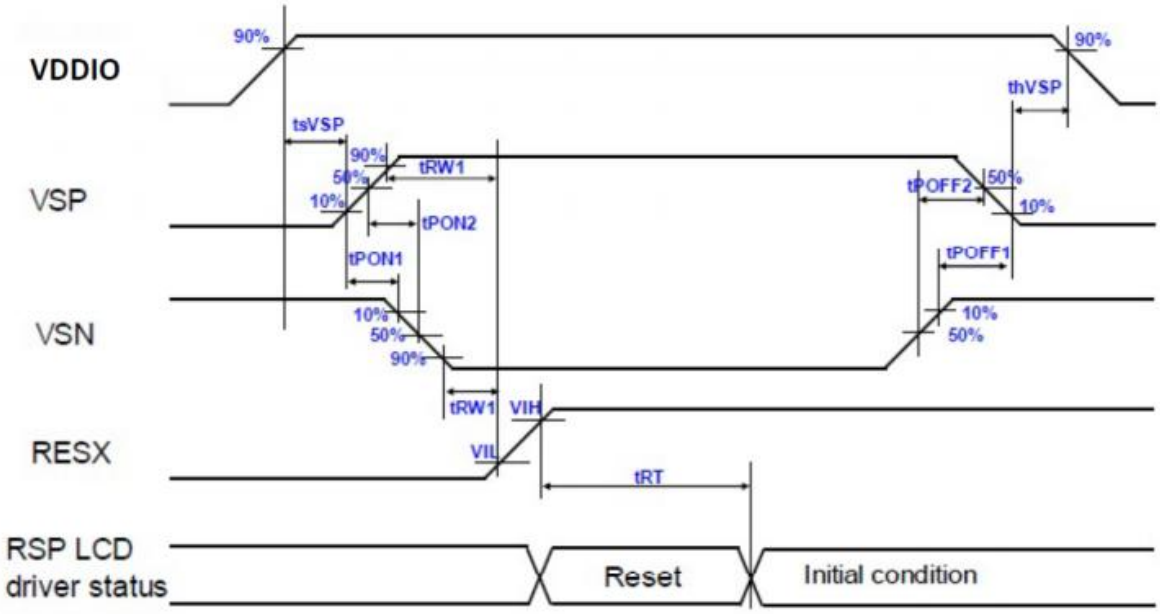
Note 1) VCMRX(DC) = (VDP+VDN)/2

Note 2) Excluding COG registance (contact resistance and ITO wiring resistance).The values are tentative.

Note 3) Minimum 110mV/-110mV HS differential swing is required for display data transfer.

4.3.1 Power On/Off operation and reset operation and Reset Timming

Power Supply Sequence



Item	Symbol	Unit	Test Condition	Min	Max
VSP-VSN delay time (10% to 10%)	tPON1	us	Power On	0	-
VSP-VSN delay time (50% to 50%)	tPON2	us	Power On	0	-
System power on to VSP ON time	tsVSP	ms	Power On	1	-
Reset low-level width1	tRW1	ms	Power On	10	-
Reset time(Sleep IN)	tRT	ms	Power On	10	-
VSN-VSP delay time (10% to 10%)	tPOFF1	us	Power Off	0	-
VSN-VSP delay time (50% to 50%)	tPFF2	us	Power Off	0	-
VSP OFF to system power off time	thVSP	us	Power Off	0	-

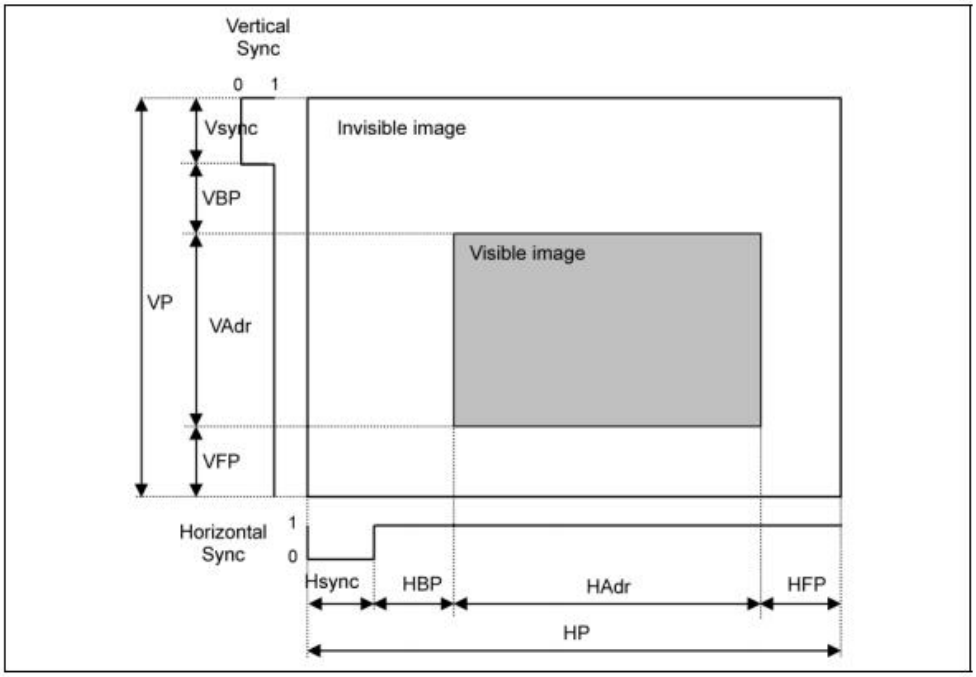
4.3.2 Timing Chart

Video Mode

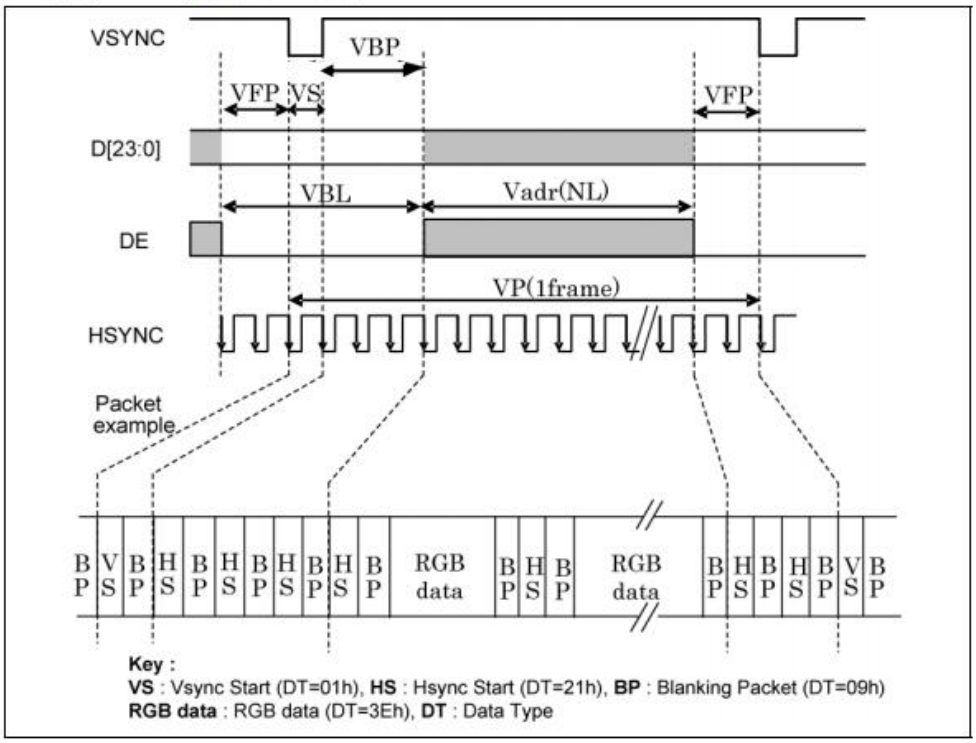
The RSP LCD driver supports Video Mode for moving pictures. There are three formats of transmission packet sequences. The RSP LCD driver supports two of these formats. See the following table.

Transmission packet sequence in video mode	RSP LCD driver implementation
Non-burst mode with sync pulses	Supported
Non-burst mode with sync events	Not Supported
Burst mode	Supported

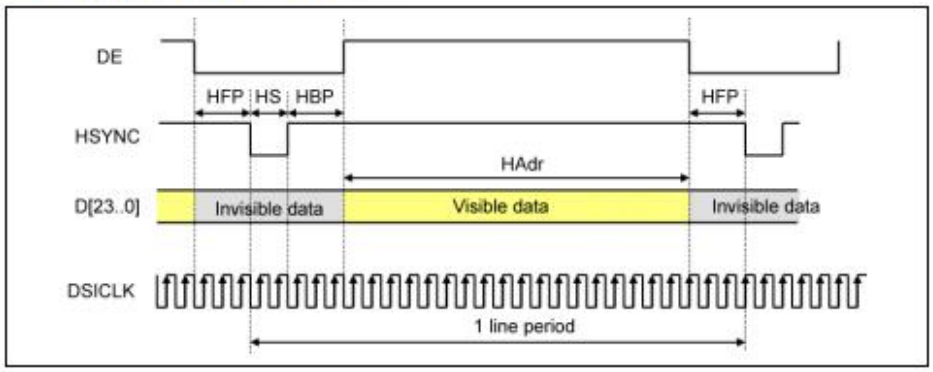
Display Timing (Video Mode)



Vertical Display Timing (Video Mode)



Horizontal Display Timing (Video Mode)



Vertical Display Timing (Video Mode, RM = 1h, DM = 3h, Method-1)

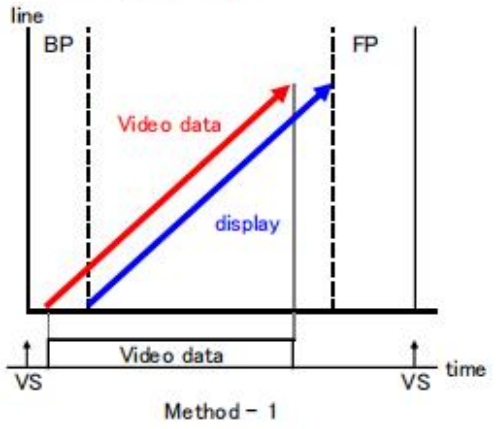
Item	Symbol	Condition	Unit	Min.	Typ.	Max.	Notes
Vertical cycle	VP		Line	1608	1616	-	
Vertical low pulse width	VS		Line	1	3	-	See
Vertical front porch	VFP		Line	4	7	-	
Vertical back porch	VBP		Line	4	6	BP-3	See
Vertical data start point	VBP	VS+VBP	Line	5	9	BP-4	See
Vertical blanking period	VBL	VBP+VFP	Line	8	13	-	
Vertical active area	Vadr		Line	-	1600	-	

Note: "VS + VBP" is set as back porch by BP register.
1 line : prescribed by HSYNC (when RM = 2'h0, DM = 4'h1)
prescribed by RTN setting (whenRM = 2'h1, DM = 4'h3)
BP : register setting

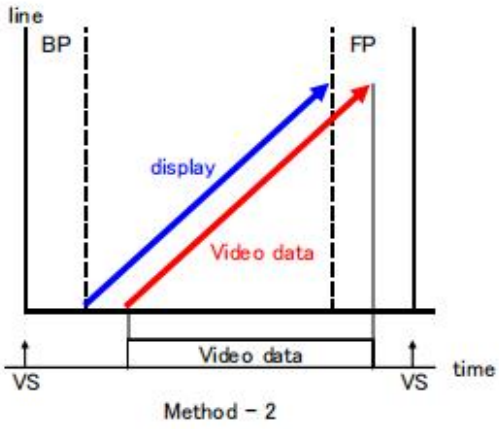
Vertical Display Timing (Video Mode, RM = 1h, DM = 3h, Method-2)

Item	Symbol	Condition	Unit	Min.	Typ.	Max.	Notes
Vertical cycle	VP		Line	1608	1616	-	
Vertical low pulse width	VS		Line	1	3	-	See
Vertical front porch	VFP		Line	4	7	-	
Vertical back porch	VBP		Line	BP+3	6	-	See
Vertical data start point	VBP	VS+VBP	Line	BP+4	9	-	See
Vertical blanking period	VBL	VBP+VFP	Line	BP+7	13	-	See
Vertical active area	Vadr		Line	-	1600	-	

Note: "VS + VBP" is set as back porch by BP register.
1 line : prescribed by HSYNC (when RM = 2'h0, DM = 4'h1)
prescribed by RTN setting (whenRM = 2'h1, DM = 4'h3)
BP : register setting



Method − 1



Method − 2

Horizontal Display Timing (Video Mode, RM = 1h, DM = 3h)

Item	Symbol	Condition	Unit	Min.	Typ.	Max.	Notes
Horizontal front porch	HFP		ByteClock	4lane:100+β	-	-	
Horizontal data start point	-	HS+HBP	ByteClock	45+α	-	-	
Horizontal active area	Hadr		Pixel	-	1280	-	2Chip

Note: fByteClock = (1/4) * fDSICLK. fByteClock = frequency of ByteClock.
α, β ≦ 45 ByteClock
Please refer to the following restrictions about α, β.

Vertical Display Timing (Video Mode, DM = 1h)

Item	Symbol	Condition	Unit	Min.	Typ.	Max.	Notes
Vertical cycle	VP		Line	1608	1616	-	
Vertical low pulse width	VS		Line	1	3	-	See
Vertical front porch	VFP		Line	4	7	-	
Vertical back porch	VBP		Line	4	6	-	See
Vertical data start point	VBP	VS+VBP	Line	5	9	-	
Vertical blanking period	VBL	VBP+VFP	Line	8	13	-	
Vertical active area	Vadr		Line	-	1600	-	

Note: "VS + VBP" is set as back porch by BP register.
1 line : prescribed by HSYNC (when RM = 2'h0, DM = 4'h1)
prescribed by RTN setting (when RM = 2'h1, DM = 4'h3)

Horizontal Display Timing (Video Mode, RM = 0h, DM = 1h)

Item	Symbol	Condition	Unit	Min.	Typ.	Max.	Notes
Horizontal front porch	HFP		ByteClock	4lane:100+β	-	-	
Horizontal data start point	-	HS+HBP	ByteClock	45+α	-	-	
Horizontal active area	Hadr		Pixel	-	1280	-	2Chip

Note: fByteClock = (1/4) * fDSICLK. fByteClock = frequency of ByteClock.
α, β ≦ 45 ByteClock
Please refer to the following restrictions about α, β.

Timing restrictions in Video mode of Two Chips

The blanking period is specified for the pixel data transfer to the two chips in Video Mode.
Set 45 ByteClock or less in the time that the pixel data transfer to the Second(Salve) chip precedes and is behind the pixel data transfer to the First(Master) chip.

α: Time the pixel data is transferred to the Second(Slave) chip(CPUS=1, CPPOS=1) precedes time the pixel data is transferred to the First(Master) chip(CPUS=1, CPPOS=0).

β: Time the pixel data is transferred to the Second(Slave) chip(CPUS=1, CPPOS=1) is behind time the pixel data is transferred to the First(Master) chip(CPUS=1, CPPOS=0).

4.3.3 Power On Sequence

Step	DataTyp (Hex)	index (Hex)	Parameter (Hex)	Delay	L/R	Command
1						Power Supply (VDDIO=1.8V)
2				5ms		
3						Power Supply (VSP=5.4V)
4				8ms		
5						Power Supply (VSN=-5.4V)
6				10ms		
7						RESET L→H (100ms)→L(200ms)→H
8				200ms		
9	23	0xB0	0x00		L/R	MCAP
10	23	0XD6	0x01		L/R	T_SLPOUT=0(NVM load stop)
11	29	0XB3	0x14		L/R	Interface setting
			0x08			
			0x00			
			0x22			
			0x00			
11				100ms		
12	05	0X29			L/R	Display on
13	05	0X11				Sleep out
14				100ms		
15						Backlight turn on

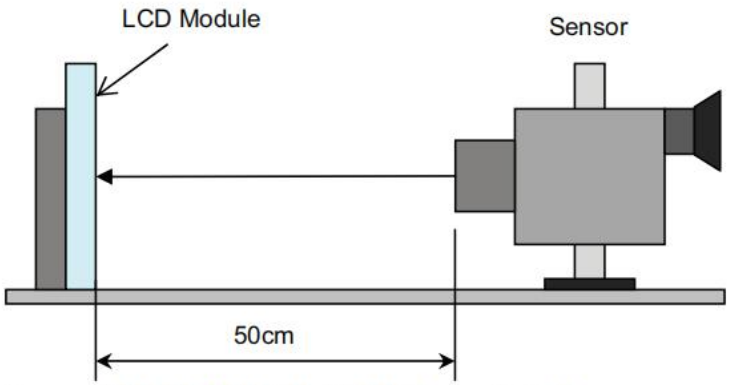
4.3.3 Power Off Sequence

Step	DataTyp (Hex)	index (Hex)	Parameter (Hex)	Delay	L/R	Command
1						Backlight turn off
2				100ms		
3	05	0x28			L/R	Display off
4				100ms		
7	05	0x10			L/R	Sleep in
8				150ms		
9						Power off

8. Electro-Optical Characteristics

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Notes
Brightness		B	φ=0°, θ=0°	400	(450)	-	Cd/m2	(1),(2)
Viewing Angle on axis	φ=0	θ	CR>10	(80)	-	-	degree	(3),(4)
	φ=90							
	φ=180							
	φ=270							
Contrast Ratio		CR	φ=0°, θ=0°	-	(1200)	-	-	(5)
Color Gamut CIE 1931 (Primary Color)	Red	x	φ=0°, θ=0°	-	0.6379	-	-	-
		y		-	0.3393	-		
	Green	x		-	0.3179	-		
		y		-	0.647	-		
	Blue	x		-	0.1502	-		
		y		-	0.0461	-		
	White	x		-	0.2911	-		
		y		-	0.3082	-		
NTSC Ratio (CIE1931)		-	φ=0°, θ=0°	-	(77)	-	-	
Gamma Curve		-	φ=0°, θ=0°	-	(2.2)	-	-	
Cross Talk		CT	-	-	-	(4)	%	(6)

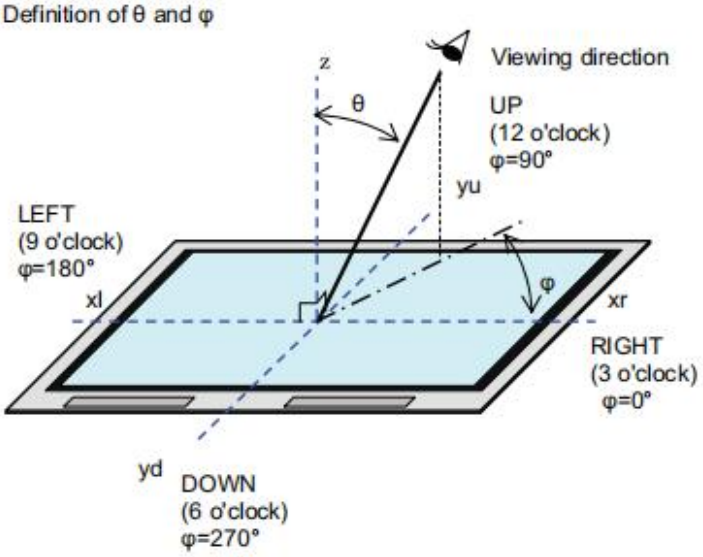
otes (1) Definition of Brightness "B". At the Center of Active Area.



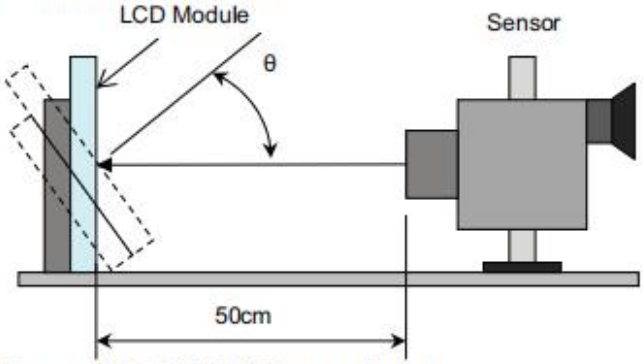
Sensor : KONICA MINOLTA CS-1000 or equivalent

(2) Display image for measurement : All White

(3) Definition of θ and φ



(4) Definition of Viewing Angle θ



Sensor : TOPCON's BM-5A or equivalent

(5) Definition of Contrast "CR"

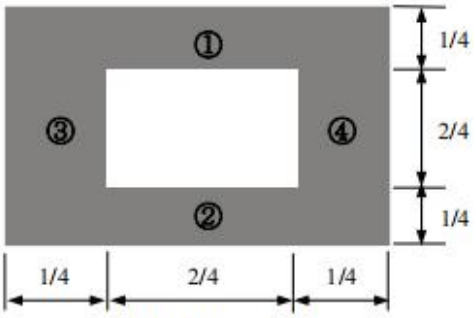
CR = (Brightness when displaying White raster) / (Brightness when displaying Black raster)

(6) Definition of Cross Talk "CT"

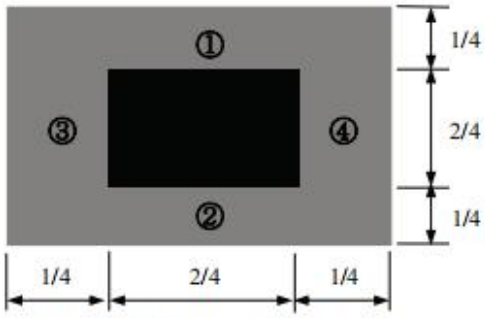
CT = {(Brightness [Cross-talk pattern]) – (Brightness [127Gray])} / (Brightness [127Gray]) x 100(%)

Measurement pattern :
- Cross talk pattern 1 : White box
- Cross talk pattern 2 : Black box

Measurement Point :
- Vertical Crosstalk : ① and ②
- Horizontal Crosstalk : ③ and ④



Cross talk pattern 1 : White box



Cross talk pattern 2 : Black box

9.Records Of Version

Version	Revise Date	Page	Content
00		ALL	New released