PRODUCT SPECIFICATION FOR LCD MODULE

Revision: 1.0

Model No: LS1330I01-E-V1

Module Type: COG+B/L+PCBA

APPROVED SIGNATURE

■ Approved Product Specification only

□ Approved Product Specification and Samples

Prepared By	Checked By	Approved By

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1. General Description

LS1330I01-E-V1 is a color active matrix TFT LCD module using amorphous silicon TFT's (Thin Film Transistors) as an active switching devices. This module has a 13.3inch diagonally measured active area with WUXGA resolutions (1920 horizontal by 1200 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe and this module can display 8bit colors and color gamut sRGB 100%. The TFT-LCD panel used for this module is a low reflection and higher color type.

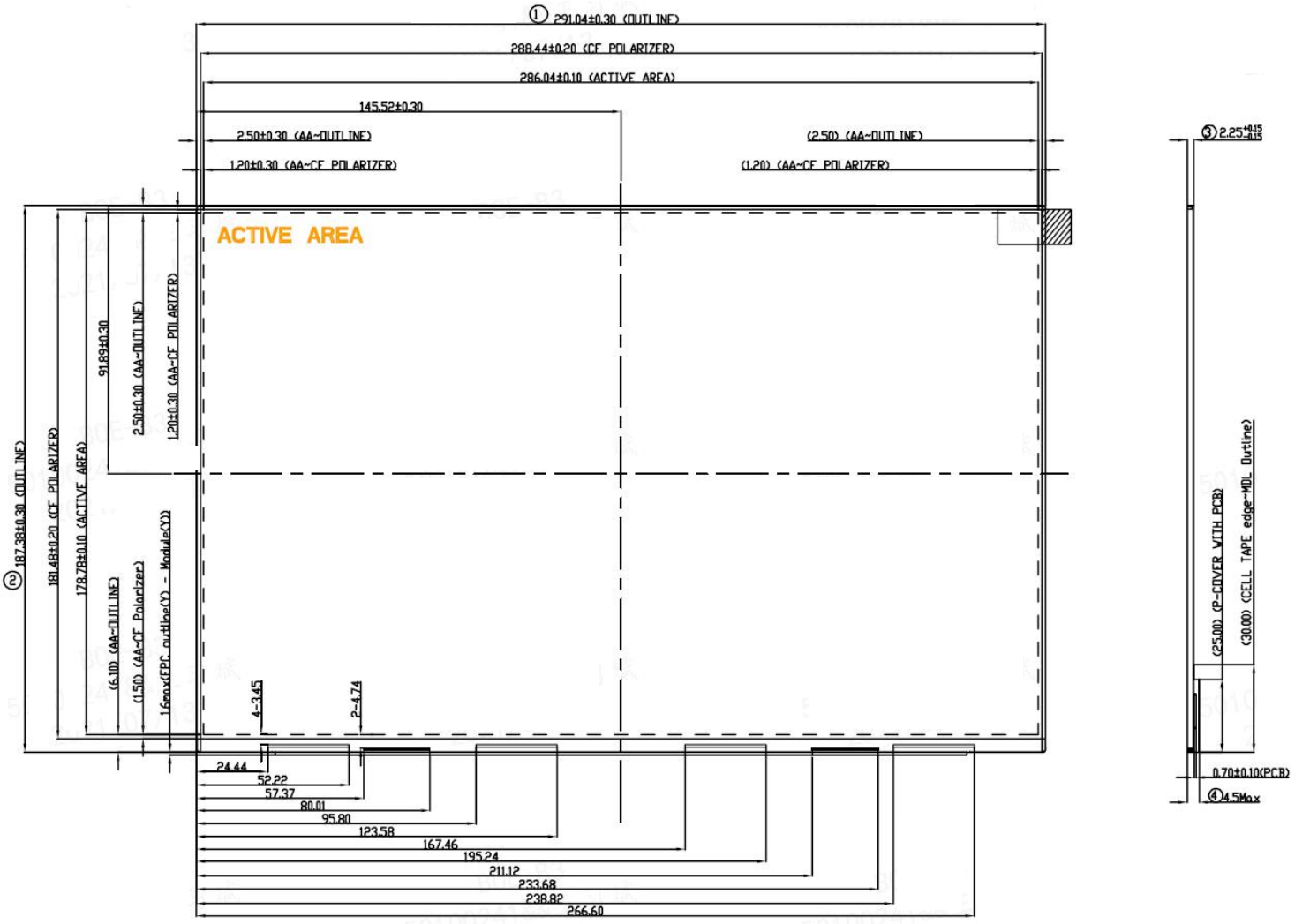
2. Physical Features

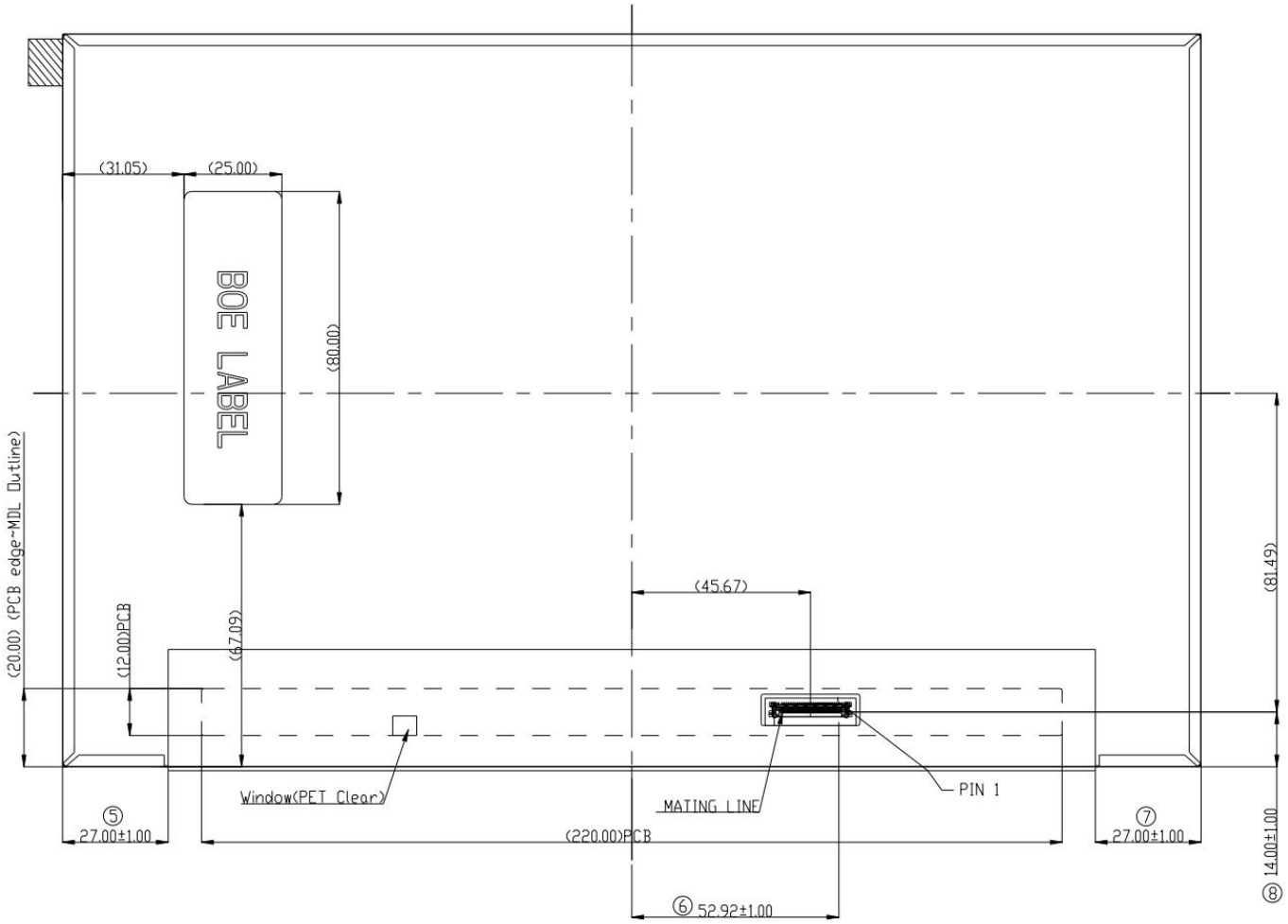
Display Mode	TFT-LCD Module
	Active matrix TFT, Transmissive type
Display Format	Graphic 1920(RGB)×1200 Dot-matrix
Input Data	eDP
Viewing Direction （Grayscale Inversion）	Free（IPS）

3. Mechanical Specification

Item	Specification	Unit
Module size (H×V×D)	291.04 ×187.38 ×2.25	mm
Number of dots	1920(RGB) ×1200	pixel
Active area (H×V)	286.042×178.776	mm

4. Outline Dimension




(31.05)
(25.00)
BOE LABEL
(80.00)
(20.00) (PCB edge~MDL Outline)
(12.00)PCB
(67.09)
(45.67)
(81.49)
Window(PET Clear)
MATING LINE
PIN 1
⑤ 27.00±1.00
(220.00)PCB
⑦ 27.00±1.00
⑥ 52.92±1.00
⑧ 14.00±1.00

5. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Remarks
Power Supply Voltage	V_{DD}	-0.3	4.0	V	Note 1
eDP input Voltage	V_{eDP}	0	2.0	V	
Logic Supply Voltage	V_{IN}	V_{SS}-0.3	V_{DD}+0.3	V	
Operating Temperature	T_{OP}	0	+50	°C	Note 2
Storage Temperature	T_{ST}	-20	+60	°C	

Notes :
1. Permanent damage to the device may occur if maximum values are exceeded functional operation should be restricted to the condition described under normal operating conditions.

6. Electrical Characteristics

Parameter			Min.	Typ.	Max.	Unit	Remarks
Power Supply Voltage		V_{DD}	3.0	3.3	3.6	V	Note 1
Permissible Input Ripple Voltage		V_{RF}	-10% VDD	-	+10% VDD	V	Note 4
BIST Control Level		High Level	0.8 VDDIO	-	3.3	V	@V_{DDIO}=1.8
		Low Level	0	-	0.15 VDDIO	V	
Power Supply Inrush Current		Inrush	-	-	2	A	Note3
Power Supply Current	Mosaic	I_{DD}	-	-	166	mA	Note 1
	RGB		-	-	-	mA	
	Solid		-	-	-	mA	
Power Consumption	Mosaic	P_M	-	-	0.5	W	
	RGB	P_{RGB}	-	-	-	W	
	Solid	P_S	-	-	-	W	
	BLU	P_{BL}	-	-	2.62	W	Note 2
	Total	P_{Total}	-	-	3.12	W	@Mosaic

7. Backlight Unit

Parameter			Min.	Typ.	Max.	Unit	Remarks
LED Forward Voltage		V_F	-	-	2.85	V	
LED Forward Current		I_F	-	13	-	mA	
LED Power Input Voltage		V_{LED}	5	12	21	V	
LED Power Input Current		I_{LED}	-	-	218	mA	Note 1
LED Power Consumption		P_{LED}	-	-	2.62	W	
Power Supply Voltage for LED Driver Inrush		Iled inrush	-	-	1.5	A	Note 3
LED Life-Time		N/A	15,000	-	-	Hour	I_F = 20mA Note 2
EN Control Level	Backlight On	V_{BL_EN}	2.5	-	5.0	V	
	Backlight Off		0	-	0.5	V	
PWM Control Level	High Level	V_{BL_PWM}	2.5	-	5.0	V	
	Low Level		0	-	0.5	V	
PWM Control Frequency		F_{PWM}	200	-	2,000	Hz	
Duty Ratio			5	-	100	%	

Notes :

1. Power supply voltage12V for LED driver.
   Calculator value for reference IF × VF ×54/driver efficiency = PLED
2. The LED life-time define as the estimated time to 50% degradation of initial luminous.
3. Measure condition (Figure 5)

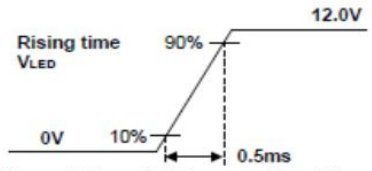
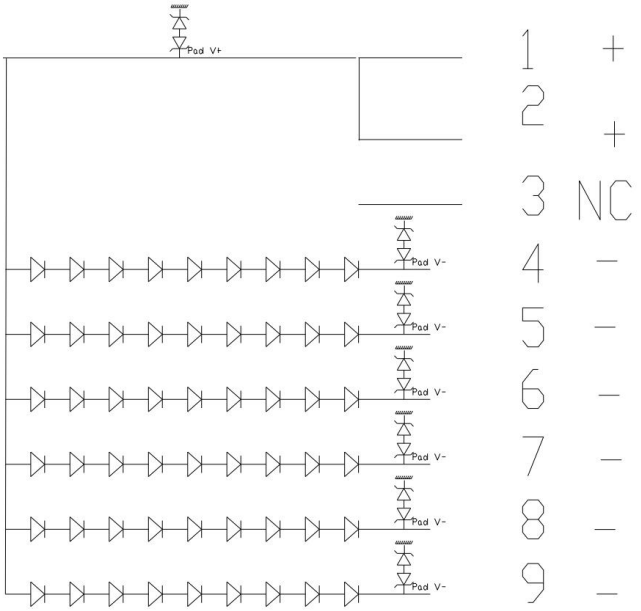
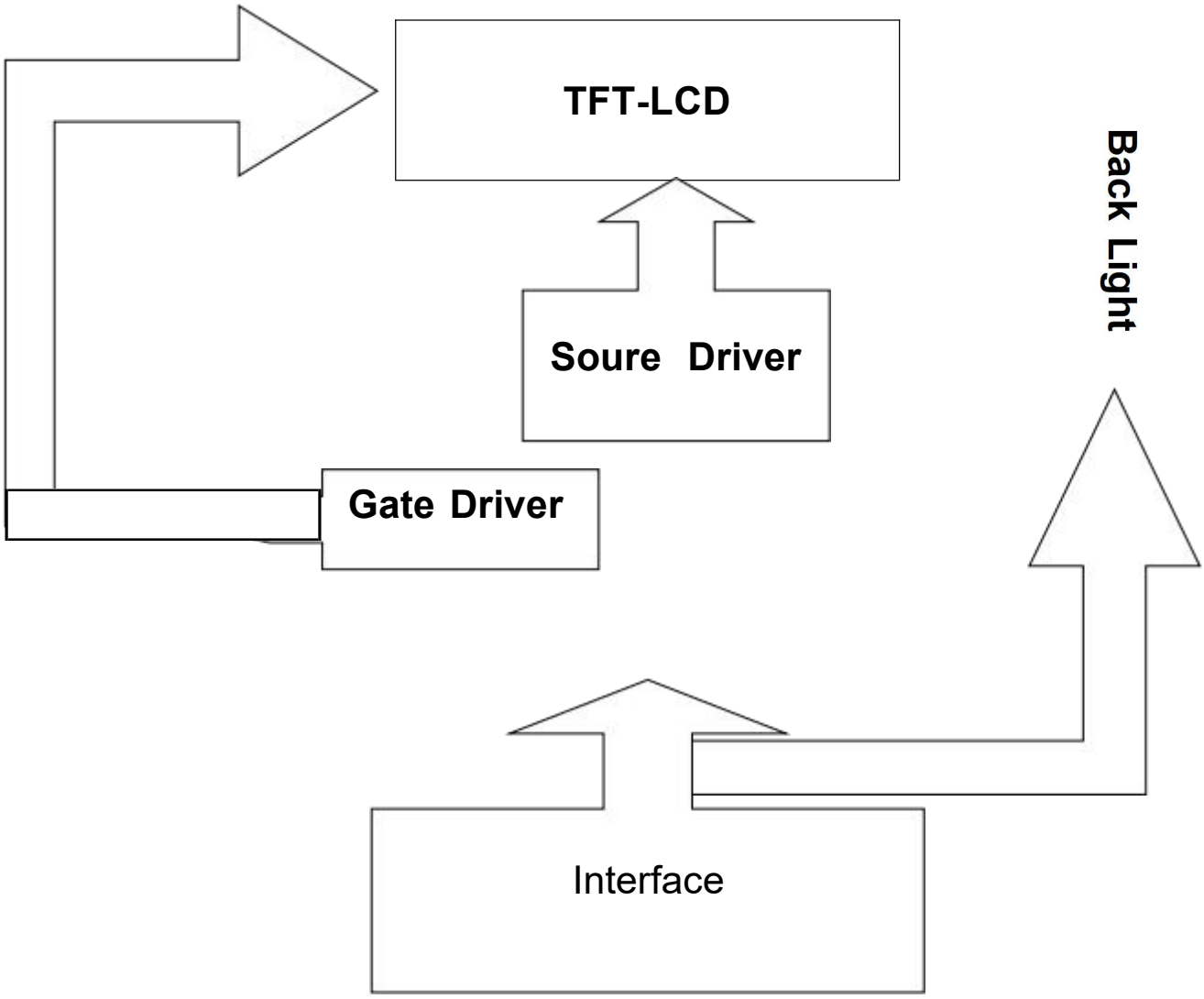


Figure 5. Inrush Measure Condition



7. Module Function Description

7-1. Block Diagram Of LCM



7-2. Pin Description

The electronics interface connector is STM MSAK24025P30.
The connector interface pin assignments are listed in Table 6.

<Table 6. Pin Assignments for the Interface Connector>

Terminal	Symbol	Functions
Pin No.	Symbol	Description
1	NC	Disable
2	H_GND	Ground
3	LANE1_N	eDP RX Channel 1 Negative
4	LANE1_P	eDP RX Channel 1 Positive
5	H_GND	Ground
6	LANE0_N	eDP RX Channel 0 Negative
7	LANE0_P	eDP RX Channel 0 Positive
8	H_GND	Ground
9	AUX_CH_P	eDP AUX CH Positive
10	AUX_CH_N	eDP AUX CH Negative
11	H_GND	Ground
12	LCD_VCC	Power Supply, 3.3V (typ.)
13	LCD_VCC	Power Supply, 3.3V (typ.)
14	BIST	Panel Self Test Enable
15	H_GND	Ground
16	H_GND	Ground
17	HPD	Hot Plug Detect Output
18	BL_GND	LED Ground
19	BL_GND	LED Ground
20	BL_GND	LED Ground
21	BL_GND	LED Ground
22	BL_ENABLE	LED Enable Pin(+3.3V Input)
23	BL_PWM	System PWM Signal Input
24	NC	No Connection
25	NC	No Connection
26	BL_POWER	LED Power Supply 5V-21V
27	BL_POWER	LED Power Supply 5V-21V
28	BL_POWER	LED Power Supply 5V-21V
29	BL_POWER	LED Power Supply 5V-21V
30	NC	No Connection

BLU Interface Connector: STM MSK24037P9 .

<Table 7. Pin Assignments for the BLU Connector>

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	Vout	LED anode connection	6	LED	LED cathode connection
2	Vout	LED anode connection	7	LED	LED cathode connection
3	NC	No Connection	8	LED	LED cathode connection
4	LED	LED cathode connection	9	LED	LED cathode connection
5	LED	LED cathode connection			

7-3 Timing Characteristics

6.1 The NV133WUM-N61 Is Operated By The DE Only

< Table 8. Signal Timing Specification >

Item		Symbols	Min	Typ	Max	Unit
Clock	Frequency	1/Tc	-	154.8	-	MHz
Frame Period		Tv	-	2080	-	lines
			-	60	-	Hz
			-	16.67	-	ms
Vertical Display Period		Tvd	-	1200	-	lines
One line Scanning Period		Th	-	1240	-	clocks
Horizontal Display Period		Thd	-	1920	-	clocks

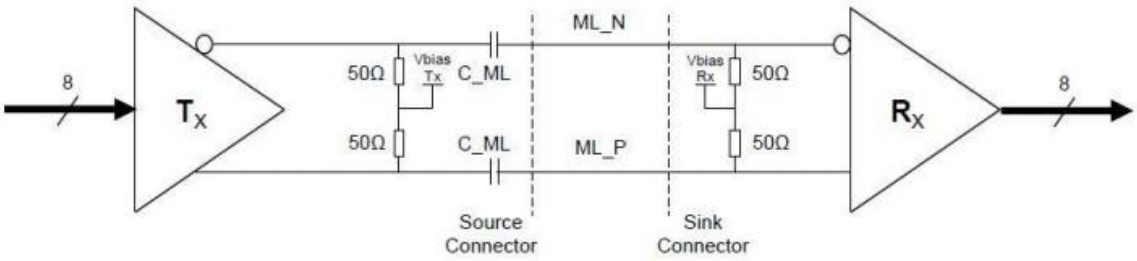
Note : The above is as optimized setting.

6.2 eDP Rx Interface Timing Parameter

The specification of the eDP Rx interface timing parameter is shown in Table 9.

<Table 9. eDP Main-Link RX TP4 Package Pin Parameters>

Item	Symbol	Min	Typ	Max	Unit	Remark
Spread spectrum clock (Link clock down-spreading)	SSC	-	-	0.5	%	
Differential peak-to-peak input voltage at package pins	$V_{RX-DIFFp-p}$	120	-	1200	mV	
Rx input DC common mode voltage	$V_{RX\_DC\_CM}$	0	-	2	V	
Differential termination resistance	$R_{RX-DIFF}$	80	-	100	Ω	
Single-ended termination resistance	R_{RX-SE}	40	-	60	Ω	
Rx short circuit current limit	I_{RX_SHORT}	-	-	20	mA	
Intra-pair skew at Rx package pins (HBR) RX intra-pair skew tolerance at HBR	$L_{RX\_SKEW\_INTRA\_PAIR}$	-	-	60	ps	
AC Coupling Capacitor	C_{SOURCE_ML}	75		200	nF	Source side



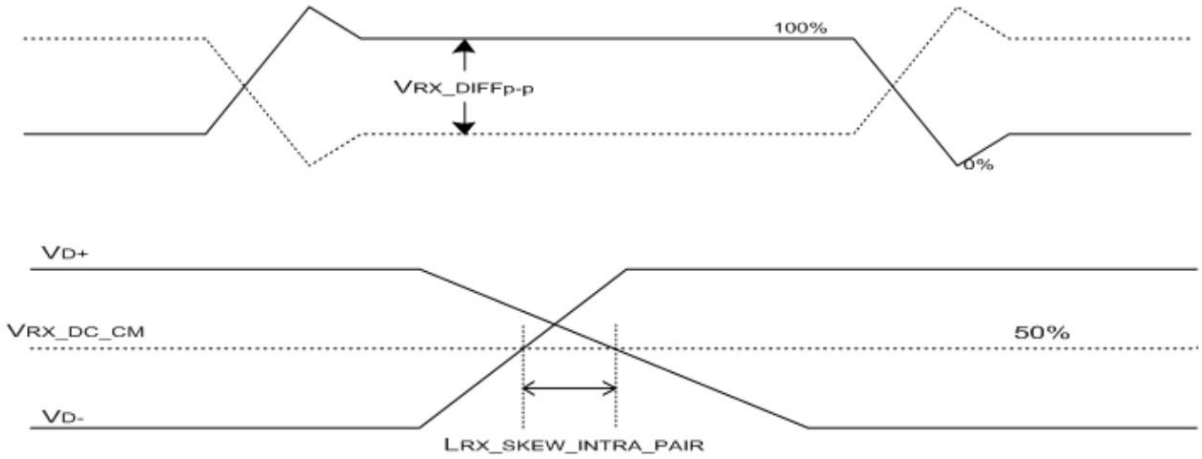


Figure 15. VRX-DIFFp-p & LRX_SKEW_INTRA_PAIR

<Table 10. HPD Characteristics>

Item	Symbol	Min	Typ	Max	Unit	Remark
HPD voltage	V_{HPD}	2.5	-	3.6	V	Sink side
Hot Plug Detection Threshold	-	2.0	-	-	V	Source side
Hot Unplug Detection Threshold	-	-	-	0.8V	V	
HPD_IRQ Pulse Width	HPD_IRQ	0.5	-	1	ms	
HPD_TimeOut	-	2.0	-	-	ms	

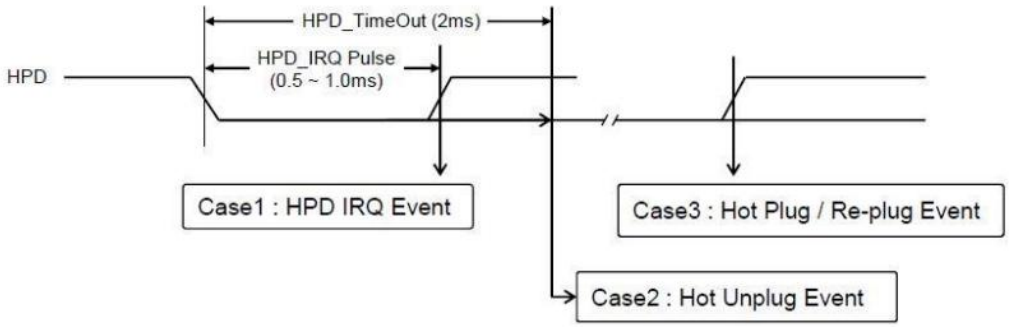


Figure 16. HPD Events

<Table 11. AUX Characteristics>

Item	Symbol	Min	Typ	Max	Unit	Remark
AUX unit interval	U_{IAUX}	0.4	0.5	0.6	Us	
AUX peak-to-peak input differential voltage	$V_{AUX-RX-DIFFp-p}$	0.29	-	1.38	V	Sink Side Connector Pin
AUX CH termination DC resistance	$R_{AUX-TERM}$	80	100	120	Ohm	
AUX DC common mode voltage	$V_{AUX-DC-CM}$	0	-	2	V	
AUX turn around common mode voltage	$V_{AUX-TURN-CM}$			0.3	V	
AUX short circuit current limit	$I_{AUX-SHORT}$	-	-	90	mA	
AUX AC Coupling Capacitor	$C_{SOURCE-AUX}$	75		200	nF	Source side

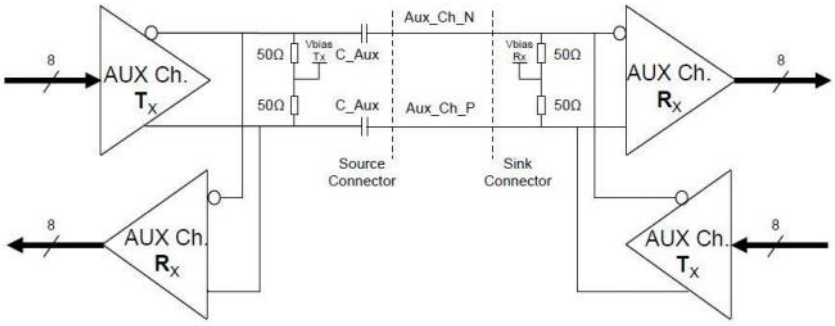


Figure 17. AUX differential pair

7-4 POWER SEQUENCE

To prevent a latch-up or DC operation of the LCD module, the power on/off sequence shall be as shown in below.

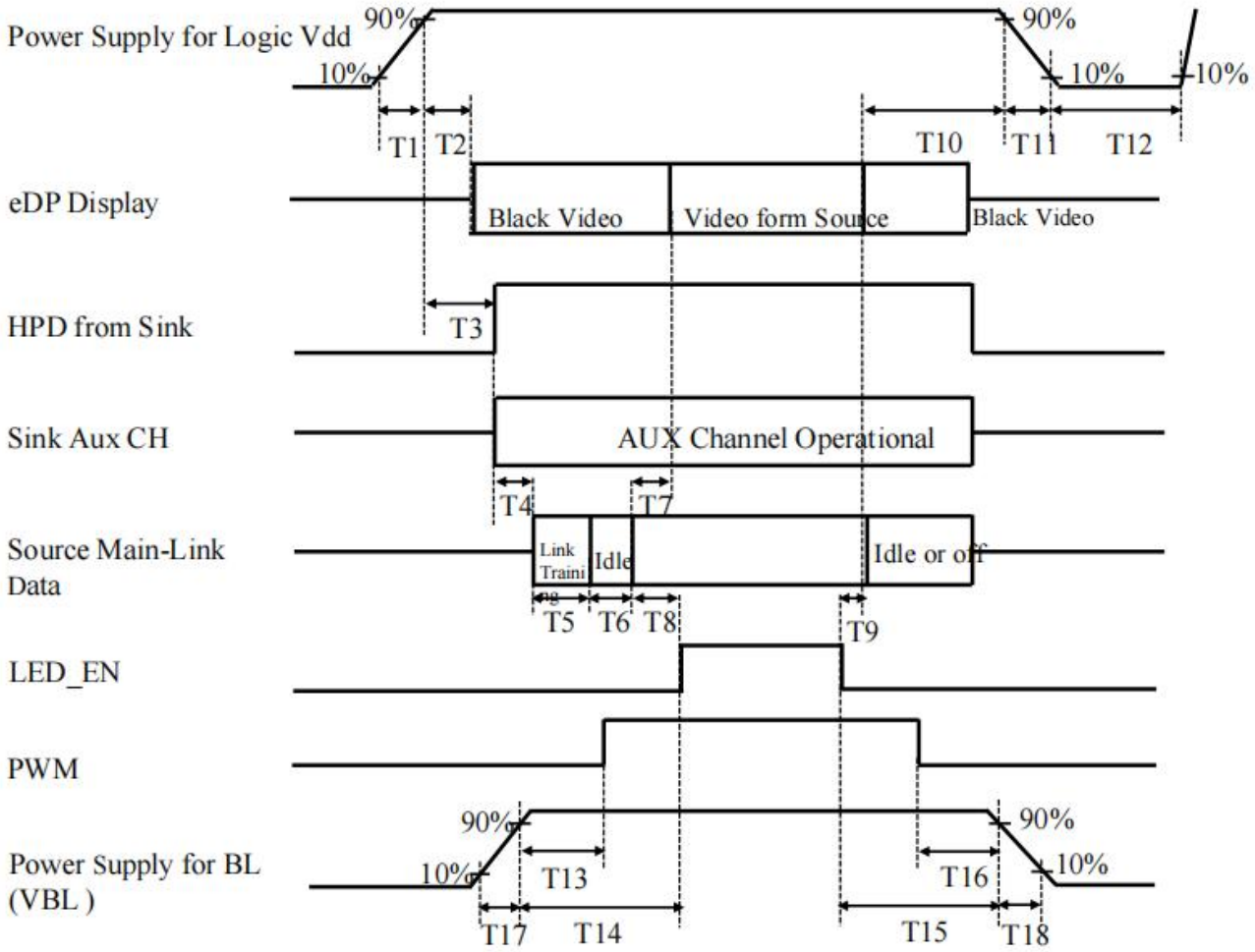


Figure 18. Power Sequence

- 0.5ms ≤ T1 ≤ 10 ms
- 0ms < T2 ≤ 200 ms
- 0ms < T3 ≤ 200 ms
- T4+T5+T6+T8>80ms
- 0ms < T7 ≤ 50ms
- 50ms < T8
- 0ms < T9
- 0ms < T10 < 500 ms
- 0.5ms ≤ T11 ≤ 10 ms
- 500ms ≤ T12
- 0ms < T13
- 0ms < T14
- 0ms < T15
- 0ms < T16
- 0.5ms ≤ T17
- 0.5ms ≤ T18

Notes:

1. When the power supply VDD is 0V, keep the level of input signals on the low or keep high impedance.
2. Do not keep the interface signal high impedance when power is on. Back Light must be turn on after power for logic and interface signal are valid.

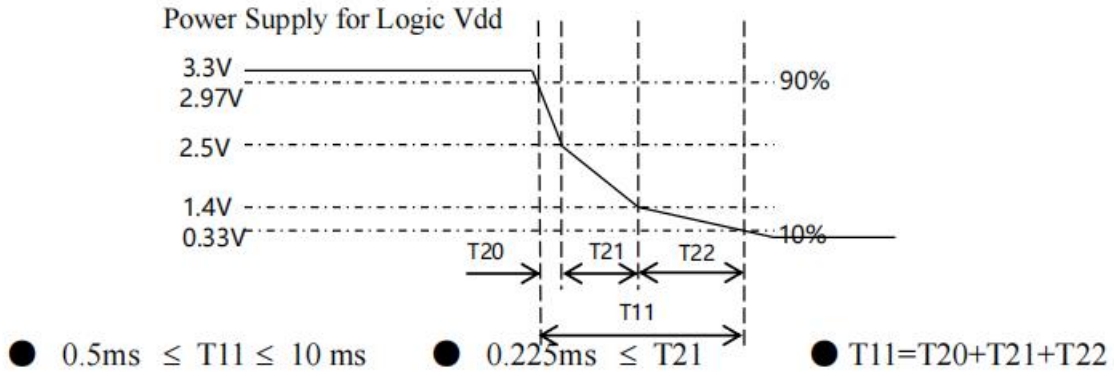


Figure 19. T11 timing requirements

8. Electro-Optical Characteristics

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle Range	Horizontal	Θ_3	CR > 10	80	89	-	Deg.	Note 1
		Θ_9		80	89	-	Deg.	
	Vertical	Θ_{12}		80	89	-	Deg.	
		Θ_6		80	89	-	Deg.	
	Horizontal	Θ_3 Θ_9	CR > 100	-	80	-	Deg.	
	Vertical	Θ_{12} Θ_6		-	80	-	Deg.	
Luminance Contrast Ratio		CR	Θ = 0°	800	1000	-		Note 2
Luminance of White	5 Points	Y_w	Θ = 0° I_{LED} = 13mA	255	300	345	cd/m²	Note 3
White Luminance Uniformity	5 Points	ΔY5		80	-	-		Note 4
	13 Points	ΔY13		65	-	-		
White Chromaticity		W_x	Θ = 0°	0.283	0.313	0.343		Note 5
		W_y		0.299	0.329	0.359		
Reproduction of Color	Red	R_x	Θ = 0°	Typ.-0.03	0.650	Typ.+0.03		
		R_y			0.318			
	Green	G_x			0.300			
		G_y			0.610			
	Blue	B_x			0.150			
		B_y			0.058			
Color Gamut				95	100	-	%	sRGB
Response Time (Rising + Falling)		T_{RT}	Ta= 25°C Θ = 0°	-	25	30	ms	Note 6
Cross Talk		CT	Θ = 0°	-	-	2.0	%	Note 7

The test of optical specifications shall be measured in a dark room (ambient luminance ≤ 1 lux and temperature = 25±2°C) with the equipment of luminance meter system (PR730&PR810) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θ and Φ equal to 0°. We refer to θØ=0 (=θ3) as the 3 o'clock direction (the "right"), θØ=90 (= θ12) as the 12 o'clock direction ("upward"), θØ=180 (= θ9) as the 9 o'clock direction ("left") and θØ=270(= θ6) as the 6 o'clock direction ("bottom"). While scanning θand/or Ø, the center of the measuring spot on the display surface shall stay fixed. The backlight should be operating for 30 minutes prior to measurement. VDD shall be 3.3+/- 0.3V at 25°C. Optimum viewing angle direction is 6 'clock.

Notes :

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see Figure 7).

2. Contrast measurements shall be made at viewing angle of $\Theta = 0$ and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state . (see Figure 7) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

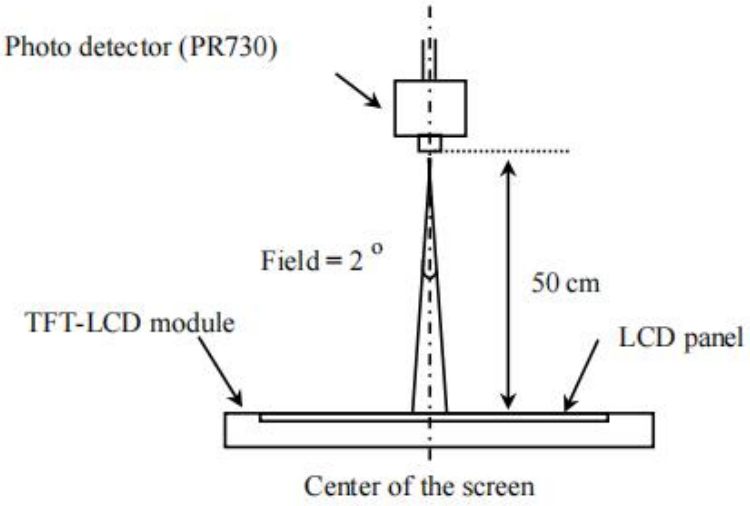
3. Center Luminance of white is defined as luminance values of 5 point average across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in Figure 8 for a total of the measurements per display.

4. The White luminance uniformity on LCD surface is then expressed as : ΔY =Minimum Luminance of 5(or 13) points / Maximum Luminance of 5(or 13) points.(see Figure 8 and Figure 9).

5. The color chromaticity coordinates specified in Table 5 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

6. The electro-optical response time measurements shall be made as Figure 10 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is T_r, and 90% to 10% is T_f.

7. Cross-Talk of one area of the LCD surface by another shall be measured by comparing the luminance (Y_A) of a 25mm diameter area, with all display pixels set to a gray level, to the luminance (Y_B) of that same area when any adjacent area is driven dark. (See Figure 11).



Optical characteristics measurement setup

Figure 7. Measurement Set Up

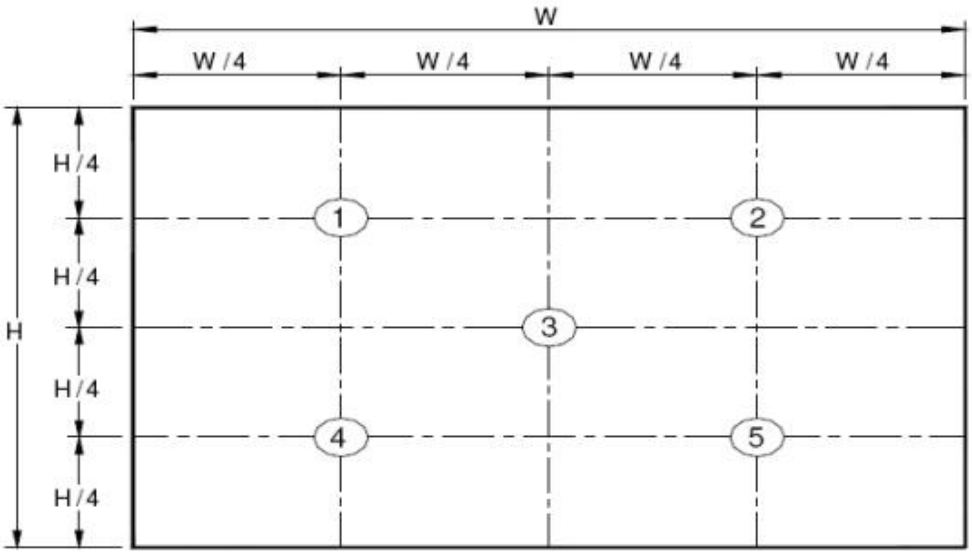


Figure 8. White Luminance and Uniformity Measurement Locations (5 points)

Center Luminance of white is defined as luminance values of center 5 points across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in Figure 7 for a total of the measurements per display.

9.Records Of Version

Version	Revise Date	Page	Content
00	2023-11-20	ALL	New released