

PRODUCT SPECIFICATION **FOR LCD MODULE**

Revision: 1.0

Model No: LS140I01-E-V1

Module Type: COG+FPC+B/L

APPROVED SIGNATURE

- ☒ Approved Product Specification only
- ☐ Approved Product Specification and Samples

<u>Prepared By</u>	<u>Checked By</u>	<u>Approved By</u>

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1. General Description

LS140I01-E-V1 is a color active matrix TFT LCD module using amorphous silicon TFT's (Thin Film Transistors) as an active switching devices. This module has a 14.09inch diagonally measured active area with 4k1k resolutions (3840 horizontal by 1100 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe and this module can display 16.7M(8bit) colors and color gamut 72% NTSC. The TFT-LCD panel used for this module is a low reflection and higher color type. Therefore, this module is suitable for Notebook Touch bar. The LED driver for back-light driving is built in this model.

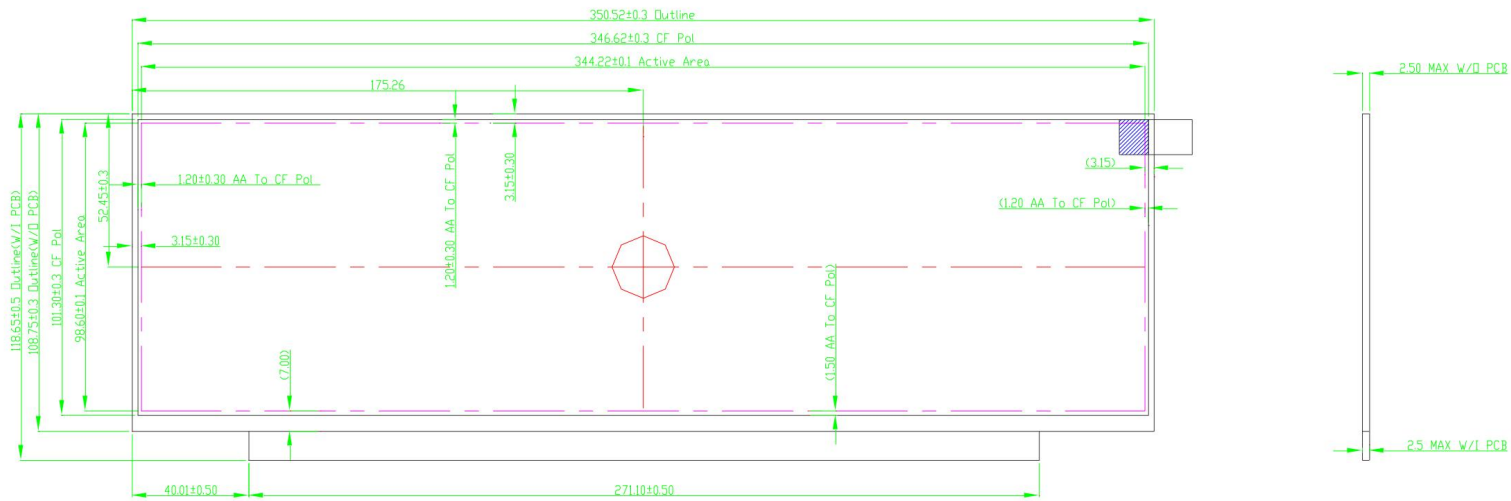
2. Physical Features

Display Mode	TFT-LCD Module
	Active matrix TFT, Transmissive type
Display Format	Graphic 3840(RGB)×1100 Dot-matrix
Input Data	EDP
Viewing Direction (Grayscale Inversion)	Free (IPS)

3. Mechanical Specification

Item	Specification	Unit
Module size (H×V×D)	350.52 ×118.65 ×2.5	mm
Number of dots	3840(RGB) ×1100	pixel
Active area (H×V)	344.2176×98.604	mm

4. Outline Dimension



5. Absolute Maximum Ratings

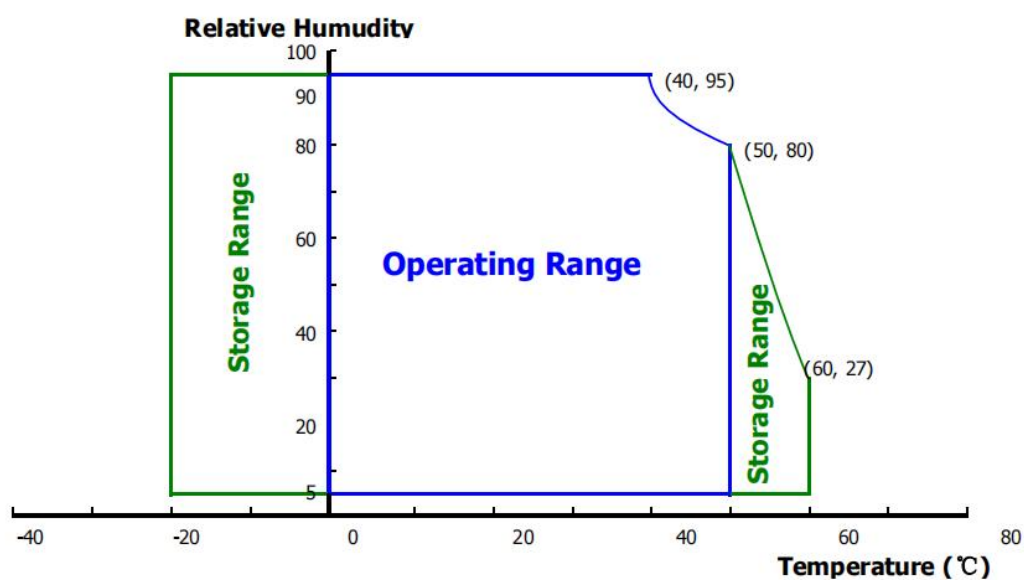
Parameter	Symbol	Min.	Max.	Unit	Remarks
Power Supply Voltage	V_{DD}	-0.3	4.0	V	Note 1
eDP input Voltage	V_{eDP}	0	1.2	V	
Logic Supply Voltage	V_{IN}	$V_{SS}-0.3$	$V_{DD}+0.3$	V	
Operating Temperature	T_{OP}	0	+60	°C	Note 2
Storage Temperature	T_{ST}	-20	+65	°C	

Notes :

1. Permanent damage to the device may occur if maximum values are exceeded functional operation should be restricted to the condition described under normal operating conditions.

2. Temperature and relative humidity range are shown in the figure below.

95 % RH Max. ($40\text{ }^{\circ}\text{C} \geq T_a$) Maximum wet - bulb temperature at $39\text{ }^{\circ}\text{C}$ or less. ($T_a > 40\text{ }^{\circ}\text{C}$) No condensation.



6. Electrical Characteristics

Parameter			Min.	Typ.	Max.	Unit	Remarks
Power Supply Voltage		V _{DD}	3.0	3.3	3.6	V	Note 1
Permissible Input Ripple Voltage		V _{RF}	-	-	100	mV	@ V _{DD} = 3.3V
BIST Control Level		High Level	0.8 VDDIO	-	3.3	V	@VDDIO=1.8 V
		Low Level	0	-	0.15 VDDIO	V	
Power Supply Inrush Current		Inrush	-	-	2	A	Note3
Power Supply Current	Mosaic	I _{DD}	-	330	360	mA	Note 1
	RGB		-	600	670	mA	
Power Consumption	Mosaic	P _M	-	-	1.1	W	
	RGB	P _{RGB}	-	-	2	W	
	BLU	P _{BL}	-	-	2	W	Note 2
	Total	P _{Total}	-	-	3.1	W	@Mosaic

7.Backlight Unit

Parameter		Min.	Typ.	Max.	Unit	Remarks	
LED Forward Voltage		V _F	-	-	2.9	V	
LED Forward Current		I _F	-	9.5	-	mA	
LED Power Input Voltage		V _{LED}	5	12	21	V	
LED Power Input Current		I _{LED}	-	-	167	mA	Note 1
LED Power Consumption		P _{LED}	-	-	2	W	
Power Supply Voltage for LED Driver Inrush		V _{LED}	5	12	21	V	Note 3
LED Life-Time		N/A	15,000	-	-	Hour	I _F = 20mA Note 2
EN Control Level	Backlight On	V _{BL_EN}	1.8	2.5	5.0	V	
	Backlight Off		0	-	0.5	V	
PWM Control Level	High Level	V _{BL_PWM}	1.8	2.5	5.0	V	
	Low Level		0	-	0.5	V	
PWM Control Frequency		F _{PWM}	200	-	2,000	Hz	
Duty Ratio			1	-	100	%	

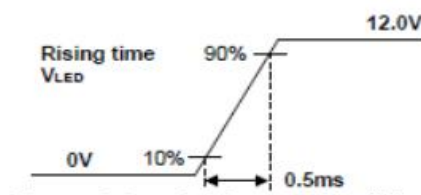
Notes :

1. Power supply voltage 12V for LED driver.

Calculator value for reference $I_F \times V_F \times N / \text{driver efficiency} = P_{LED}$

2. The LED life-time define as the estimated time to 50% degradation of initial luminous.

3. Measure condition (Figure 5)



LED Structure

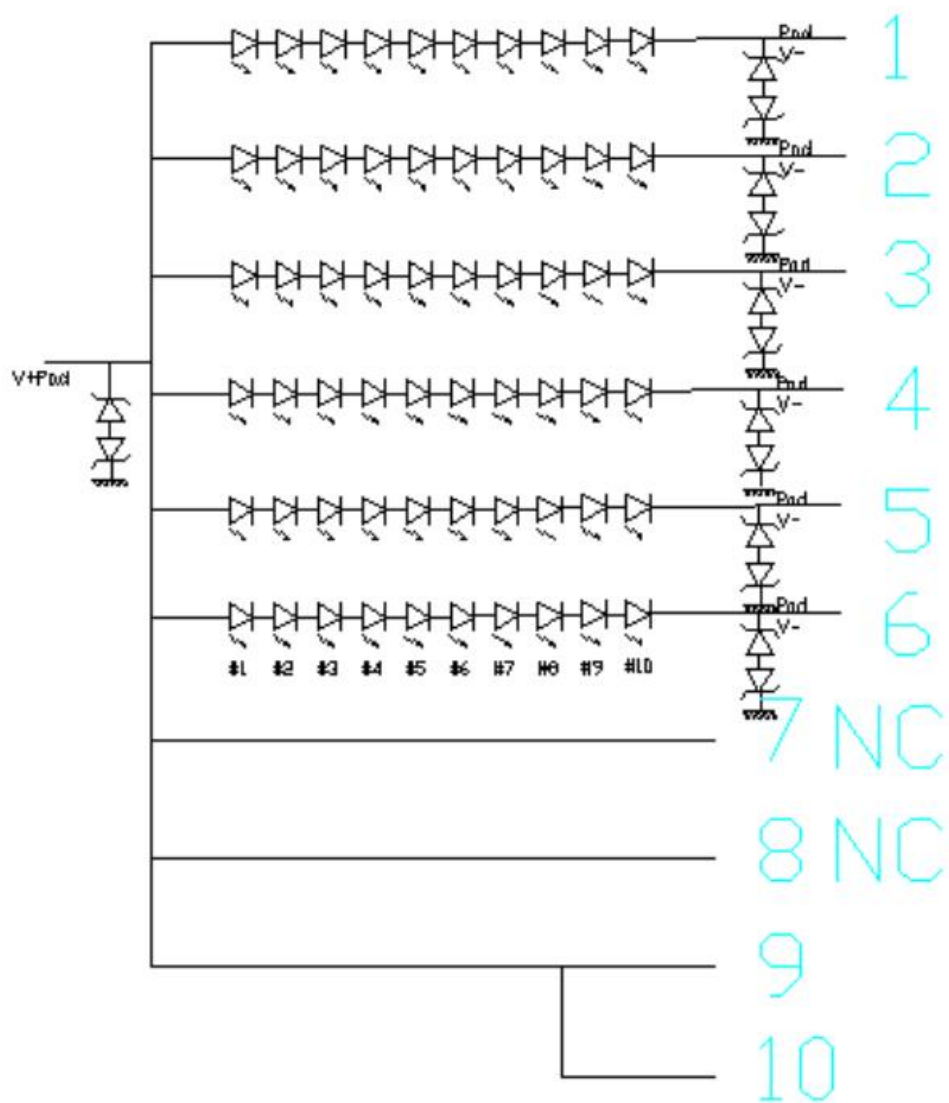
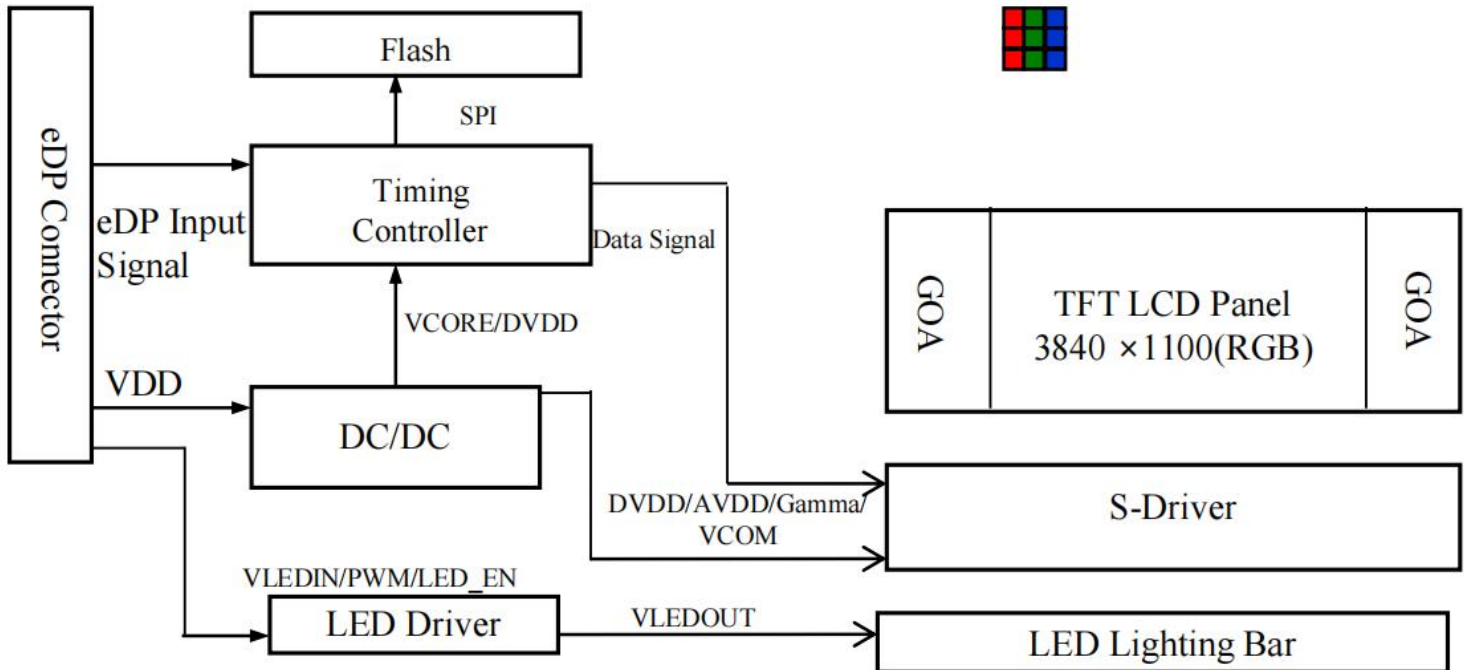


Figure 6. LED Structure

8. Module Function Description

8-1. Block Diagram Of LCM



8-2. Pin Description

The electronics interface connector is LVDS type. The mating connector part number **UJU IS050-L30B-C10**. The connector interface pin assignments are listed in Table 6.

<Table 6. Pin Assignments for the Interface Connector>

Terminal	Symbol	Functions
Pin No.	Symbol	Description
1	CABC	CABC function
2	H_GND	Ground
3	LANE1_N	eDP RX channel 1 negative
4	LANE1_P	eDP RX channel 1 positive
5	H_GND	Ground
6	LANE0_N	eDP RX channel 0 negative
7	LANE0_P	eDP RX channel 0 positive
8	H_GND	Ground
9	AUX_CH_P	eDP AUX CH positive
10	AUX_CH_N	eDP AUX CH negative
11	H_GND	Ground
12	LCD_VCC	Power Supply, 3.3V (typ.)
13	LCD_VCC	Power Supply, 3.3V (typ.)
14	LCD_Self_Test	Panel self test enable
15	H_GND	Ground
16	H_GND	Ground
17	ASUSD	Hot plug detect output
18	BL_GND	LED Ground
19	BL_GND	LED Ground
20	BL_GND	LED Ground
21	BL_GND	LED Ground
22	BL_ENABLE	LED enable pin(+3.3V Input)
23	BL_PWM	System PWM Signal Input
24	NC	No Connection
25	NC	No Connection
26	BL_POWER	LED Power Supply 5V-20V
27	BL_POWER	LED Power Supply 5V-20V
28	BL_POWER	LED Power Supply 5V-20V
29	BL_POWER	LED Power Supply 5V-20V
30	NC	No Connection

BLU Interface Connector: STM MSK24022P10

<Table 7. Pin Assignments for the BLU Connector>

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	LED	LED cathode connection	6	LED	LED cathode connection
2	LED	LED cathode connection	7	NC	No Connection
3	LED	LED cathode connection	8	NC	No Connection
4	LED	LED cathode connection	9	Vout	LED anode connection
5	LED	LED cathode connection	10	Vout	LED anode connection

8-3 Timing Characteristics

6.1 The NV140XTM-N52 V3.1 Is Operated By The DE Only

< Table 8. Signal Timing Specification >

Item		Symbols	Min	Typ	Max	Unit
Clock	Frequency	1/Tc	-	269.5	-	MHz
Frame Period		Tv	-	1140	-	lines
			-	60	-	Hz
			-	16.67	-	ms
Vertical Display Period		Tvd	-	1100	-	lines
One line Scanning Period		Th		3940		clocks
Horizontal Display Period		Thd	-	3840	-	clocks

Note : The above is as optimized setting.

6.2 eDP Rx Interface Timing Parameter

The specification of the eDP Rx interface timing parameter is shown in Table 9.

<Table 9. eDP Main-Link RX TP4 Package Pin Parameters>

Item	Symbol	Min	Typ	Max	Unit	Remark
Spread spectrum clock (Link clock down-spreading)	SSC	-	-	0.5	%	
EYE width at package pins	VRX-EYE	0.38			UI	
Differential peak-to-peak input voltage at package pins	VRX-DIFFp-p	70	-	1200	mV	
Rx input DC common mode voltage	VRX_DC_CM	0	-	2	V	
Differential termination resistance	RRX-DIFF	80	-	100	Ω	
Single-ended termination resistance	RRX-SE	40	-	60	Ω	
Rx short circuit current limit	IRX_SHORT	-	-	20	mA	
Intra-pair skew at Rx package pins (HBR) RX intra-pair skew tolerance at HBR	LRX_SKEW_ INTRA_PAIR	-	-	60	ps	
AC Coupling Capacitor	CSOURCE_ML	75		200	nF	Source side

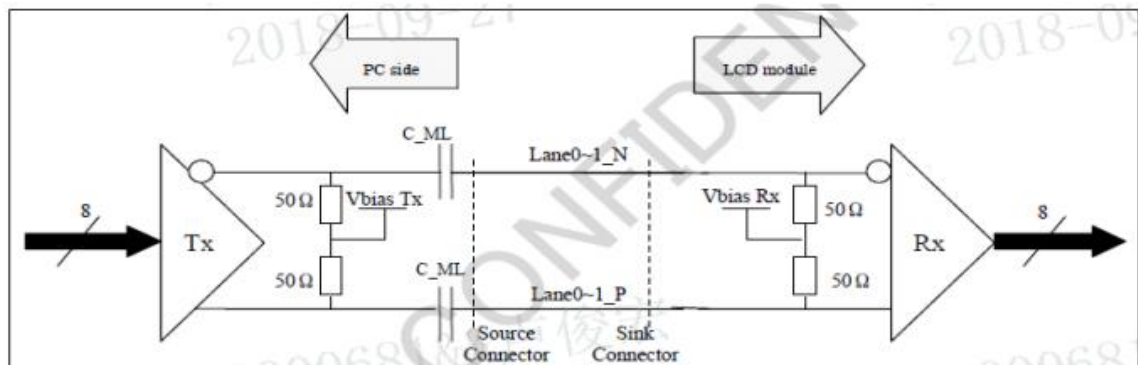


Figure 14. Main link differential pair

SIGNAL TIMING SPECIFICATION

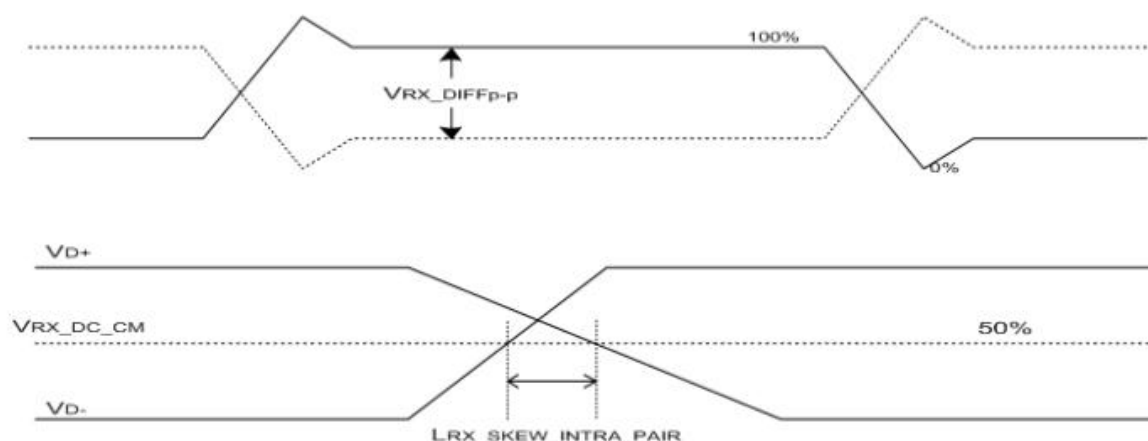


Figure 15. VRX-DIFFp-p & LRX_SKEW_INTRA_PAIR

SIGNAL TIMING SPECIFICATION

<Table 10. HPD Characteristics>

Item	Symbol	Min	Typ	Max	Unit	Remark
HPD voltage	V _{HPD}	2.25	-	3.6	V	
Hot Plug Detection Threshold	-	2.0	-	-	V	Source side Detecting
Hot Unplug Detection Threshold	-	-	-	0.8V	V	
HPD_IRQ Pulse Width	HPD_IRQ	0.5	-	1	ms	
HPD_TimeOut	-	2.0	-	-	ms	

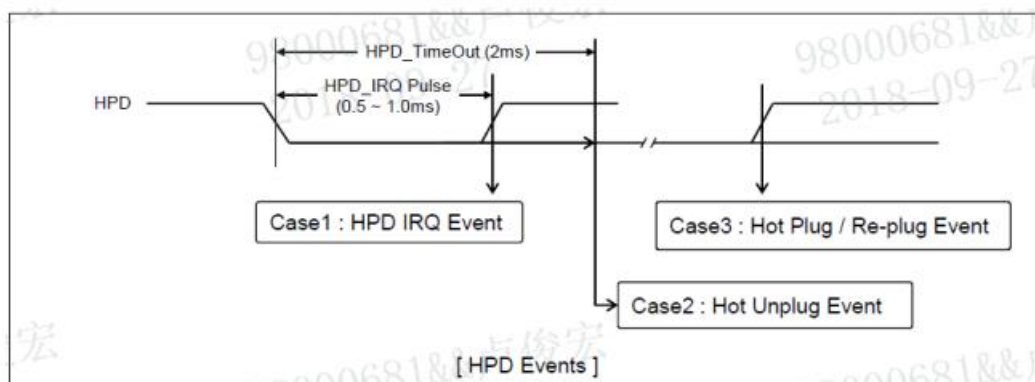


Figure 16. HPD Events

6.0 SIGNAL TIMING SPECIFICATION

<Table 11. AUX Characteristics>

Item	Symbol	Min	Typ	Max	Unit	Remark
AUX unit interval	UIAUX	0.4	0.5	0.6	Us	
AUX peak-to-peak input differential voltage	VAUX-RX-DIFFp-p	0.29	-	1.38	V	
AUX CH termination DC resistance	RAUX-TERM	80	100	120	Ohm	
AUX DC common mode voltage	VAUX-DC-CM	0	-	2	V	
AUX turn around common mode voltage	VAUX-TURN-CM	-	-	0.3	V	
AUX short circuit current limit	IAUX-SHORT	-	-	90	mA	
AUX AC Coupling Capacitor	CSOURCE-AUX	75	-	200	nf	Source side

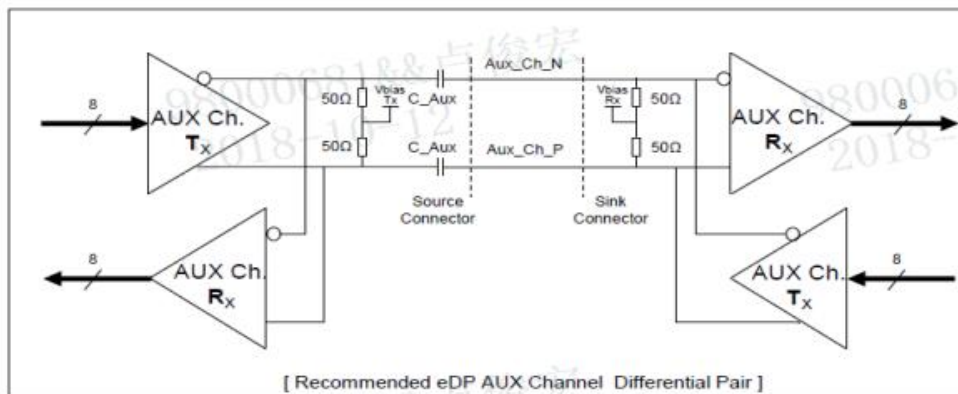


Figure 17. AUX differential pair

8.0 POWER SEQUENCE

To prevent a latch-up or DC operation of the LCD module, the power on/off sequence shall be as shown in below.

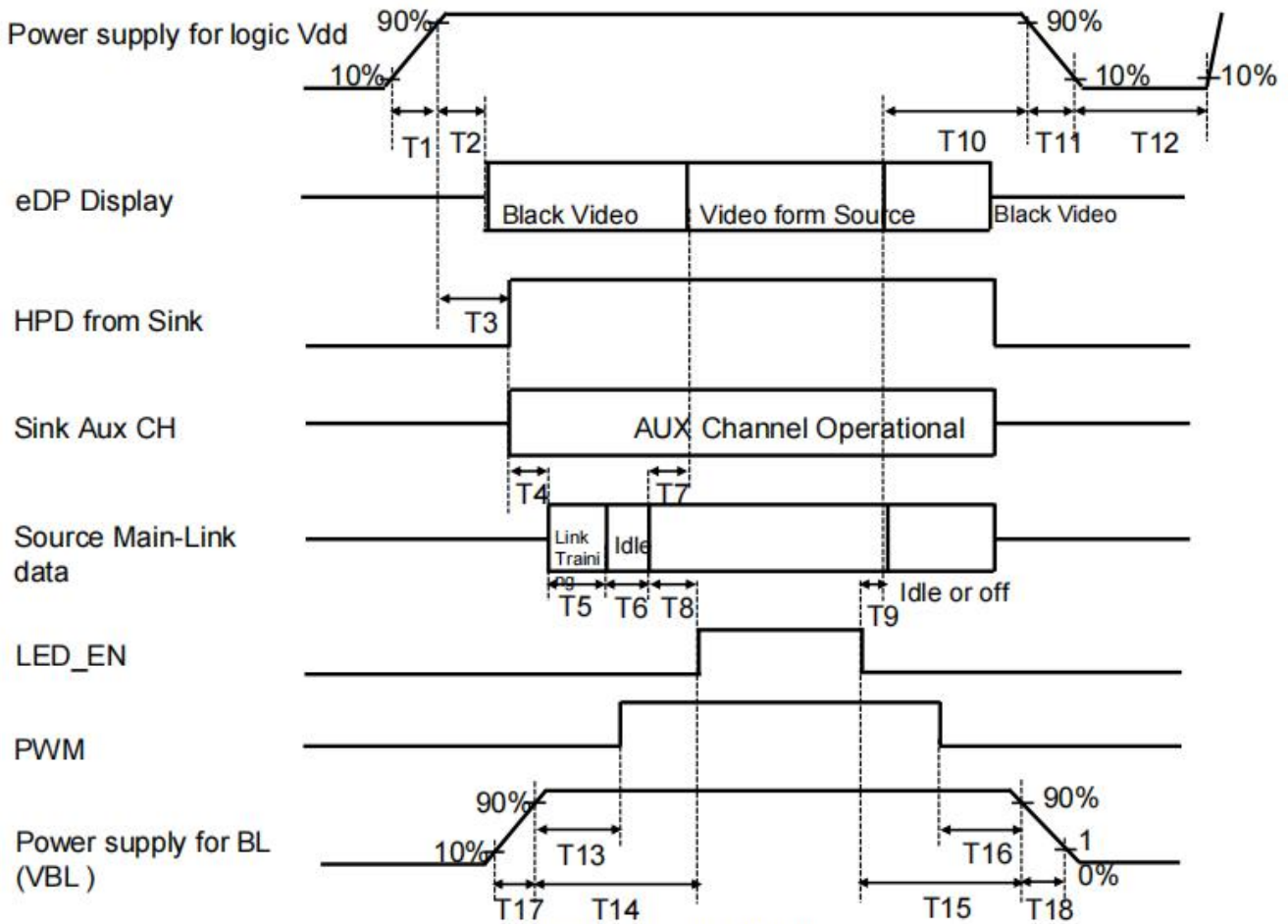


Figure 18. Power Sequence

- $0.5\text{ms} \leq T1 \leq 10\text{ms}$
- $0\text{ms} < T2 \leq 200\text{ms}$
- $0\text{ms} < T3 \leq 200\text{ms}$
- $T3+T4+T5+T6+T8 > 200\text{ms}$
- $0\text{ms} < T7 \leq 50\text{ms}$
- $50\text{ms} < T8$
- $0\text{ms} < T9$
- $0\text{ms} < T10 < 500\text{ms}$
- $0.5\text{ms} \leq T11 \leq 10\text{ms}$
- $500\text{ms} \leq T12$
- $10\text{ms} < T13$
- $20\text{ms} < T14$
- $20\text{ms} < T15$
- $10\text{ms} < T16$
- $0.5\text{ms} \leq T17$
- $0.5\text{ms} \leq T18$

Notes:

1. When the power supply VDD is 0V, keep the level of input signals on the low or keep high impedance.
2. Do not keep the interface signal high impedance when power is on. Back Light must be turn on after power for logic and interface signal are valid.

POWER SEQUENCE

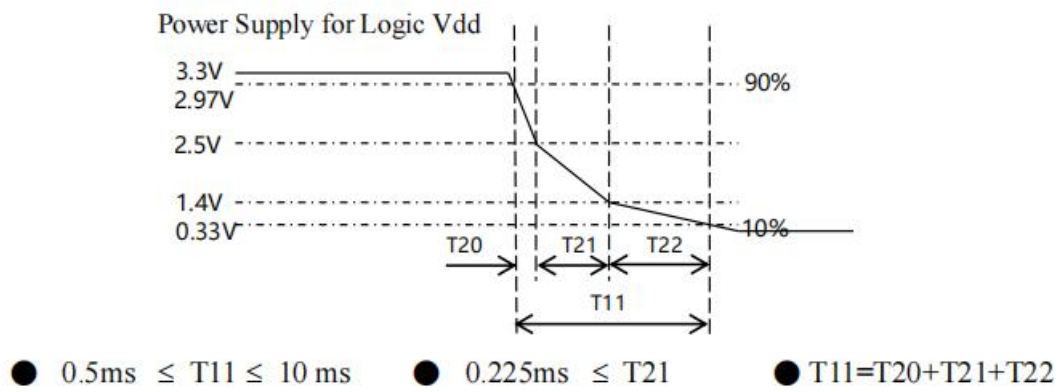


Figure 19. T11 timing requirements

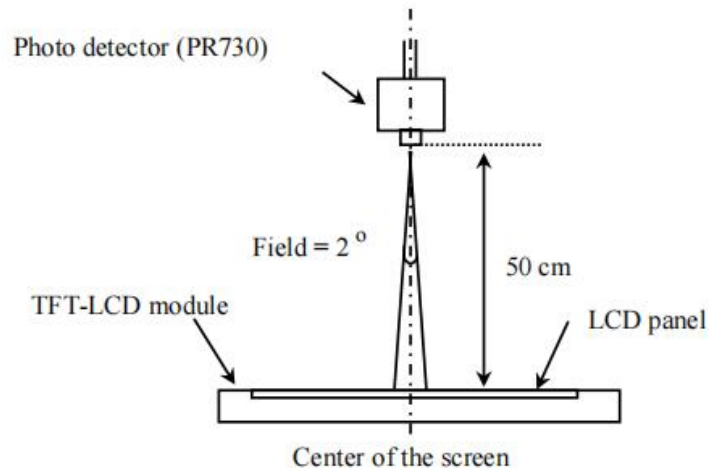
8. Electro-Optical Characteristics

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time		Tr +Tf	$\theta_x = \theta_y = 0$	---	30	35	ms	Note 1
Contrast Ratio		CR		900	1200	---	---	Note 2
Color Chromaticity (CIE1931)	White	W x	$\theta_x = \theta_y = 0$	---	0.313	---	---	
		W y		---	0.329	---	---	
Viewing angle	θ_T		CR > 10	80	85	---	Deg.	Note 3
	θ_B			80	85	---		
	θ_L			80	85	---		
	θ_R			80	85	---		
Luminance ($I_F = 21mA$)		L		255	300	---	cd/m2	Note4

Notes :

- Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see Figure 7).
- Contrast measurements shall be made at viewing angle of $\Theta = 0$ and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state . (see Figure 7) Luminance Contrast Ratio (CR) is defined mathematically.
$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$
- Center Luminance of white is defined as luminance values of 5 point average across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in Figure 8 for a total of the measurements per display.
- The White luminance uniformity on LCD surface is then expressed as : $\Delta Y = \text{Minimum Luminance of 5(or 13) points} / \text{Maximum Luminance of 5(or 13) points.}$ (see Figure 8 and Figure 9).
- The color chromaticity coordinates specified in Table 5 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.
- The electro-optical response time measurements shall be made as Figure 10 by switching the “data” input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is T_r , and 90% to 10% is T_f .
- Cross-Talk of one area of the LCD surface by another shall be measured by comparing the luminance (YA) of a 25mm diameter area, with all display pixels set to a gray level, to the luminance (YB) of that same area when any adjacent area is driven dark. (See Figure 11).

4.3 Optical Measurements



Optical characteristics measurement setup

Figure 7. Measurement Set Up

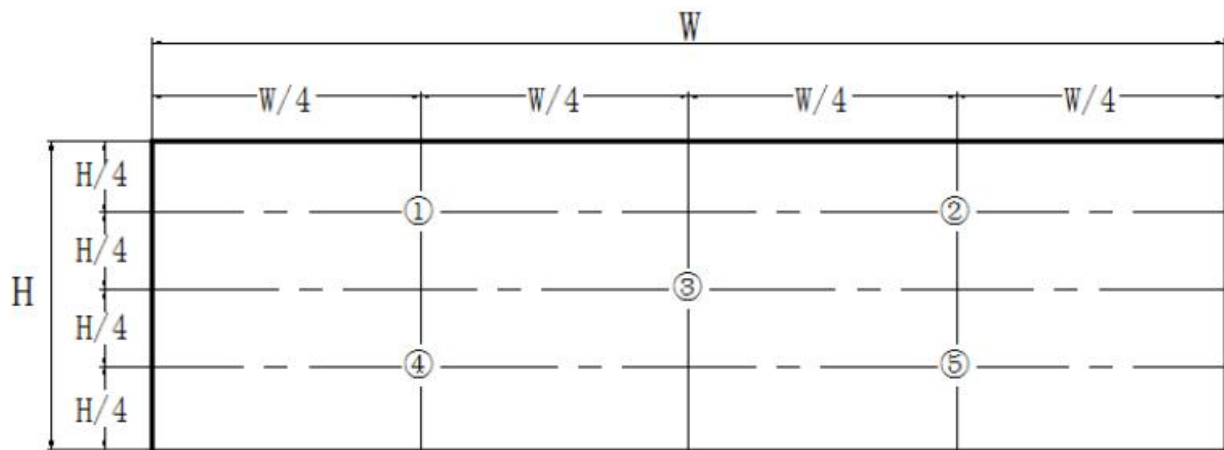


Figure 8. White Luminance and Uniformity Measurement Locations (5 points)

Center Luminance of white is defined as luminance values of center 5 points across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in Figure 7 for a total of the measurements per display.

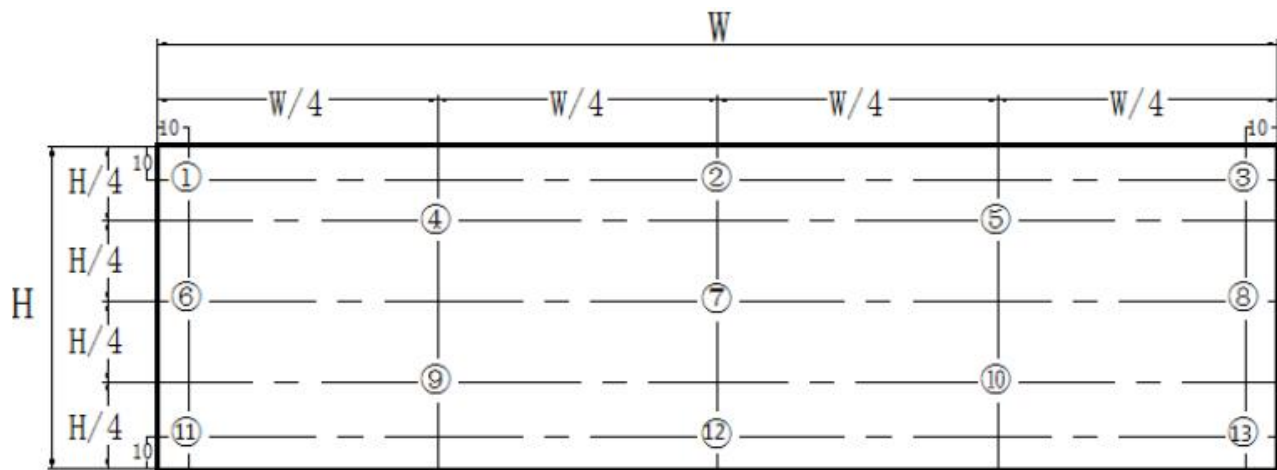


Figure 9. Uniformity Measurement Locations (13 points)

The White luminance uniformity on LCD surface is then expressed as : $\Delta Y5$ = Minimum Luminance of five points / Maximum Luminance of five points (see Figure 8) , $\Delta Y13$ = Minimum Luminance of 13 points / Maximum Luminance of 13 points (see Figure 9).

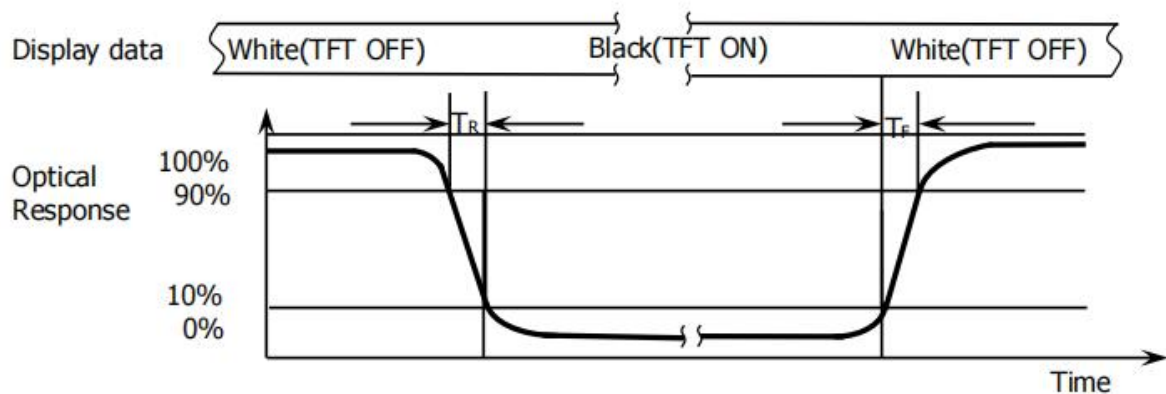


Figure 10. Response Time Testing

The electro-optical response time measurements shall be made as shown in Figure 10 by switching the “data” input signal ON and OFF. T_r : The luminance to change from 10% to 90% , T_f : The luminance to change from 90% to 10% .

9.Records Of Version

Version	Revise Date	Page	Content
00		ALL	New released