

MODEL:LS2145I01- L-V1

Ver. 2.1

Date: 19.Dec.2023

Customer's Approval	Lesson
Signature Date	Approved By Product Director Date Name: Signature:
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	Reviewed By PM Date Name: Signature:

Revision History

Version	Date	Page	Section	Description	Revision by
Ver.0. 1	2023.10.10	ALL	ALL	Preliminary Specification	
Ver.2.1	2023.12.19	P4&22	1.3&6.2	Update the optical specifications	
		P9	3.1	Update the power consumption	

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1. General Description

1.1 Product Features

- **FHD Resolution (1920 * 1080)**
- **Very High Contrast Ratio: 4000:1**
- **High Color Saturation: 72% NTSC**
- **Fast Response Time**
- **Ultra Wide Viewing Angle: 178°(H)/178°(V) (CR≥10)**
- **DE (Data Enable) Mode**
- **LVDS (Low Voltage Differential Signaling) Interface**

1.2 Overview

LS2145I01-L-V1 is a diagonal 21.45" color active matrix LCD open cell with 2 Channel interface. This open cell is a transmissive type display operating in the normally black mode. It supports 1920 * 1080 FHD resolution and can display up to 16.7M colors (8 bit). Each pixel is divided into Red, Green and Blue sub-pixels which are arranged in vertical stripe.

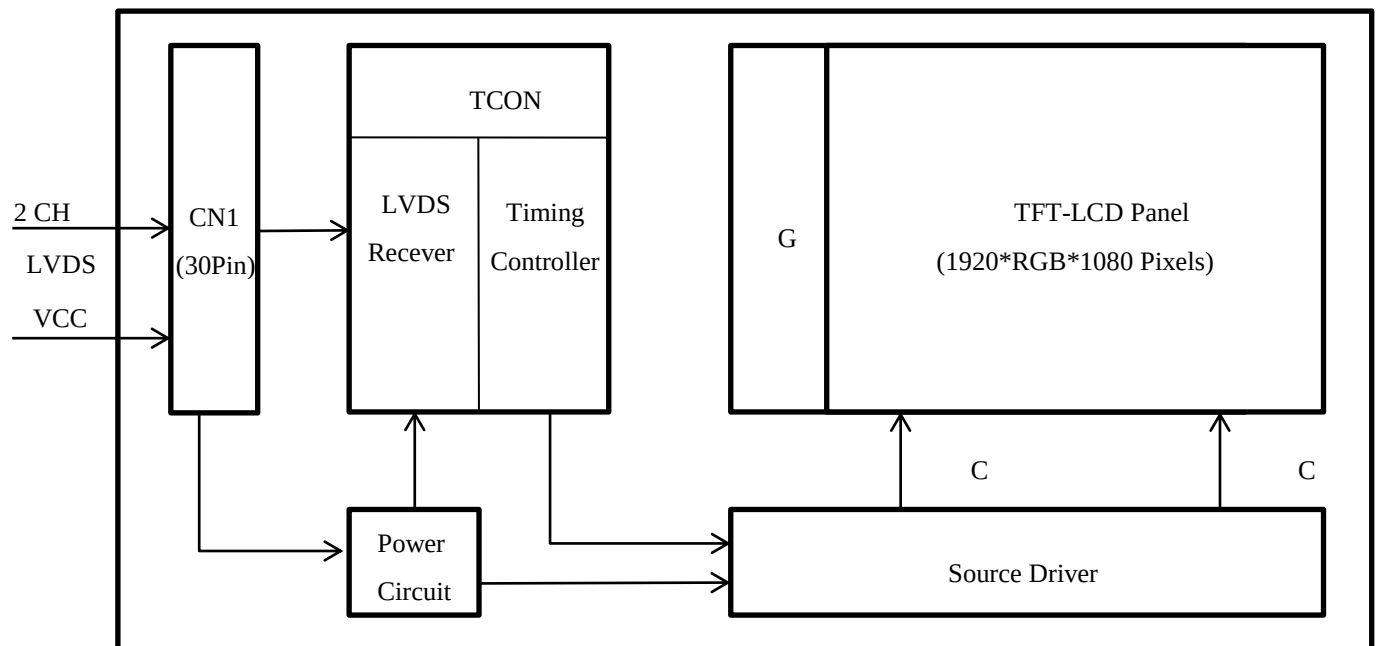
This open cell dedicates for CID products and provides excellent performance which includes high contrast ratio, high color saturation and high color depth. CSOT open cell comply with RoHS for identification.

1.3 General Information

Item	Specification	Unit	Note
Active Area	478.656 (H) x 260.28 (V)	mm	
Cell Size	487.456 (H) * 270.18 (V) * 1.335 (D)	mm	W/O side sealing
Weight	0.418	kg	Typ.
Driving Scheme	a-Si TFT Active Matrix	-	
Number of Pixels	1920 x 1080	pixel	
Pixel Pitch(Sub Pixel)	0.0831 (H) x 0.241 (V)	mm	
Pixel Arrangement	RGB Vertical Stripe	-	
Display Colors	16.7M	color	8bit
Display Mode	Transmissive Mode, Normally Black	-	
Glass thickness (Array / CF)	0.5 / 0.5	mm	
Color Chromaticity	(0.280, 0.316)	-	Typical value measured with CSOT's Flat Backlight at refresh rate FR = 60Hz. (CSOT Flat BLU Wx=0.278 · Wy=0.272)
Contrast Ratio	4000:1(Typ.)	-	
Cell Transmittance	4.4(Typ.)	%	
View Angle (CR>10)	178°(H), 178°(V) (Typ.)	-	
Polarizer (CF side)	AG25%,	-	

Interface	2 channel LVDS		
Mode	DE (Data Enable)		

1.4 Block Diagram



2. Absolute Maximum Ratings

2.1 Absolute Maximum Ratings

The followings are maximum values which, if exceeded, may cause damage to the unit.

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCC	-0.3	5.5	V	Ta=25± 2°C
Input Signal Voltage	VIN	-0.3	3.6	V	
Operating Temperature	TOP	0	+50	°C	
Storage Temperature	TST	-20	+60	°C	

2.2 Environment Requirement

(1) Temperature and relative humidity range are shown as below.

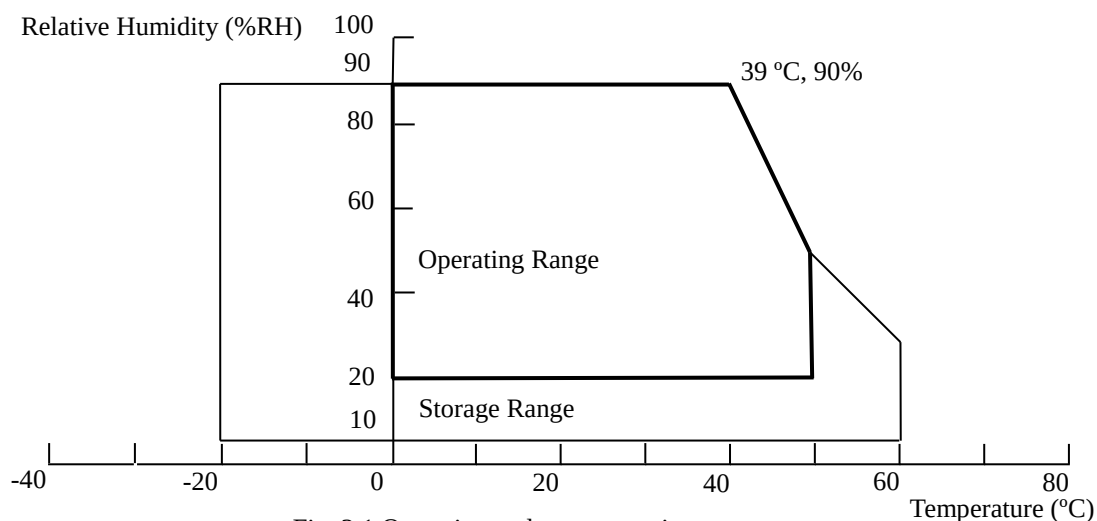


Fig. 2.1 Operating and storage environment

- (a) 90%RH maximum (TA < 39 °C).
- (b) Wet-bulb temperature should be 39 °C maximum (TA > 39 °C).
- (c) No condensation.

- (2) The storage temperature is between - 20 °C to 60 °C, and the operating ambient temperature is between 0 °C to 50 °C .The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 °C with LCD module in a temperature controlled chamber alone. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 °C. The range of operating temperature may degrade in case of improper thermal management in the end product design.
- (3) The rating of environment is based on LCD module. Leave LCD cell alone, this environment condition can't be guaranteed. Except LCD cell, the customer has to consider the ability of other parts of LCD module and LCD module process.

2.3 Package Storage

When storing open cell as spares for a long time, please follow the precaution instructions:

(1) Do not store the open cell in high temperature and high humidity for a long time. It is highly recommended to store the open cell with temperature from 5°C ~ 40°C and humidity from 35%RH~75%RH with shipping package.

(2) The open cell should be kept at a circumstance shown below:

0-2months	2-3months	3-6months
No baking	50°C 、 10%RH · 24hr	50°C 、 10%RH · 48hr

3. Electrical Specification

3.1 Open Cell Power Consumption (TA = 25 ± 2 °C)

Parameter		Symbol	Value			Unit	Note	
			Min.	Typ.	Max.			
Power Supply Voltage		VCC	4.5	5	5.5	Vdc		
Permissive Input Ripple Voltage		VRIPPLE	-	-	500	mVp-p	(1)	
Rush Current		IRUSH	-	-	3	A	(2)	
Power Supply Current	White Pattern	-	-	0.565	0.735	A	60Hz	(3)
	Green and Red Vertical Pattern		-	0.833	1.08	A		
	Black Pattern		-	0.491	0.638	A		
	Mosaic Pattern(8*8)		-	0.532	0.692	A		
Power Consumption	Green and Red Vertical Pattern	-	-	4.165	5.415	Watt	60Hz	

Note:
The Ripple Voltage should be controlled less than 10% of VCC and measured under the condition of VCC(typ),TA=25±2°C,

Measurement condition: VCC rising time = 470 μs.

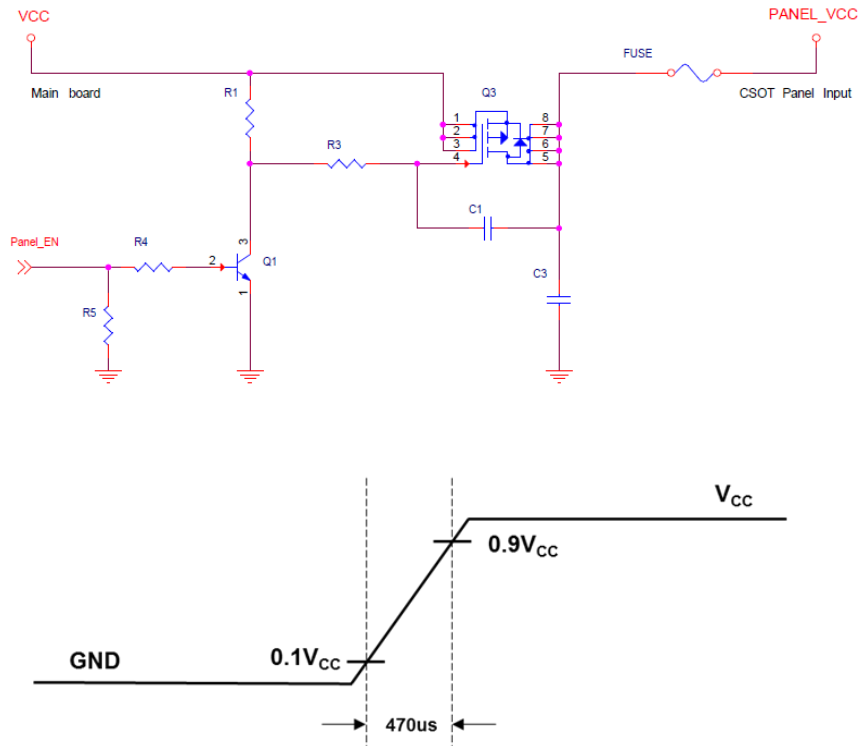
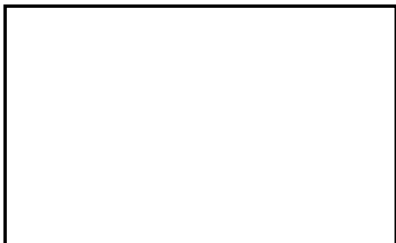


Fig. 3.1 VCC rising time condition

(3) Measurement condition: $VCC = 5V$, $T_a = 25 \pm 2\text{ }^{\circ}\text{C}$, the test patterns are shown as below.

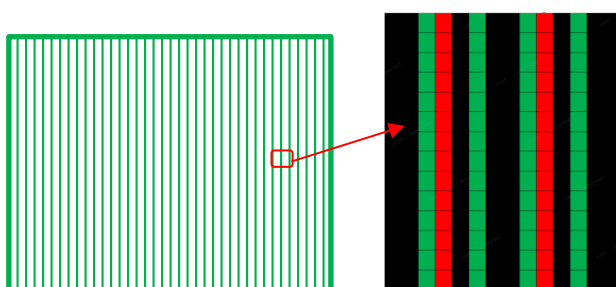
a. White Pattern



b. Black Pattern



c. Green and Red Vertical Pattern



d. Mosaic Pattern (8*8)

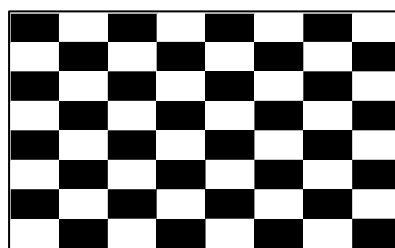


Fig. 3.2 Test patterns

3.2 LVDS Characteristics

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
LVDS Interface	Differential Input High Threshold Voltage	V _{TH}	100	-	-	mV	(1)
	Differential Input Low Threshold Voltage	V _{TL}	-	-	-100	mV	(1)
	Common Input Voltage	V _{cm}	1.0	1.2	1.4	V	(2)
	Differential Input Voltage	V _{ID}	100	-	600	mV	(3)
	Terminating Resistor	R _T	90	100	110	ohm	
CMOS Interface	Input High Threshold Voltage	V _{IH}	2.7	-	3.3	V	
	Input Low Threshold Voltage	V _{IL}	0	-	0.7	V	

Note:

- (1) Condition: V_{cm}=1.2V
- (2) The product should be always operated within above ranges.
- (3) The LVDS input signal has been defined as follows:

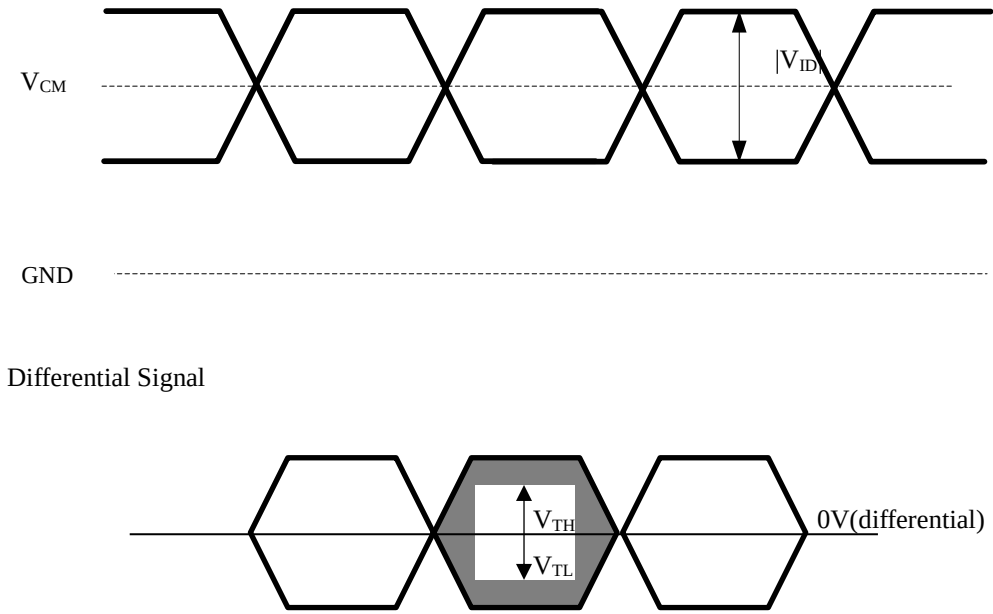


Fig. 3.3 LVDS input signal

3.3 Temperature Specifications

Parameter	Symbol	Specification			Unit	Recommended test pattern	Note
		Min.	Typ.	Max.			
Surface Temperature	TTCN	-	-	100	°C	Green and Red Vertical Pattern	(1)
	TPMIC			100		Green and Red Vertical Pattern	(1)
	TDriver	-	-	115		Green and Red Vertical Pattern	(1)

Note:

Any point on the IC surface must be less than Max. specification, if the surface temperature is out of the specification, thermal solutions should be applied to avoid be damaged. The IC surface temperature is measured at room temperature of 25°C.

3.4 Driver IC ESD Specifications

The Electro-Static Discharge tolerance of Source COF IC and Gate COF IC is +-2KV tested by ESD Gun. Especially if the LCD module is designed with the Plastic Bezel, ESD protection solutions should be applied to avoid be damaged, as shown in Fig.3.4.

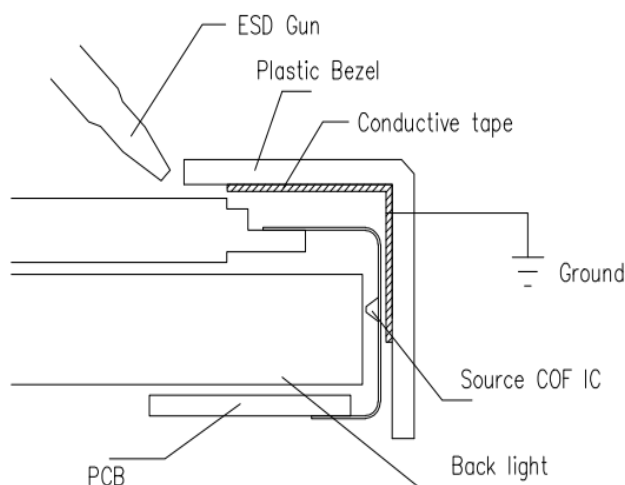


Fig. 3.4 Source COF IC ESD protection

4. Input Terminal Pin Assignment

4.1 Interface Pin Assignment

CN1: 1-301223-0(XDYT) or equivalent (see Note (1))

Pin No.	Symbol	Description	Note
1	RO[0]N	Odd LVDS Signal -	
2	RO[0]P	Odd LVDS Signal +	
3	RO[1]N	Odd LVDS Signal -	
4	RO[1]P	Odd LVDS Signal +	
5	RO[2]N	Odd LVDS Signal -	
6	RO[2]P	Odd LVDS Signal +	
7	GND	Ground	
8	ROCLK-	Odd LVDS Clock -	
9	ROCLK+	Odd LVDS Clock +	
10	RO[3]N	Odd LVDS Signal -	
11	RO[3]P	Odd LVDS Signal +	
12	RE[0]N	Even LVDS Signal -	
13	RE[0]P	Even LVDS Signal +	
14	GND	Ground	
15	RE[1]N	Even LVDS Signal -	
16	RE[1]P	Even LVDS Signal +	
17	GND	Ground	
18	RE[2]N	Even LVDS Signal -	
19	RE[2]P	Even LVDS Signal +	
20	RECLK-	Even LVDS Clock -	
21	RECLK+	Even LVDS Clock +	
22	RE[3]N	Even LVDS Signal -	
23	RE[3]P	Even LVDS Signal +	
24	GND	Ground	
25	NC	No Connection (for CSOT test only. Do not Connect)	NC
26	NC	No Connection (for CSOT test only. Do not Connect)	NC
27	NC	No Connection (for CSOT test only. Do not Connect)	NC
28	5V	DC power supply	
29	5V	DC power supply	
30	5V	DC power supply	

Note:

(1) The direction of pin assignment is shown as below:

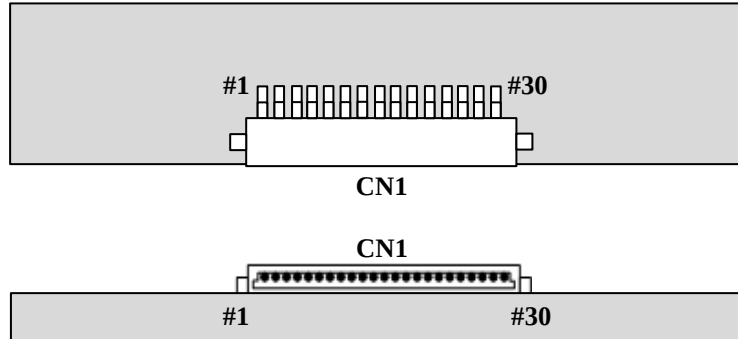


Fig. 4.1 Connector direction sketch map

4.2 Block Diagram of Interface

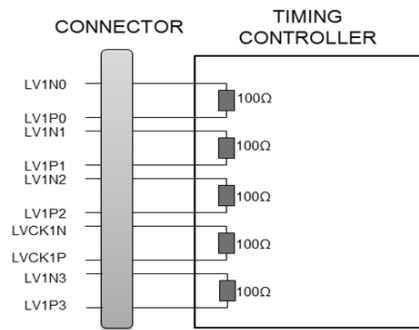


Fig. 4.2 Block diagram of interface

Attention:

- (1) This open cell uses a 100 ohms (Ω) resistor between positive and negative lines of each receiver input.
- (2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line respectively.

4.3 LVDS Interface

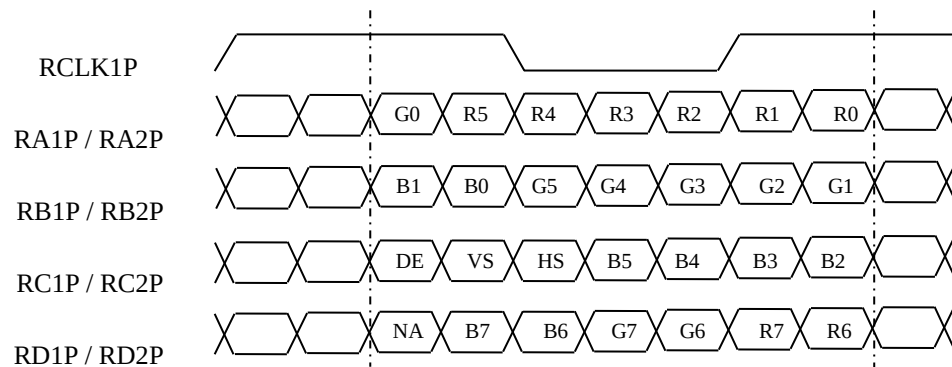
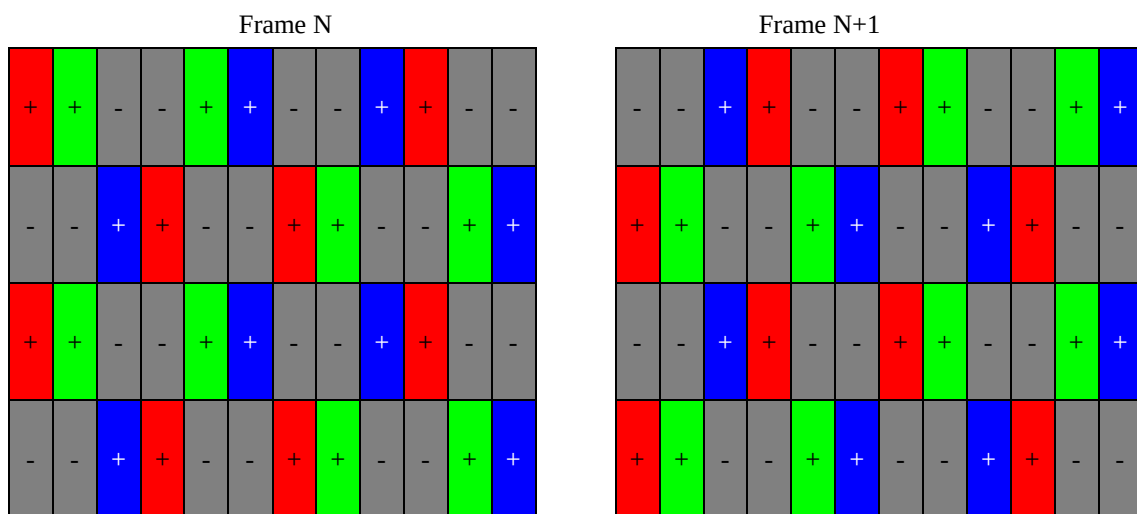


Fig. 4.3 VESA format

4.4 Flicker Pattern

Flicker should be adjusted by the 2 Dot on/off pattern, where are displayed alternately at vertical line. (2 Dot inversion)

2 Dot on/off pattern (L128)



5. Interface Timing

5.1 Timing Table (DE Only Mode)

Item		Symbol	Min.	Typ.	Max.	Unit	Note
Frequency		DCLK	55	74.25	96	MHz	(1)
Frame Rate		FR	48	60	75	Hz	
Vertical Term	Total	Tv	1092	1125	1745	Line	TV = TVD + TVB (2)
	Active Display	TVD	1080			Line	
	Blank	TVB	12	45	665	Line	
Horizontal Term	Total	TH	1060	1100	1174	Pixel	TH = THD + THB
	Active Display	THD	960			Pixel	
	Blank	THB	100	140	214	Pixel	
LVDS Receiver Clock	Input cycle to cycle jitter	Trcl	-	-	200	ps	(3)
	Spread spectrum modulation range	Fclkin_mod	-3%	-	+3%	MHz	(4)
	Spread spectrum modulation frequency	FSSM	30	-	200	KHz	
LVDS Receiver Data	Receiver Skew Margin	TRSM	-350	-	350	ps	(5)

Note:

- (1) The TFT LCD open cell is operated in DE only mode, H sync and V sync input signal have no effect on normal operation.
- (2) $F_{clkin} = TH \times TV \times Frate \times (1 + F_{clkin_mod})$, TH, TV and Frate should operate within the range between Pixel clock frequency Min. and Pixel clock frequency Max..

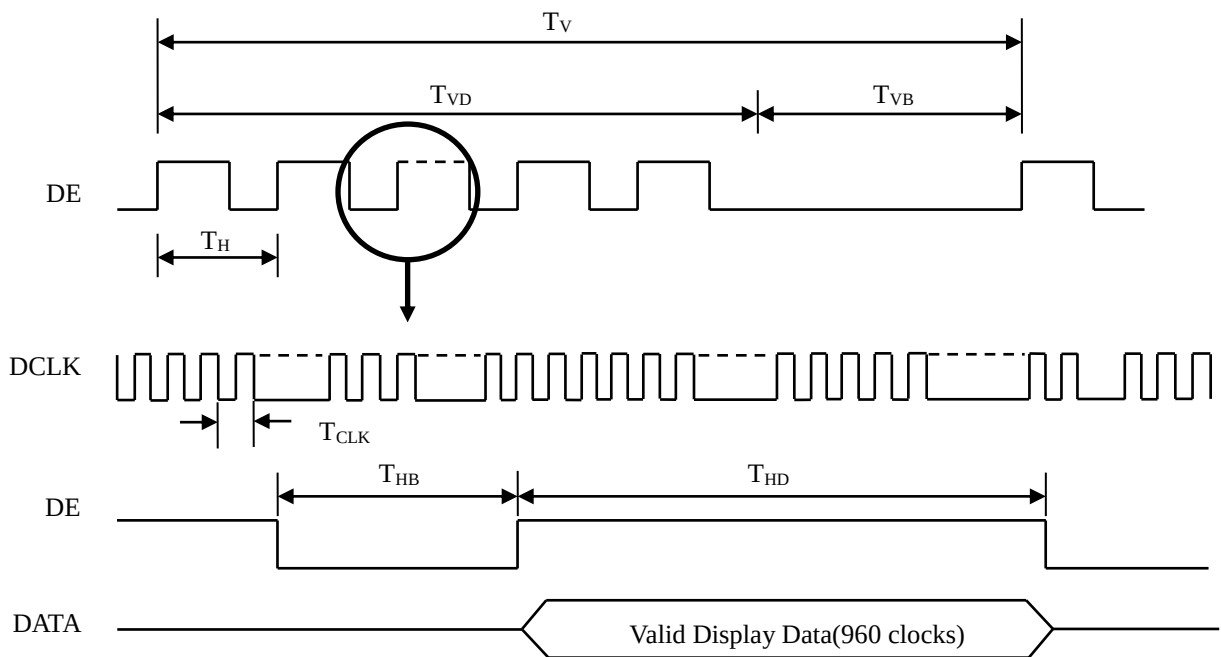


Fig. 5.1 Interface signal timing diagram

(3) The input clock cycle-to-cycle is defined as below figures.

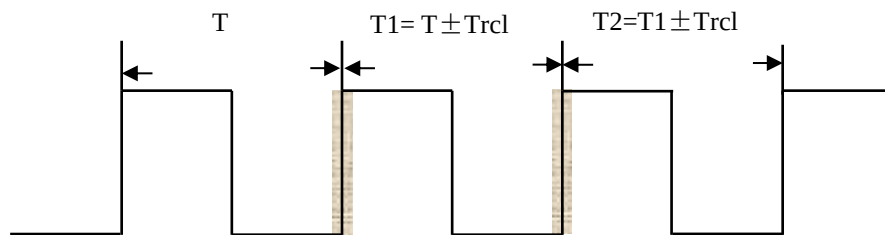


Fig. 5.2 Jitter

(4) The SSM (Spread Spectrum Modulation) is defined as the following figure. The LVDS SSM's suggestion is disabled by default; SOC board should test all validation if SOC board enables the LVDS SSM.

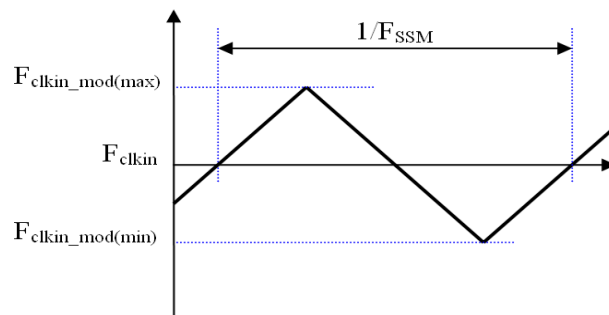


Fig. 5.3 SSM

(5) The LVDS timing diagram and setup/hold time is defined in the following figure.

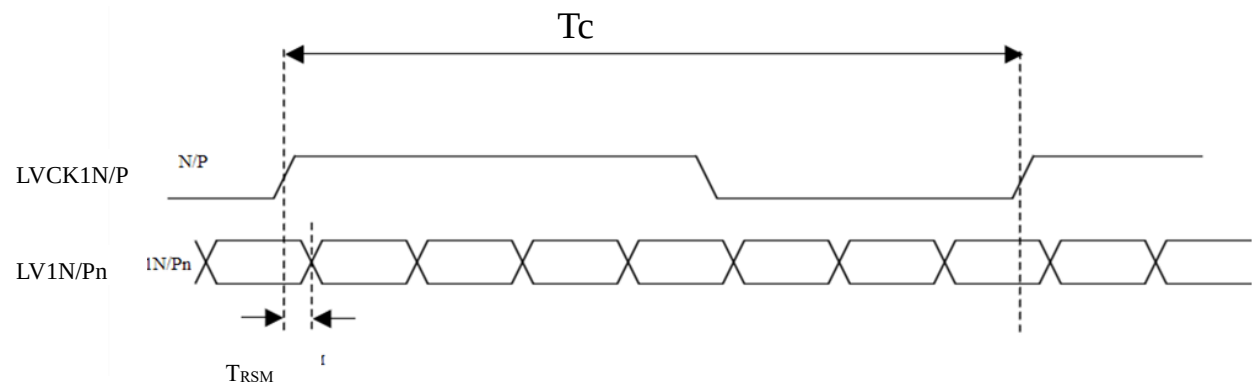


Fig.5.4 LVDS receiver interface timing diagram

5.2 Power On/Off Sequence

To prevent a latch-up or DC operation of LCD module, the power on/off change signal sequence should be as the diagram below.

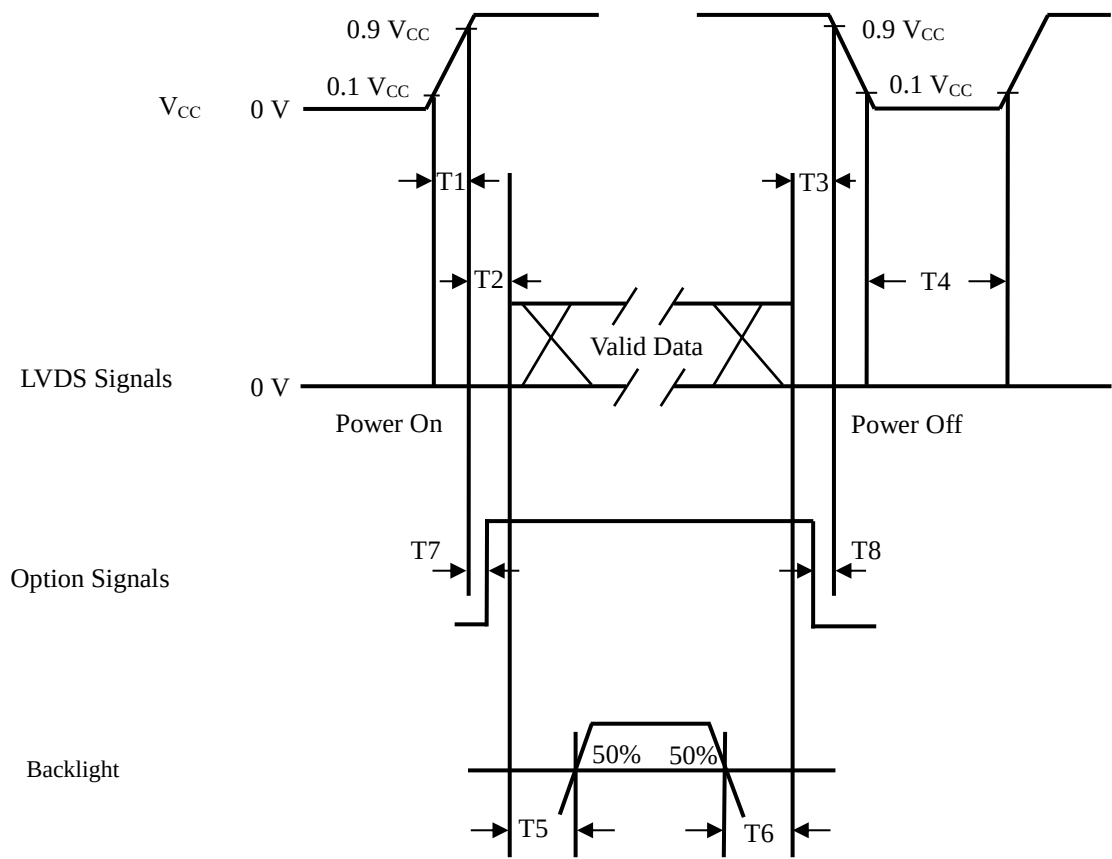


Fig.5.5 Power on/off sequence

Parameter	Values			Unit Min.
	Min.	Typ.	Max.	
T1	0.5	-	10.0	ms
T2	0.0	-	50	ms
T3	0.0	-	50	ms
T4	1000.0	-	-	ms
T5	500.0	-	-	ms
T6	100.0	-	-	ms
T7	-	-	T2	ms
T8	-	-	T3	ms

Attention:

- (1) The supplied voltage of the external system for the open cell input should follow the definition of VCC.
- (2) When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.
- (3) In case that VCC is in off level, keep the level of input signals on the low or high impedance. If $T2 < 0$, that may cause electrical overstress.
- (4) T4 should be measured after the module has been fully discharged between power off and on period.
- (5) Interface signal shall not be kept at high impedance when the power is on.

6. Optical Characteristics

6.1 Measurement Conditions

The table below is the test condition of optical measurement.

Item	Symbol	Value	Unit
Ambient Temperature	TA	25 ± 2	°C
Ambient Humidity	HA	50 ± 10	% RH
Supply Voltage	VCC	5	V
Driving Signal	Refer to the typical value in Chapter 3: Electrical Specification		
Vertical Refresh Rate	FR	60	Hz

To avoid abrupt temperature change during optical measurement, it's suggested to warm up the LCD module more than 60 minutes after lighting the backlight and in the windless environment.

To measure the LCD cell, it is suggested to set up the standard measurement system as Fig. 6.1. The measuring area S should contain at least 500 pixels of the LCD cell as illustrated in Fig.6.2 (A means the area allocated to one pixel). In this model, for example, the minimum measuring distance Z is 370mm when θ is 2 degree. Hence, 500mm is the typical measuring distance. This measuring condition is referred to 301-2H of VESA FPDM 2.0 about viewing distance, angle, and angular field of view definition.

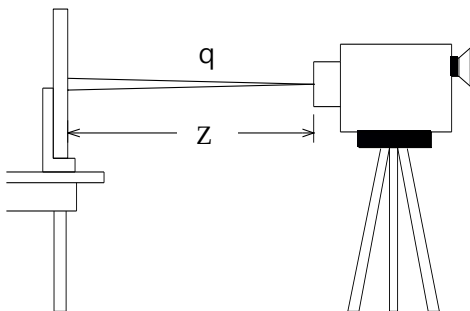


Fig. 6.1 The standard set-up system of measurement

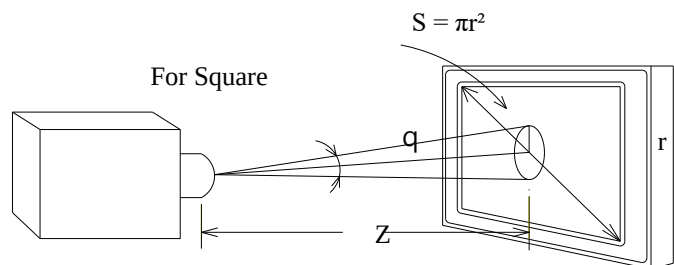


Fig. 6.2 The area S contains at least 500 pixels to be measured

$$N = \frac{S}{A} \geq 500 \text{ pixels}$$

N means the actual number of the pixels in the area S.

6.2 Optical Specifications

The table below of optical characteristics is measured by MINOLTA CS2000, MINOLTA CA310, ELDIM OPTI Scope-SA and ELDIM EZ contrast in dark room.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Static Contrast Ratio		CR	$\theta H = 0^\circ, \theta V = 0^\circ$ Normal direction at center point with CSOT's module: LS2145I01-L-V1. Typical value measured at CSOT's module Flat BLU : $W_x=0.278$ $W_y=0.272$	-	4000	-	-	(1) (2)
Center Transmittance		Tr		-	4.4	-	%	(2) (4)
Gamma		-		2.0	2.2	2.4		
Color Chromaticity (CIE1931)	Red	RX		Typ. - 0.03	0.651	Typ. + 0.03	-	(2) (5)
		RY			0.337		-	
	Green	GX			0.300		-	
		GY			0.627		-	
	Blue	BX			0.149		-	
		BY			0.068		-	
	White	WX			0.280		-	
		WY			0.316		-	
	Color Gamut	CG		-	72	-	% NTSC	
Response Time		TL	FR = 60Hz		8	12	ms	(3)
Viewing Angle	Horizontal	$\theta H+$	CR ≥ 10		89	-	Deg.	(6)
		$\theta H-$			89	-		
	Vertical	$\theta V+$			89	-		
		$\theta V-$			89	-		

Note:

(1) Definition of static contrast ratio (CR):

It's necessary to switch off all the dynamic and dimming function when measuring the static contrast ratio.

$$\text{Static Contrast Ratio (CR)} = \frac{\text{CR-W}}{\text{CR-D}}$$

CR-W is the luminance measured by LMD (light-measuring device) at the center point of the LCD module with full-screen displaying white. The standard setup of measurement is illustrated in Fig. 6.3; CR-D is the luminance measured by LMD at the center point of the LCD module with full-screen displaying black. The LMD in this item is CS2000.

(2) The LMD in the item could be a spectroradiometer such as (KONICA MINOLTA) CS2000, CS1000(TOPCON), SR-UL2 or the same level spectroradiometer. Other display color analyzer (KONICA MINOLTA) CA210, CA310 or (TOPCON) BM-7 could be involved after being calibrated with a spectroradiometer on each stage of a product.

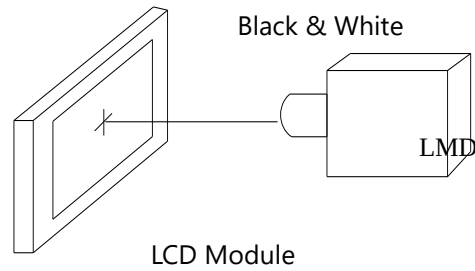


Fig. 6.3 The standard setup of CR measurement

(3) Response time T_L is defined as the average transition time in the response time matrix. The table below is the response time matrix in which each element t_X to Y is the transition time from luminance ratio X to Y . X and Y are two different gray level among 0%, 25%, 50%, 75%, and 100% gray level. The transition time t_X to Y is defined as the time taken from 10% to 90% of the luminance difference between X and Y ($X < Y$) as illustrated in Fig.6.4. When $X > Y$, the definition of t_X to Y is the time taken from 90% to 10% of the luminance difference between X and Y . The response time is optimized on refresh rate $F_r = 60\text{Hz}$.

Measured Transition Time		Gray level of Previous Frame				
		0%	25%	50%	75%	100%
Gray level of Current Frame	0%		$t_{25\% \text{ to } 0\%}$	$t_{50\% \text{ to } 0\%}$	$t_{75\% \text{ to } 0\%}$	$t_{100\% \text{ to } 0\%}$
	25%	$t_{0\% \text{ to } 25\%}$		$t_{50\% \text{ to } 25\%}$	$t_{75\% \text{ to } 25\%}$	$t_{100\% \text{ to } 25\%}$
	50%	$t_{0\% \text{ to } 50\%}$	$t_{25\% \text{ to } 50\%}$		$t_{75\% \text{ to } 50\%}$	$t_{100\% \text{ to } 50\%}$
	75%	$t_{0\% \text{ to } 75\%}$	$t_{25\% \text{ to } 75\%}$	$t_{50\% \text{ to } 75\%}$		$t_{100\% \text{ to } 75\%}$
	100%	$t_{0\% \text{ to } 100\%}$	$t_{25\% \text{ to } 100\%}$	$t_{50\% \text{ to } 100\%}$	$t_{75\% \text{ to } 100\%}$	

t_X to Y means the transition time from luminance ratio X to Y .

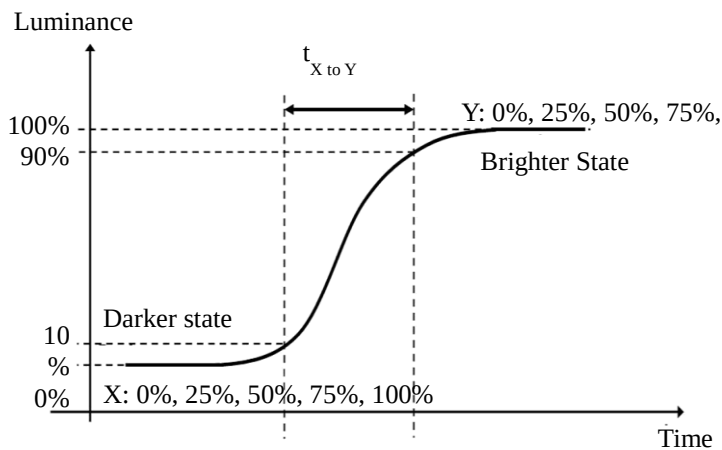


Fig. 6.4 The definition of t_X to Y

All the transition time is measured at the center point of the LCD module by ELDIM OPTI Scope-SA.

(4) Definition of center Transmittance ($T\%$):

The transmittance is measured with full white pattern (Gray 255)

$$\text{Center Transmittance (T\%)} = \frac{\text{Luminance of LCD module}}{\text{Luminance of Backlight}}$$

(5) Definition of color chromaticity:

Each chromaticity coordinates (x, y) are measured in CIE1931 color space when full-screen displaying primary color R, G, B and white. The color gamut is defined as the fraction in percent of the area of the triangle bounded by R, G, B coordinates and the area is defined by NTSC 1953 color standard in the CIE color space. Chromaticity coordinates are measured by CS2000 and the standard setup of measurement is shown in Fig. 6.5.

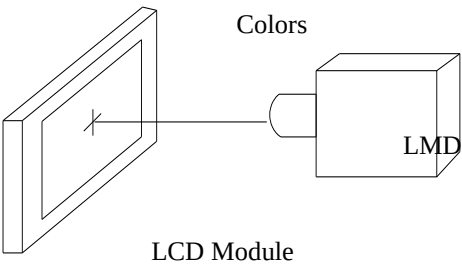


Fig. 6.5 The standard setup of color chromaticity measurement

(6) Definition of viewing angle coordinate system (θ_H , θ_V):

The contrast ratio is measured at the center point of the LCD module. The viewing angles are defined at the angle that the contrast ratio is larger than 10 at four directions relative to the perpendicular direction of the LCD module (two vertical angles: up θ_{V+} and down θ_{V-} ; and two horizontal angles: right θ_{H+} and left θ_{H-}) as illustrated in Fig. 6.6. The contrast ratio is measured by ELDIM EZ Contrast.

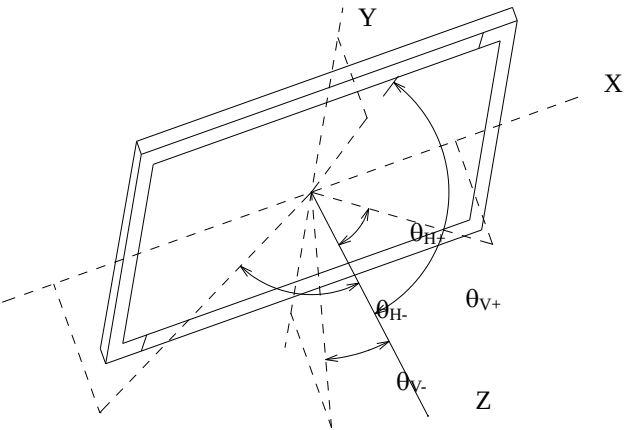
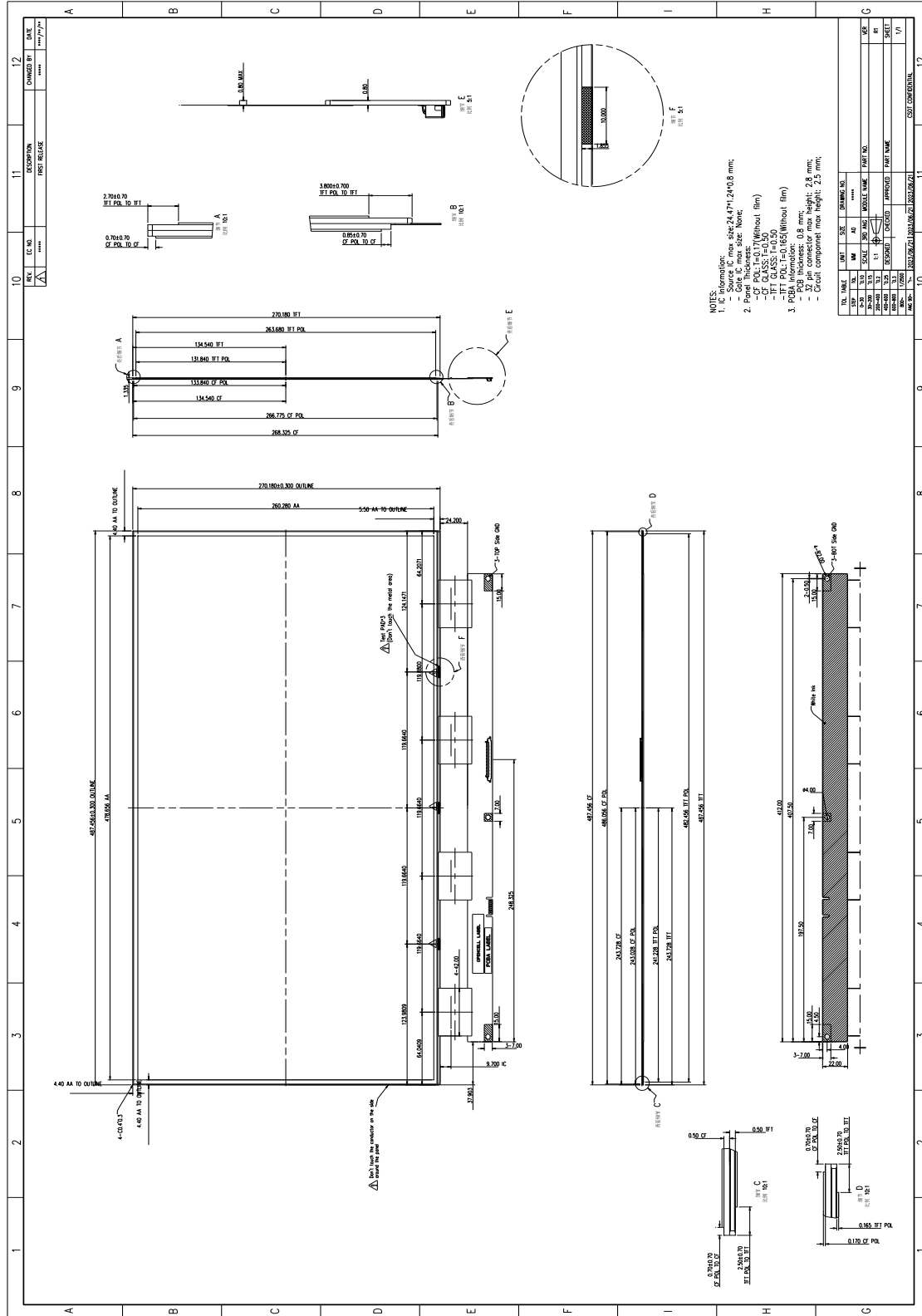


Fig. 6.6 Viewing angle coordination system

7. Mechanical Characteristics

7.1 Mechanical Specification



7.2 Packing

7.2.1 Packing Specifications

Item	Specification		
	Quantity	Dimension (mm)	Weight (kg)
Packing Box	20pcs/box	605 (L) x 480 (W) x125 (H)	Net Weight: 8.4 Gross Weight: 9.2
Pallet	1	1250 (L) x 1000 (W) x144 (H)	Net Weight: 17
Stack Layer	8		
Boxes per Pallet	32		
Pallet after Packing	640 pcs/pallet	1250 (L) x 1000 (W) x1099 (H)	Gross Weight: 313
Pallet Stack Layer	2 layers/Warehouse, 2 layers/40GP, 2 layers/40HQ.		

7.2.2 Packing Method

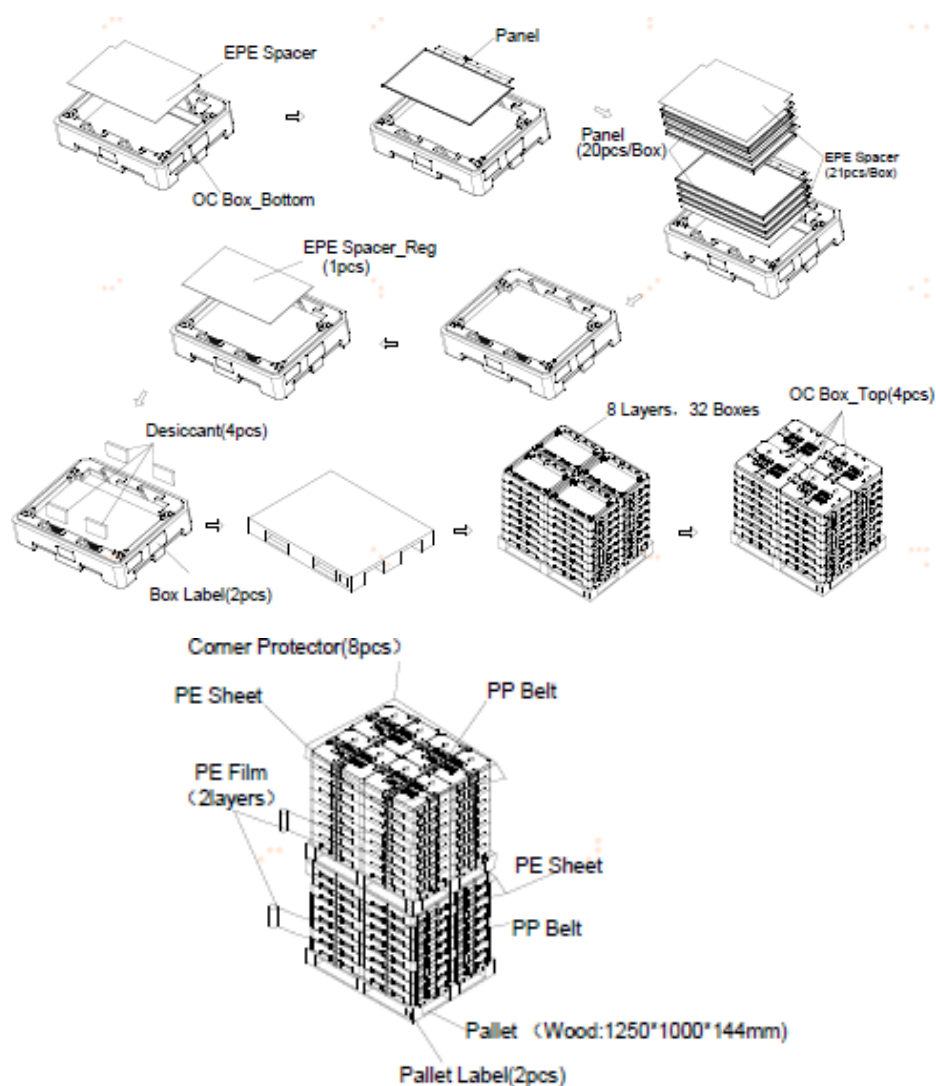


Fig. 7.1 Packing method

8. Precautions

8.1 Assembly and Handling Precautions

- (1) The device listed in the product specification sheets was designed and manufactured for CID application only.
- (2) Do not apply rough force such as bending or twisting to the open cell during assembly.
- (3) It is recommended to assemble or install an open cell into the user's system in clean working areas. The dust and oil may cause electrical short or damage the polarizer.
- (4) Do not apply pressure or impulse to the open cell to prevent the damage to the open cell.
- (5) Always follow the correct power-on sequence. This can prevent the damage and latch-up to the chips.
- (6) Do not plug in or pull out the interface connector while the open cell is in operation.
- (7) Use soft dry cloth without chemicals for cleaning because the surface of polarizer is very soft and easily be scratched.
- (8) Moisture can easily penetrate into the open cell and may cause the damage during operation.
- (9) High temperature or humidity may deteriorate the performance of the open cell. Please store open cell in the specified storage conditions.
- (10) When ambient temperature is lower than 10 °C, the display quality might be deteriorated. For example, the response time will become slow.
- (11) Any attachment on polarizer of open-cell , such as tape , is forbidden and not recommended , especially under the high temperature and high humidity environment.

8.2 Safety Precautions

- (1) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it should be washed away thoroughly with soap.
- (2) After the open cell end of life, it is not harmful in case of norm.

Appendix I Input Connector & FFC Drawing

