PRODUCT SPECIFICATION FOR LCD MODULE

Revision: 1.0

Model No: LSC0395I08-R-V1

Module Type: COG+FPC+B/L+LENS

APPROVED SIGNATURE

■ Approved Product Specification only

□ Approved Product Specification and Samples

Prepared By	Checked By	Approved By

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1. General Description

LSC0395I08-R-V1 is a transmissive type a-Si TFT-LCD (amorphous silicon thin film transistor liquid crystal display) module, which is composed of a TFT-LCD panel, a driver circuit and a backlight unit. The panel size is 3.95 inch and the resolution is 480(RGB)*480, the panel can display up to 16.7M colors.

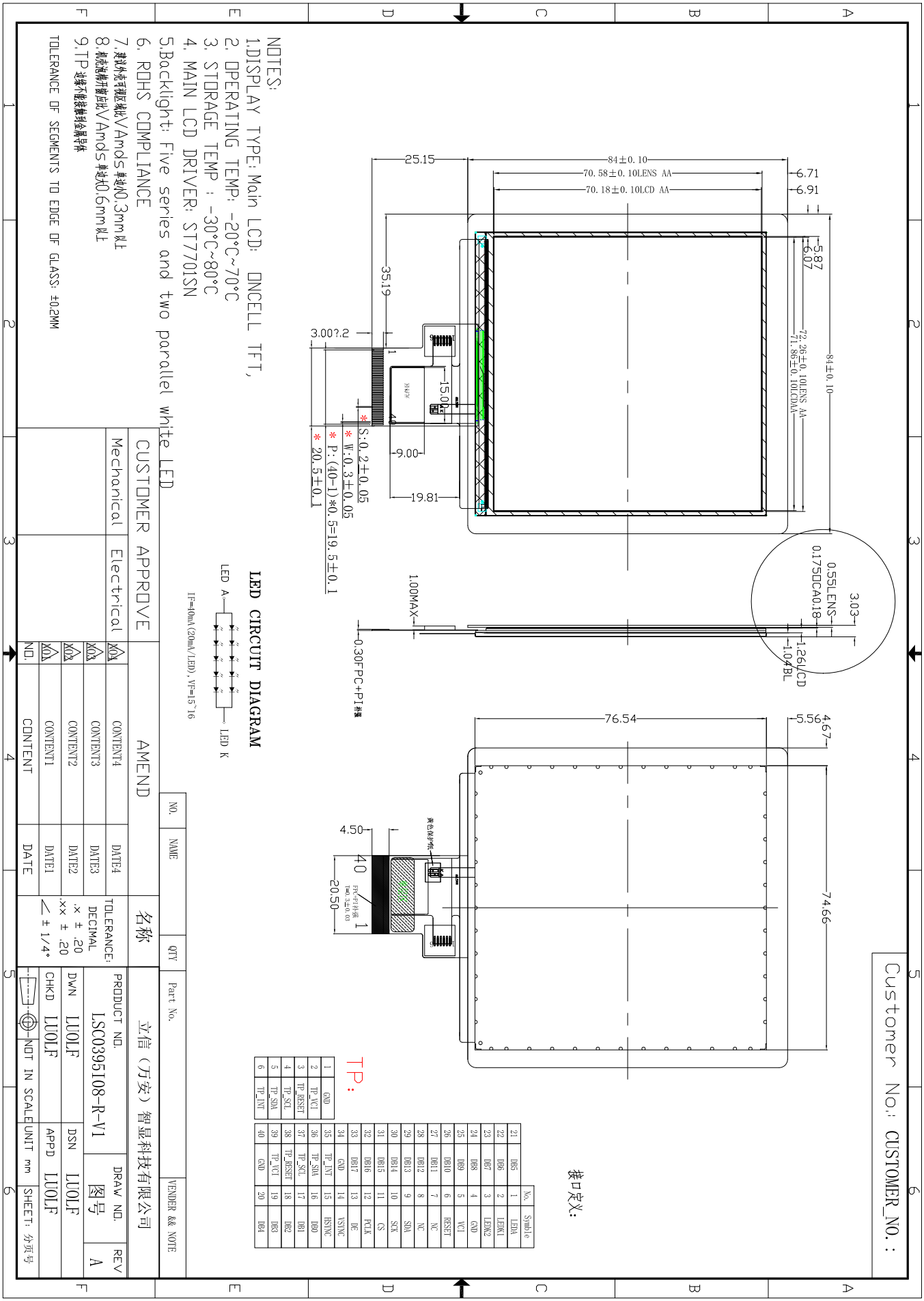
2. Physical Features

Display Mode	TFT-LCD Module
	Active matrix TFT, Transmissive type
Display Format	Graphic 480(RGB)×480Dot-matrix
Input Data	18 BIT RGB
Viewing Direction （Grayscale Inversion）	Free（IPS）
Drive	ST7701SN

3. Mechanical Specification

Item	Specification	Unit
Module size (H×V×D)	84 ×84×3.03	mm
Number of dots	480(RGB) ×480	pixel
Active area (H×V)	71.86×70.18	mm

4. Outline Dimension



5. Absolute Maximum Ratings

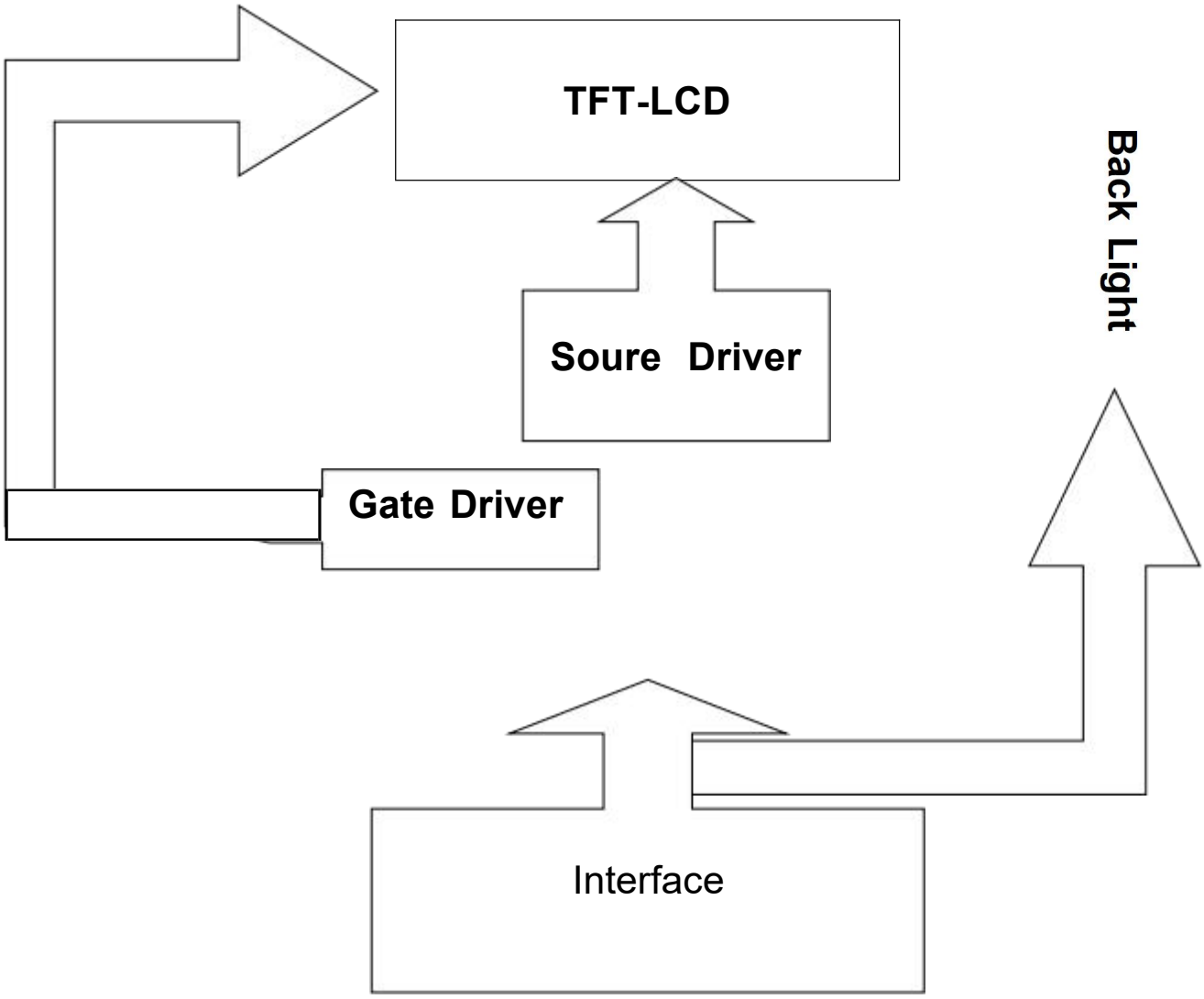
Item	Symbol	Min	Max	Unit	Remark
Supply voltage	VCC	-0.3	3.6	V	Note1 Note2
Supply voltage	IOVCC	-0.3	3.6	V	
Operating temperature	TOPR	-20	70	℃	
Storage temperature	TSTR	-30	80	℃	

6. Electrical Characteristics

Item		Symbol	Rating			Unit	Remark
			Min	Typ	Max		
Supply voltage		VCC	2.5	2.8	3.6	V	Note1
Supply voltage		IOVCC	1.65	1.8	3.3	V	
Input Voltage	L level	VIL	VSS	---	0.3*IOVCC	V	
	H level	VIH	0.7*IOVCC	---	IOVCC	V	

7. Module Function Description

7-1. Block Diagram Of LCM



7-2. Pin Description

PIN NO.	Symbol	I/O	Description
1	LEDA	P	Power for LED backlight anode
2	LEDK	P	Power for LED backlight cathode
3	LEDK	P	Power for LED backlight cathode
4	GND	P	Ground
5	VCI	P	Power voltage
6	RESET	I	The external reset input
7	NC		
8	NC		
9	SDA	I	Serial data input pin for SPI Interface
10	SCK	I	Serial clock input for SPI interface.
11	CS	I	A chip select signal Low: the chip is selected and accessible High: the chip is not selected and not accessible
12	PCLK	I	Dot clock signal for RGB interface operation
13	DE	I	Data enable signal for RGB interface operation Low: access enabled High: access inhibited
14	VSYNC	I	Frame synchronizing signal for RGB interface operation
15	HSYNC	I	Line synchronizing signal for RGB interface operation
16	DB0	I	parallel data bus
17	DB1	I	parallel data bus
18	DB2	I	parallel data bus
19	DB3	I	parallel data bus
20	DB4	I	parallel data bus
21	DB5	I	parallel data bus
22	DB6	I	parallel data bus
23	DB7	I	parallel data bus
24	DB8	I	parallel data bus
25	DB9	I	parallel data bus

26	DB10	I	parallel data bus
27	DB11	I	parallel data bus
28	DB12	I	parallel data bus
29	DB13	I	parallel data bus
30	DB14	I	parallel data bus
31	DB15	I	parallel data bus
32	DB16	I	parallel data bus
33	DB17	I	parallel data bus
34	GND	P	Ground
35	TP_INT	I/O	External interrupt to the host
36	TP_SDA	I/O	I2C data input and output
37	TP_SCL	I/O	I2C clock input
38	TP_RESET	I	Reset Pin
39	TP_VCI	P	Power voltage
40	GND	P	Ground

7-3 Timing Characteristics

7.5.1 Serial Interface Characteristics (3-line serial):

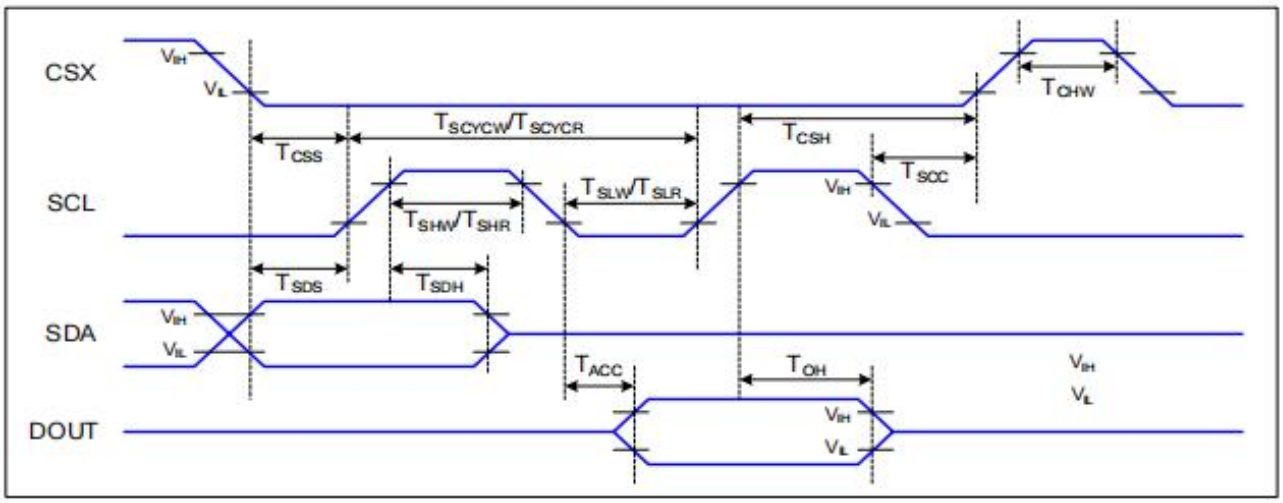


Figure 1 3-line serial Interface Timing Characteristics

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	Tcss	Chip select setup time (write)	15		ns	
	Tcsh	Chip select hold time (write)	15		ns	
	Tcss	Chip select setup time (read)	60		ns	
	Tscc	Chip select hold time (read)	60		ns	
	Tchw	Chip select "H" pulse width	40		ns	
SCL	Tscycw	Serial clock cycle (Write)	66		ns	
	Tshw	SCL "H" pulse width (Write)	15		ns	
	Tslw	SCL "L" pulse width (Write)	15		ns	
	Tscycr	Serial clock cycle (Read)	150		ns	
	Tshr	SCL "H" pulse width (Read)	60		ns	
	Tslr	SCL "L" pulse width (Read)	60		ns	
SDA (DIN)	Tsds	Data setup time	10		ns	
	Tsdh	Data hold time	10		ns	
SDO (DOUT)	Tacc	Access time	20	50	ns	Max: CL=30pF
	Toh	Output disable time	50	50	ns	Min: CL=8pF

Table 4 3-line serial Interface Characteristics

Note : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

7.5.3 RGB Interface Characteristics :

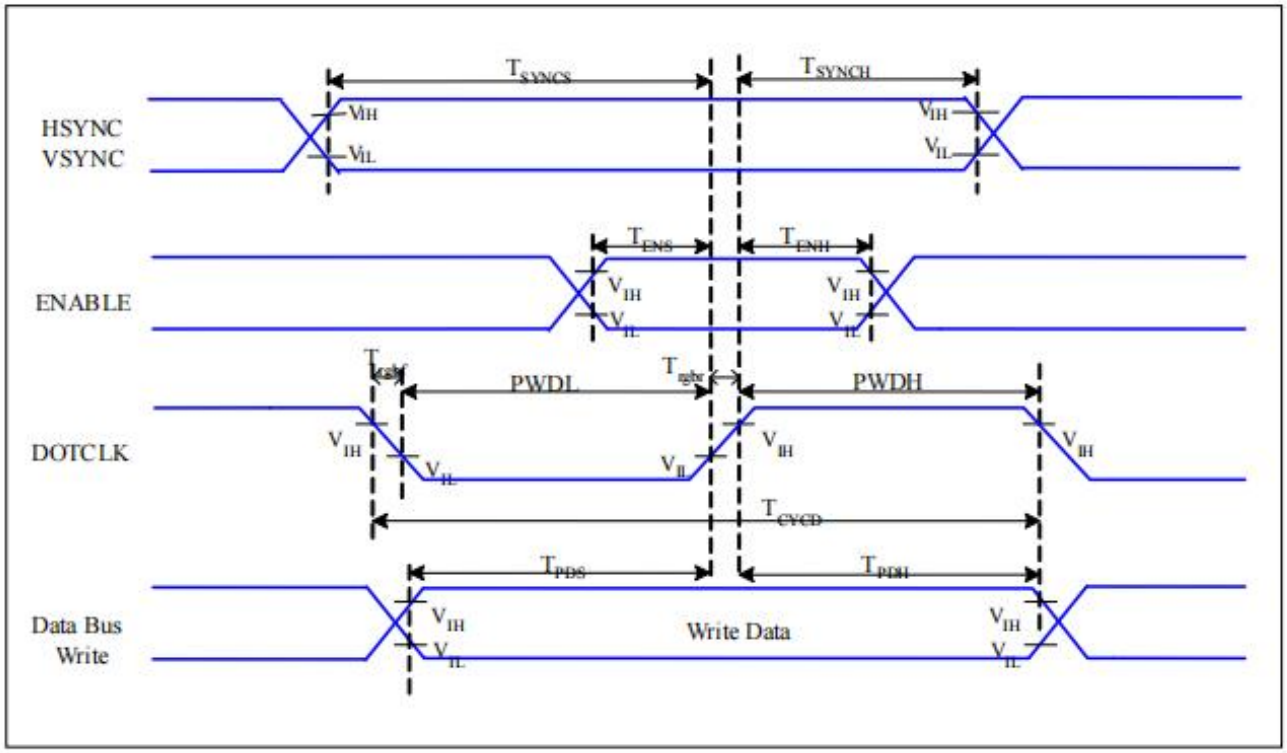


Figure 3 RGB Interface Timing Characteristics

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	5	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	5	-	ns	
	T_{ENH}	Enable Hold Time	5	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	15	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	15	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	33	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	15	ns	
DB	T_{PDS}	PD Data Setup Time	5	-	ns	
	T_{PDH}	PD Data Hold Time	5	-	ns	

Table 6 18/16 Bits RGB Interface Timing Characteristics

8. Electro-Optical Characteristics

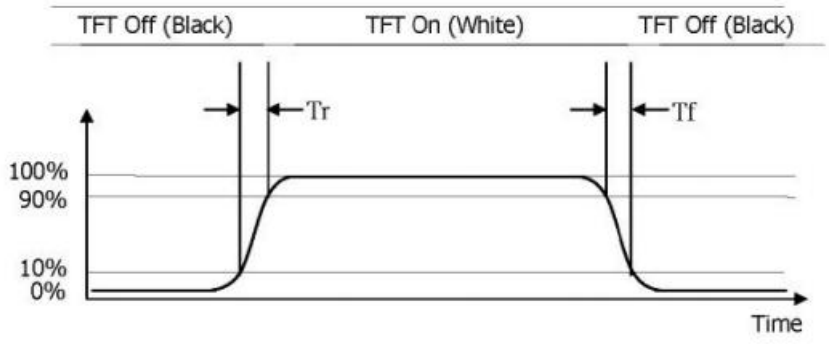
Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time		Tr +Tf	θx = θy =0	---	30	40	ms	Note 1
Contrast Ratio		CR		1000	1200	---	---	Note 2
Transmittance		T%		---	---	2	%	
Color Chromaticity (CIE1931)	White	W x	θx = θy =0	---	0.302	---	---	
		W y		---	0.337	---	---	
Viewing angle	θ_T		CR > 10	---	85	---	Deg.	Note 3
	θ_B			---	85	---		
	θ_L			---	85	---		
	θ_R			---	85	---		

Note :

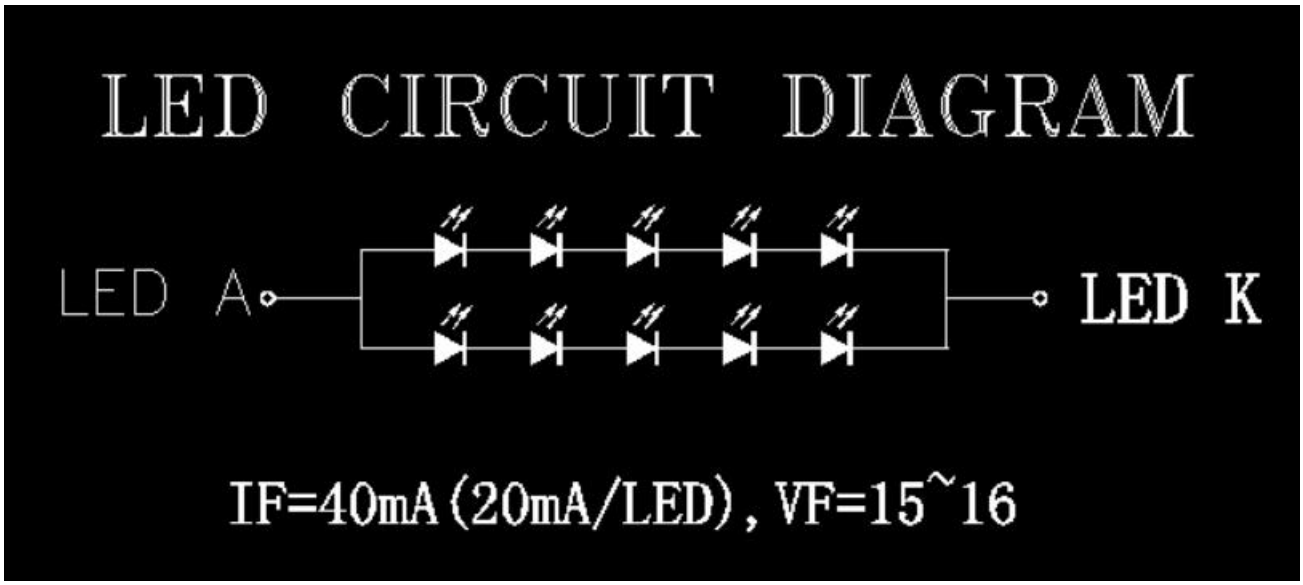
1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface.
2. Contrast measurements shall be made at viewing angle of θ= 0° and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (See FIGURE 1 shown in Appendix) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Center Luminance of white is defined as the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in FIGURE 4 for a total of the measurements per display.
4. The White luminance uniformity on LCD surface is then expressed as : ΔY = Minimum Luminance of 9 Points or 5 points / Maximum Luminance of 9 Points or 5 points(See FIGURE 2).
5. The color chromaticity coordinates specified in Table 5. shall be calculated from the spectral data measured with C light. Measurements shall be made at the center of the panel.
6. The electro-optical response time measurements shall be made as FIGURE 5 shown in Appendix by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Td, and 90% to 10% is Tr.



Note(4) Backlight circuit



9.Records Of Version

Version	Revise Date	Page	Content
00	2025-12-2	ALL	New released