

PRODUCT SPECIFICATION **FOR LCD MODULE**

Revision: 1.0

Model No: LS0146I02-M-V1

Module Type: COG+FPC+B/L

APPROVED SIGNATURE

- Approved Product Specification only
- Approved Product Specification and Samples

<u>Prepared By</u>	<u>Checked By</u>	<u>Approved By</u>

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1. General Description

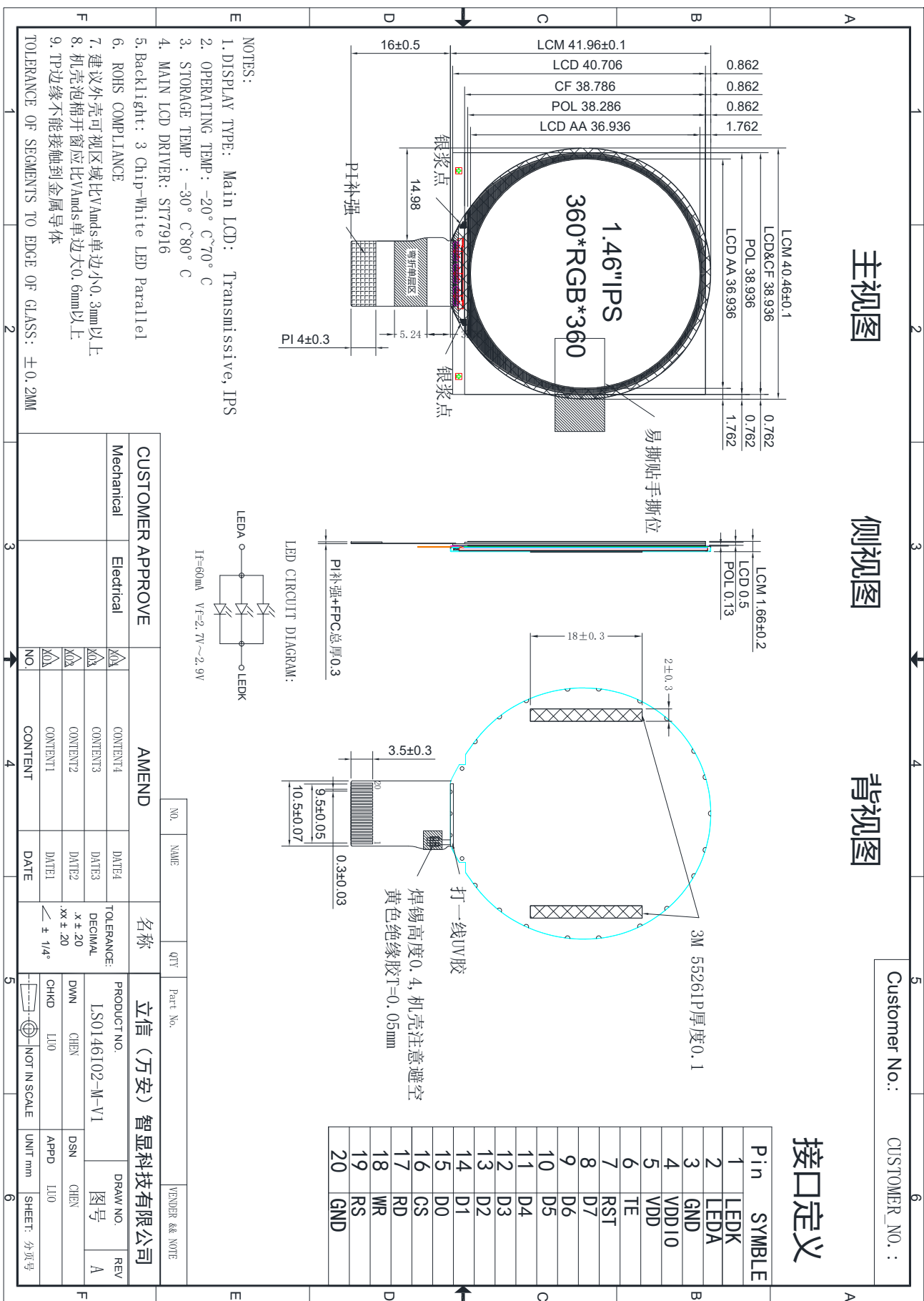
LS0146I02-M-V1 is a transmissive type a-Si TFT-LCD (amorphous silicon thin film transistor liquid crystal display) module, which is composed of a TFT-LCD panel, a driver circuit and a backlight unit. The panel size is 1.46 inch and the resolution is 360(RGB)*360, the panel can display up to 262k colors.

Display Mode	TFT-LCD Module
	Active matrix TFT, Transmissive type
Display Format	Graphic 360(RGB)×360 Dot-matrix
Input Data	8bit 8080
Viewing Direction (Grayscale Inversion)	Free (IPS)
Drive	ST77916

3. Mechanical Specification

Item	Specification	Unit
Module size (H×V×D)	40.464 ×41.96 ×1.66	mm
Number of dots	360(RGB) ×360	pixel
Active area (H×V)	36.936×36.936	mm

4. Outline Dimension



5. Absolute Maximum Ratings

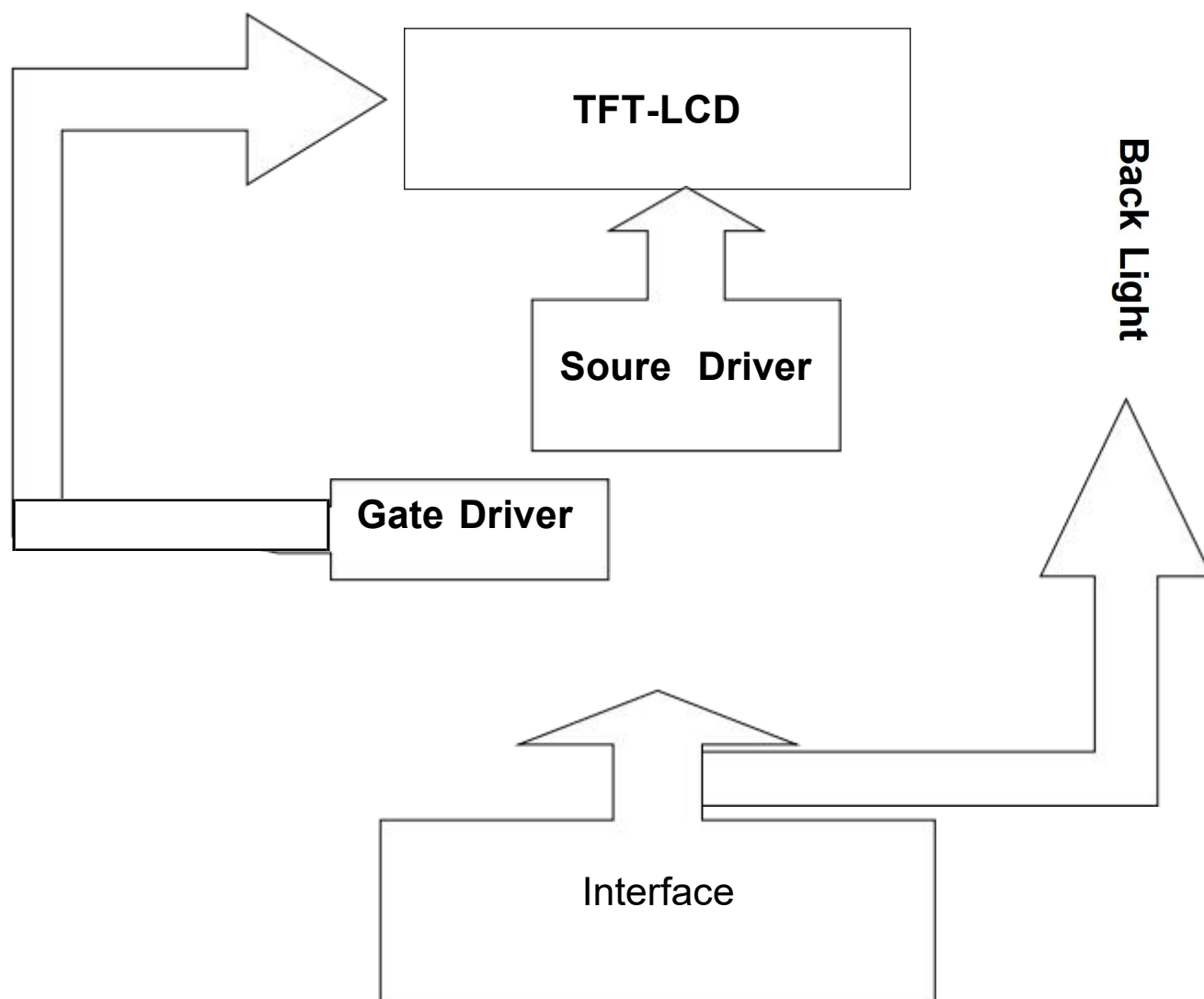
Item	Symbol	Min	Max	Unit	Remark
Supply voltage	VCC	-0.3	4.6	V	Note1 Note2
Supply voltage	IOVCC	-0.3	4.6	V	
Operating temperature	TOPR	-20	70	°C	
Storage temperature	TSTR	-30	80	°C	

6. Electrical Characteristics

Item		Symbol	Rating			Unit	Remark
			Min	Typ	Max		
Supply voltage		VCC	2.65	2.8	3.3	V	Note1
Supply voltage		IOVCC	1.65	1.8	3.3	V	
Input Voltage	L level	VIL	0	---	0.3*IOVCC	V	
	H level	VIH	0.7*IOVCC	---	IOVCC	V	

7. Module Function Description

7- 1. Block Diagram Of LCM



7-2. Pin Description

PIN NO.	Symbol	I/O	Description
1	LEDK	P	Power for LED backlight cathode
2	LEDA	P	Power for LED backlight anode
3	GND	P	Ground
4	VDDIO	P	power supply
5	VDD	P	power supply
6	TE	O	Tearing effect signal is used to synchronize MCU to frame memory writing
7	RST	I	Reset pin.
8	D7	I	data bus
9	D6	I	data bus
10	D5	I	data bus
11	D4	I	data bus
12	D3	I	data bus
13	D2	I	data bus
14	D1	I	data bus
15	D0	I	data bus
16	CS	I	Chip select pin
17	RD	I	Read enable in MCU parallel interface
18	WR	I	Write enable in MCU parallel interface
19	RS	I	Display data/command selection pin in parallel interface. DCX='1': display data or parameter. DCX='0': command data.
20	GND	P	Ground

The timing diagram illustrates the relationship between several control and data signals during a memory access cycle. The signals and their timing parameters are as follows:

- CSX (Chip Select):** Shows a pulse with high voltage V_H and low voltage V_L . Key timing parameters include T_{CHW} (chip select high-to-low delay), T_{CS} (chip select pulse width), T_{CSH} (chip select low-to-high delay), and T_{CSF} (chip select fall time).
- D/CX (Data/Command):** A bidirectional signal that can be driven by the processor or the memory. It shows a transition from high to low and back to high. Key timing parameters include T_{AST} (address-to-strobe delay), T_{WC} (write command delay), and T_{AHT} (address hold time).
- WRX (Write Strobe):** A pulse indicating a write operation. Key timing parameters include T_{WRH} (write strobe high-to-low delay), T_{WRH} (write strobe pulse width), and T_{DHT} (data hold time).
- D[7:0] write:** The data bus during a write operation. Key timing parameters include T_{RCS}/T_{RCSFM} (read-to-command delay), T_{AHT} (address hold time), and T_{RDH}/T_{RDHFM} (read-to-data delay).
- RDX (Read Strobe):** A pulse indicating a read operation. Key timing parameters include T_{AST} (address-to-strobe delay), T_{RDH}/T_{RDHFM} (read-to-data delay), and T_{RDH}/T_{RDHFM} (read-to-data delay).
- D[7:0] read:** The data bus during a read operation. Key timing parameters include T_{RAT}/T_{RATFM} (read-to-address delay), T_{ODH} (output delay), and T_{RDH}/T_{RDHFM} (read-to-data delay).

VDDI=1.65 to 3.3V, VDD=2.65 to 3.3V, GND=RGND=0V, Ta=25°C

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T _{AST}	Address setup time	0		ns	
	T _{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T _{CHW}	Chip select "H" pulse width	0		ns	
	T _{CS}	Chip select setup time (Write)	15		ns	
	T _{RCS}	Chip select setup time (Read ID)	45		ns	
	T _{RCSFM}	Chip select setup time (Read FM)	355		ns	
	T _{CSF}	Chip select wait time (Write/Read)	10		ns	
	T _{CSH}	Chip select hold time	10		ns	
WRX	T _{WC}	Write cycle	30		ns	
	T _{WRH}	Control pulse "H" duration	14		ns	
	T _{WRL}	Control pulse "L" duration	14		ns	
RDX (ID)	T _{RC}	Read cycle (ID)	160		ns	When read ID data
	T _{RDH}	Control pulse "H" duration (ID)	90		ns	
	T _{RDL}	Control pulse "L" duration (ID)	45		ns	
RDX (FM)	T _{RCFM}	Read cycle (FM)	450		ns	When read from frame memory
	T _{RDHFM}	Control pulse "H" duration (FM)	90		ns	

	T_{RDLFM}	Control pulse "L" duration (FM)		355		ns	
D[7:0]	T_{DST}	Data setup time		10		ns	For CL=30pF
	T_{DHT}	Data hold time		10		ns	
	T_{RAT}	Read access time (ID)			40	ns	
	T_{RATFM}	Read access time (FM)			340	ns	
	T_{ODH}	Output disable time		20	80	ns	

Table 1 8080 Parallel Interface Characteristics



Figure 2 Rising and Falling Timing for I/O Signal

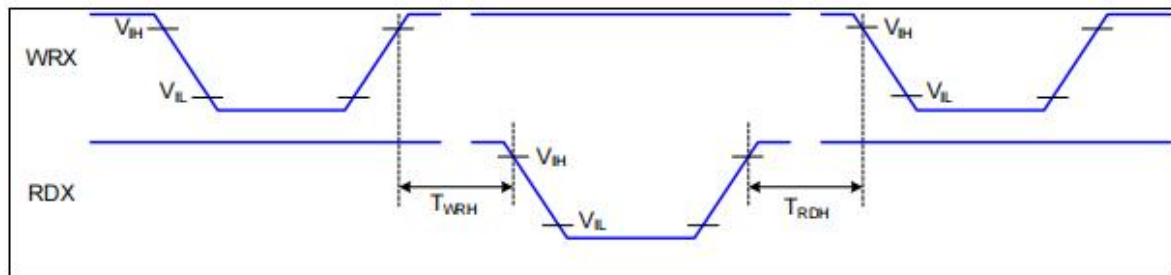
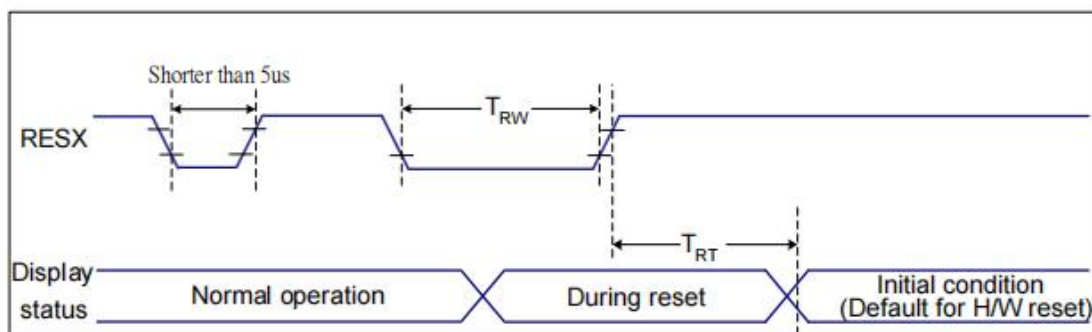


Figure 3 Write-to-Read and Read-to-Write Timing

Note: The rising time and falling time (T_R , T_F) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

7.4.7 Reset Timing



VDDI=1.8V, VDD=2.8V, GND=RGND=0V, Ta=25°C

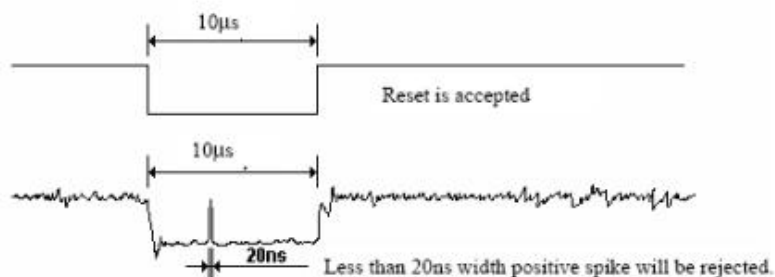
Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
			-	120 (Note 1, 6, 7)	ms

Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (TRT) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown below:



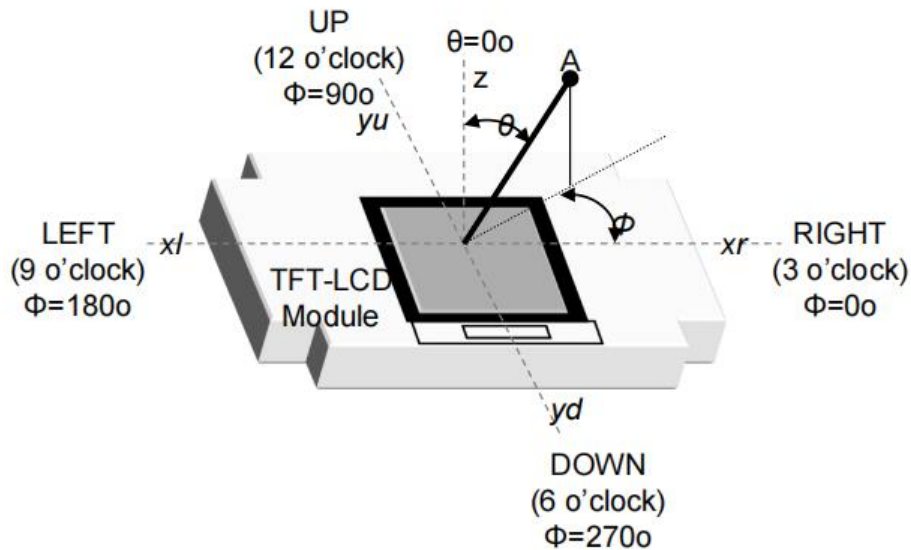
5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

8. Electro-Optical Characteristics

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time		Tr +Tf	$\theta_x = \theta_y = 0$	---	30	35	ms	Note 1
Contrast Ratio		CR		900	1200	---	---	Note 2
Transmittance		T%		2.5	2.94	---	%	
Color Chromaticity (CIE1931)	White	W x	$\theta_x = \theta_y = 0$	---	0.294	---	---	
		W y		---	0.323	---	---	
Viewing angle	θ_T		CR > 10	80	85	---	Deg.	Note 3
	θ_B			80	85	---		
	θ_L			80	85	---		
	θ_R			80	85	---		

Note 4.1: Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see Figure 8).

<Figure 8. Viewing Angle Range Is Defined As Follows>



Note 4.2: Contrast measurements shall be made at viewing angle of $\Theta=0^\circ$ and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. Luminance Contrast Ratio (CR) is defined mathematically.

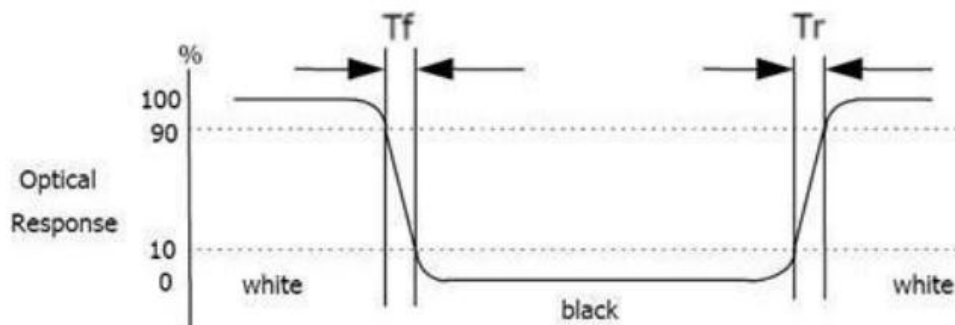
$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

Note 4.3: Transmittance is the Value with out **APF** Polarizer.

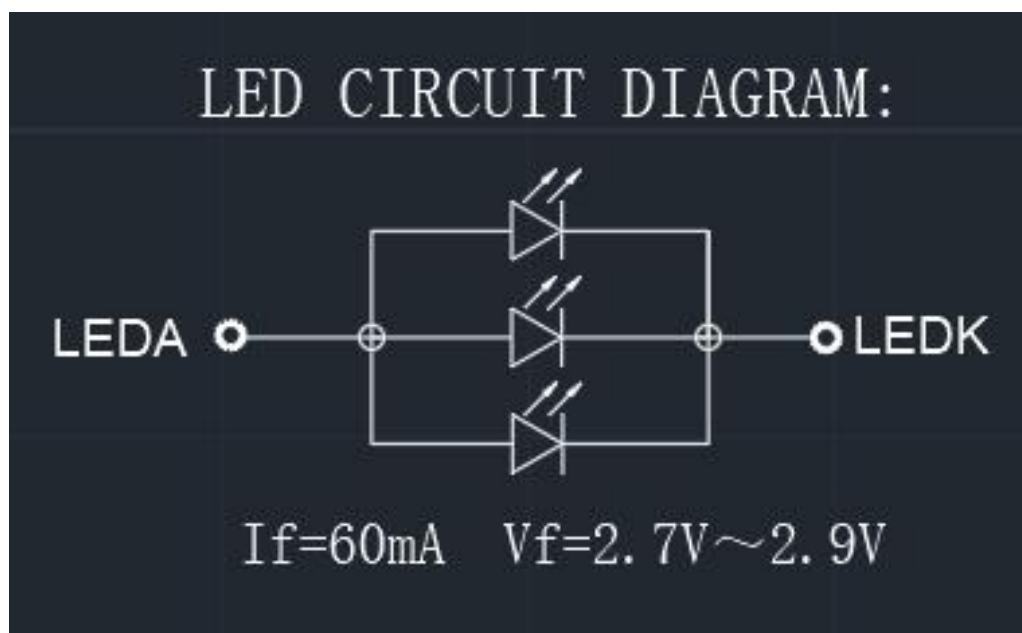
Note 4.4: The color chromaticity coordinates specified in Table 16 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

Note 4.5: The electro-optical response time measurements shall be made as Figure 9 by switching the “data” input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is T_r , and 90% to 10% is T_f .

<Figure 9. Response Time Testing>



Note(4) Backlight circuit



9.Records Of Version

Version	Revise Date	Page	Content
00	2026-1-20	ALL	New released