PRODUCT SPECIFICATION FOR LCD MODULE

Revision: 1.0

Model No: LSC101I34-MP-V1

Module Type: COG+FPC+B/L+CTP

APPROVED SIGNATURE

■ Approved Product Specification only

□ Approved Product Specification and Samples

Prepared By	Checked By	Approved By

Contents

目录

1. General Description

LSC101I34-MP-V1 is a transmissive type a-Si TFT-LCD (amorphous silicon thin film transistor liquid crystal display) module, which is composed of a TFT-LCD panel, a driver circuit and a backlight unit. The panel size is 10.1 inch and the resolution is 800(RGB)*1280, the panel can display up to 16.7M colors.

2. Physical Features

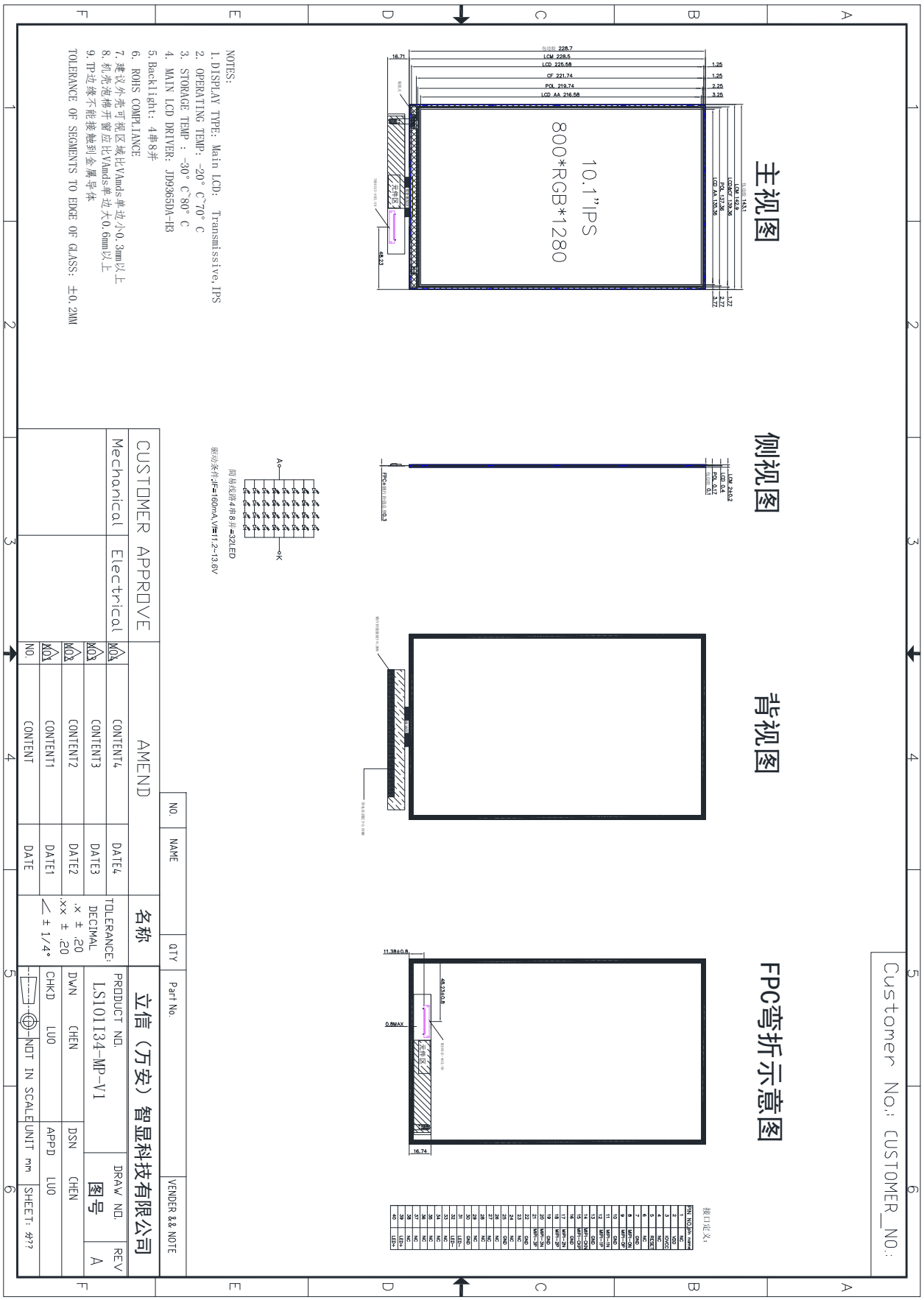
Display Mode	TFT-LCD Module
	Active matrix TFT, Transmissive type
Display Format	Graphic 800(RGB)×1280 Dot-matrix
Input Data	MIPI
Viewing Direction （Grayscale Inversion）	Free（IPS）
Drive	JD9365DA-H3

3. Mechanical Specification

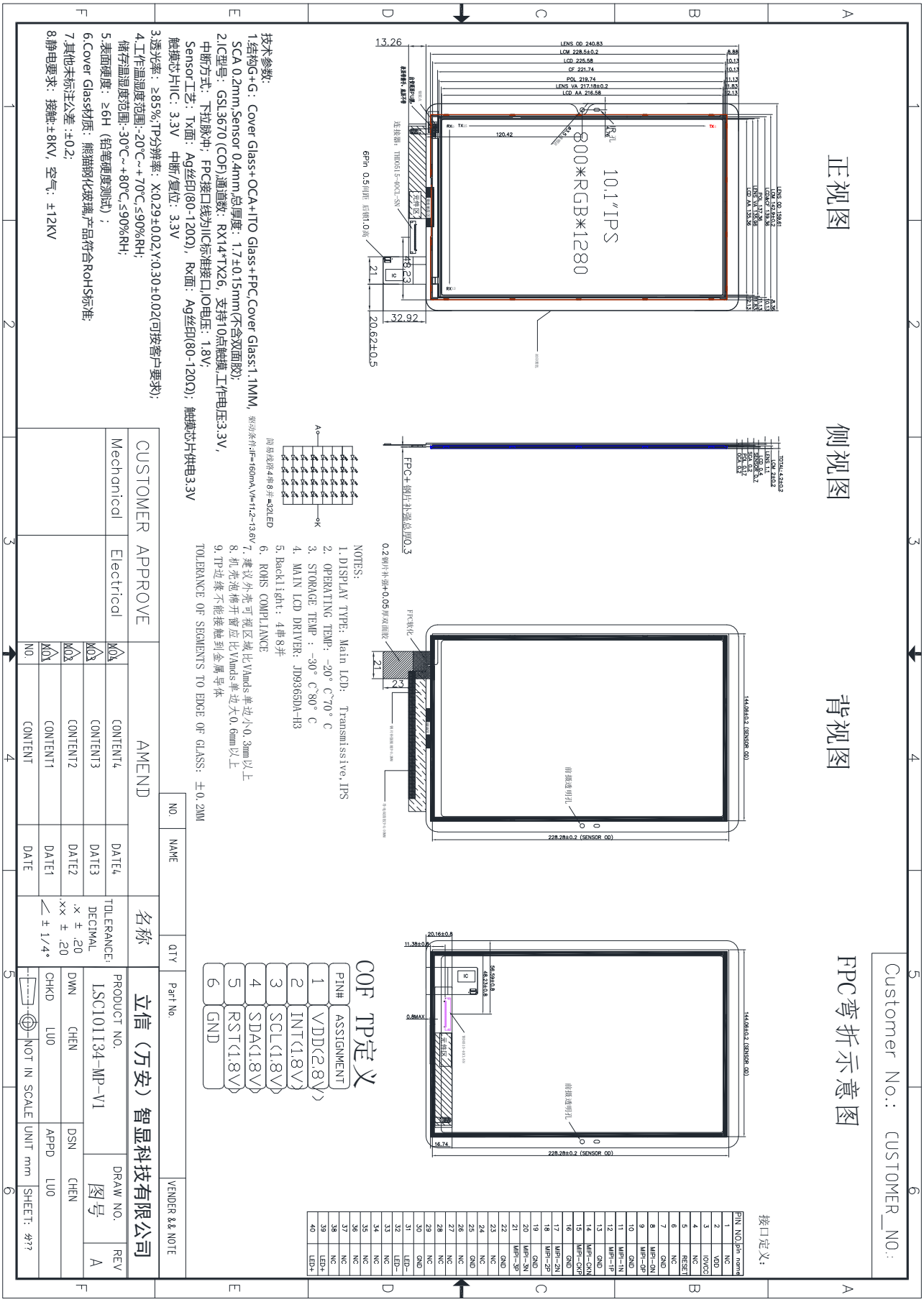
Item	Specification	Unit
Module size (H×V×D)	159.61 ×240.83 ×4.2	mm
Number of dots	800(RGB) ×1280	pixel
Active area (H×V)	135.36×216.58	mm

4. Outline Dimension

LCM



LCM+CTP


正视图
侧视图
背视图
FPC弯折示意图
Customer No.: CUSTOMER_NO.:
10.1"IPS
800*RGB*1280
技术参数:
1.结构G+G: Cover Glass+OCA+ITO Glass+FPC,Cover Glass:1.1MM,
SCA 0.2mm,Sensor 0.4mm,总厚度: 1.7±0.15mm(不含双面胶);
2.IC型号: GSL3670 (COF),通道数: RX14*TX26, 支持10点触摸,工作电压3.3V,
中断方式: 下拉脉冲; FPC接口线为IC标准接口,IO电压: 1.8V;
Sensor工艺: Tx面: Ag丝印(80-120Ω), Rx面: Ag丝印(80-120Ω); 触摸芯片供电3.3V
触摸芯片IIC: 3.3V 中断/复位: 3.3V
3.透光率: ≥85%;TP分辨率: X:0.29±0.02,Y:0.30±0.02(可按客户要求);
4.工作温湿度范围:-20℃~+70℃,≤90%RH;
储存温湿度范围:-30℃~+80℃,≤90%RH;
5.表面硬度: ≥6H (铅笔硬度测试) ;
6.Cover Glass材质: 熊猫钢化玻璃,产品符合RoHS标准;
7.其他未标注公差 :±0.2;
8.静电要求: 接触±8KV, 空气: ±12KV
NOTES:
1. DISPLAY TYPE: Main LCD: Transmissive,IPS
2. OPERATING TEMP: -20° C~70° C
3. STORAGE TEMP : -30° C~80° C
4. MAIN LCD DRIVER: JD9365DA-H3
5. Backlight: 4串8并
6. ROHS COMPLIANCE
7. 建议 外壳可视区域 比VAmds单边小0.3mm以上
8. 机壳油棉开窗应比VAmds单边大0.6mm以上
9. TP边缘不能接触到金属导体
TOLERANCE OF SEGMENTS TO EDGE OF GLASS: ±0.2MM
COF TP定义
PIN# ASSIGNMENT
1 VDD(2.8V)
2 INT(1.8V)
3 SCL(1.8V)
4 SDA(1.8V)
5 RST(1.8V)
6 GND
接口定义:
CUSTOMER APPROVE
Mechanical
Electrical
AMEND
名称
立信（万安）智显科技有限公司
PRODUCT NO. LSC101I34-MP-V1
DRAW NO. 图号
REV A
DESIGN CHEN
DSN CHEN
CHKD LUO
APPD LUO
UNIT mm
SHEET: 分??
NOT IN SCALE
TOLERANCE DECIMAL .x ± .20 .xx ± .20 ∠ ± 1/4°
NO. NAME QTY Part No. VENDER && NOTE
CONTENT4 DATE4
CONTENT3 DATE3
CONTENT2 DATE2
CONTENT1 DATE1
CONTENT DATE

5. Absolute Maximum Ratings

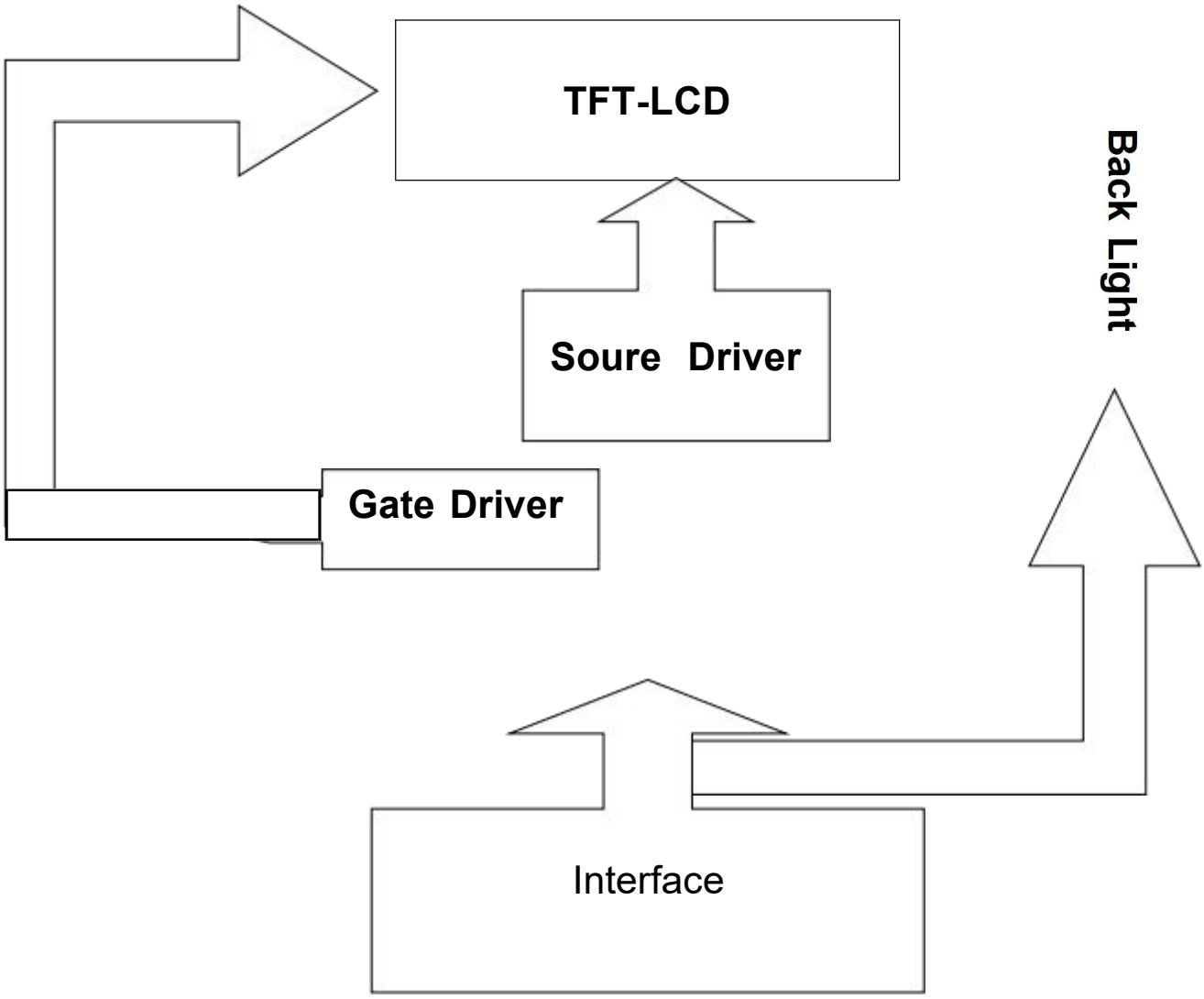
Item	Symbol	Min	Max	Unit	Remark
Supply voltage	VCC	-0.3	3.6	V	Note1 Note2
Supply voltage	IOVCC	-0.3	3.6	V	
Operating temperature	TOPR	-20	70	℃	
Storage temperature	TSTR	-30	80	℃	

6. Electrical Characteristics

Item		Symbol	Rating			Unit	Remark
			Min	Typ	Max		
Supply voltage		VCC	2.5	3.3	---	V	Note1
Supply voltage		IOVCC	---	1.8	---	V	
Input Voltage	L level	VIL	0	---	0.3*IOVCC	V	
	H level	VIH	0.7*VCC	---	IOVCC	V	

7. Module Function Description

7-1. Block Diagram Of LCM



7-2. Pin Description

PIN NO.	Symbol	I/O	Description
1	NC		
2	VDD	P	Power supply
3	IOVCC	P	Power supply
4	NC		
5	RESET	I	Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied
6	NC		
7	GND	P	ground
8	D0N	I/O	MIPI-DSI Data differential signal input pins. (Data lane 0)
9	D0P	I/O	MIPI-DSI Data differential signal input pins. (Data lane 0)
10	GND	P	ground
11	D1N	I	MIPI-DSI Data differential signal input pins. (Data lane 1)
12	D1P	I	MIPI-DSI Data differential signal input pins. (Data lane 1)
13	GND	P	ground
14	CLKN	I	MIPI-DSI CLOCK differential signal input pins
15	CLKP	I	MIPI-DSI CLOCK differential signal input pins
16	GND	P	ground
17	D2N	I	MIPI-DSI Data differential signal input pins. (Data lane 2)
18	D2P	I	MIPI-DSI Data differential signal input pins. (Data lane 2)
19	GND	P	ground
20	D3N	I	MIPI-DSI Data differential signal input pins. (Data lane 3)
21	D3P	I	MIPI-DSI Data differential signal input pins. (Data lane 3)
22	GND	P	ground
23	NC		
24	NC		
25	GND	P	ground
26	NC		

27	NC		
28	NC		
29	NC		
30	GND	P	ground
31	LED-	P	Power for LED backlight cathode
32	LED-	P	Power for LED backlight cathode
33	NC		
34	NC		
35	NC		
36	NC		
37	NC		
38	NC		
39	LED+	P	Power for LED backlight anode
40	LED+	P	Power for LED backlight anode

7-3 Timing Characteristics

The Description of D-PHY Layer

In general, the DSI - PHY may contain the following electrical functions: Low-Power Receiver (LP-RX), High-Speed Receiver (HS-RX), the Low-Power Contention Detector (LP-CD), and Low Power Transmitter (LP-TX). Figure 13.2 shows the complete set of electronic functions required for a fully featured PHY transceiver.

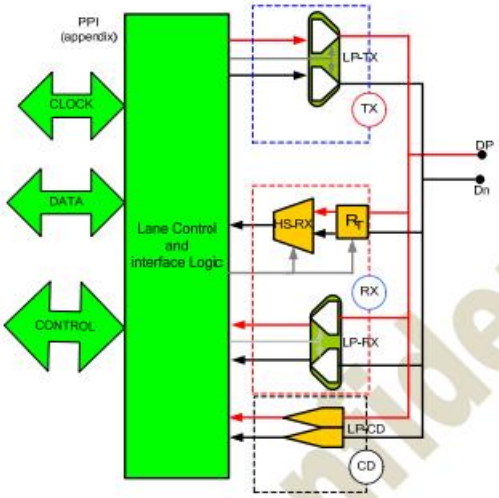
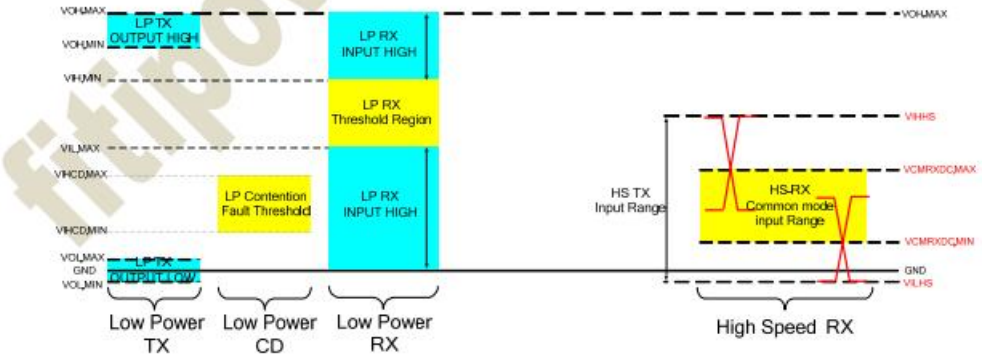


Figure 11.2: Electronic functions of a D-PHY transceiver

Figure13.3 shows both the HS and LP signal levels of electronic characteristics, respectively. Where, the HS receiver utilizes low-voltage swing differential signaling. The LP transmitter and LP receiver utilize low-voltage swing single signaling. Because the HS signaling levels are below the LP low-level input threshold, Lane switches between Low-Power and High-Speed mode during normal operation.



The Electronic Characteristics of Low-Power Transmitter (TX)

The Low-Power TX shall be a slew-rate controlled push-pull driver. It is used for driving the Lines in all Low-Power modes. Hence, it is important to keep static power consumption of a LP TX be as low as possible. Under tables list DC and AC characteristic for Low power transmitter.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{OH}	Thevenin output high level	1.1	1.2	1.3	V	-
V_{OL}	Thevenin output low level	-50	-	50	mV	
Z_{OLP}	Output impedance of LP-TX	110	-	-	Ω	(1)

Note: (1)Though no maximum value for Z_{OLP} is specified, the LP transmitter output impedance shall ensure the t_{RLP}/t_{FLP} specification is met.

Table 11.4: LP-TX DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
t_{RLP}/t_{FLP}	15%-85% rise time and fall time	-	-	25	ns	(1)
$T_{LP\text{-}PER\text{-}TX}$	Period of the LP exclusive-OR clock	90			ns	
$\delta V/\delta t_{SR}$	Slew rate @ CLOAD = 0pF	30	-	500	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 5pF	-	-	300	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 20pF	-	-	250	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 70pF	-	-	150	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 0 to 70pF (Rising Edge Only)	30	-	-	mV/ns	(1),(3),(7)
	Slew rate @ CLOAD = 0 to 70pF (Rising Edge Only)	30 – 0.075 * (VO,INST- 700)	-	-	mV/ns	(1),(8),(9)
	Slew rate @ CLOAD = 0 to 70pF (Falling Edge Only)	30	-	-	mV/ns	(1),(2),(3)
C_{LOAD}	Load capacitance	-	-	70	pF	-

Note: (1) CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.
(2) When the output voltage is between 400 mV and 930 mV.
(3) Measured as average across any 50 mV segment of the output signal transition.
(4) This parameter value can be lower than TLPX due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters.
(5) This value represents a corner point in a piecewise linear curve.
(6) When the output voltage is in the range specified by VPIN(absmax).
(7) When the output voltage is between 400 mV and 700 mV.
(8) Where VO,INST is the instantaneous output voltage, VDP or VDN, in millivolts.
(9) When the output voltage is between 700 mV and 930 mV.

Table 11.5: LP-TX AC Specifications

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 8.13. Data is launched in a quadrature relationship to the clock such that the Clock signal edge may be used directly by the receiver to sample the received data.

The transmitter shall ensure that a rising edge of the DDR clock is sent during the first payload bit of a transmission burst such that the first payload bit can be sampled by the receiver on the rising clock edge, the second bit can be sampled on the falling edge, and all following bits can be sampled on alternating rising and falling edges.

All timing values are measured with respect to the actual observed crossing of the Clock differential signal. The effects due to variations in this level are included in the clock to data timing budget.

Receiver input offset and threshold effects shall be accounted as part of the receiver setup and hold parameters.

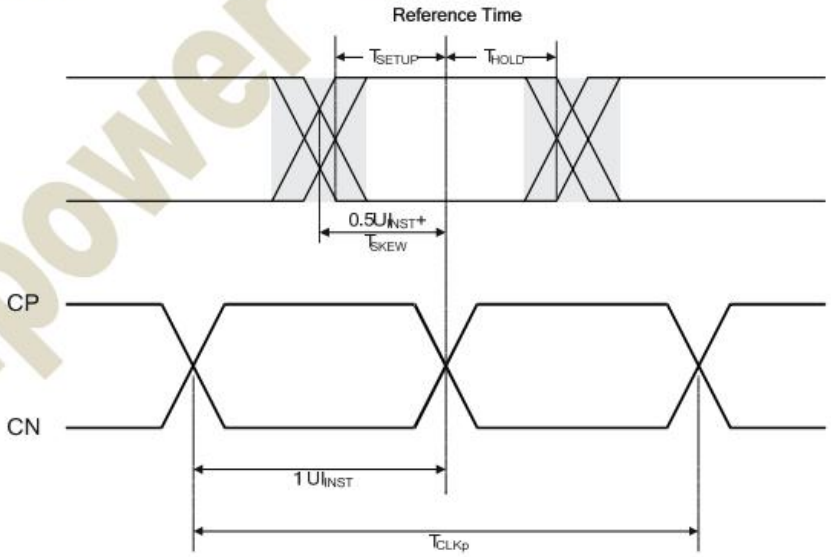


Figure 11.6: Data to Clock Timing Definitions

Burst Mode Data Transmission

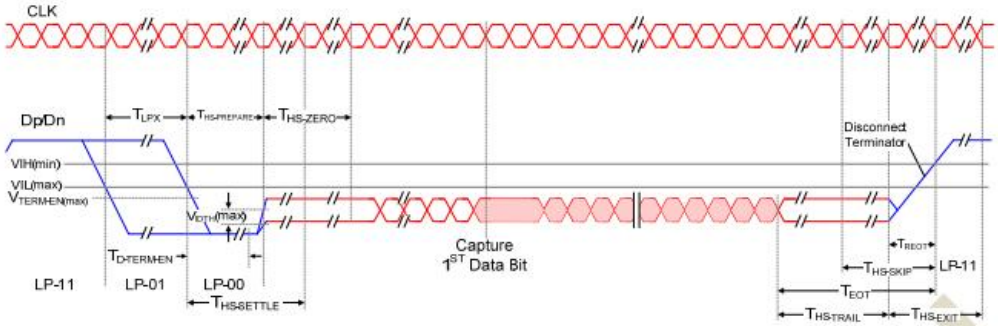


Figure 11.7: High-Speed Data Transmission in Bursts

Parameter	Description	Min	Typ	Max	UNIT
T_{LPX}	Transmitted length of any Low-Power state period	50	-	-	ns
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40 + 4*UI	-	85 + 6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145 + 10*UI	-	-	ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination.	-	-	35 + 4*UI	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions.	85 + 6*UI	-	145 + 10*UI	ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	max(n*8*UI, 60 + n*4*UI)	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns

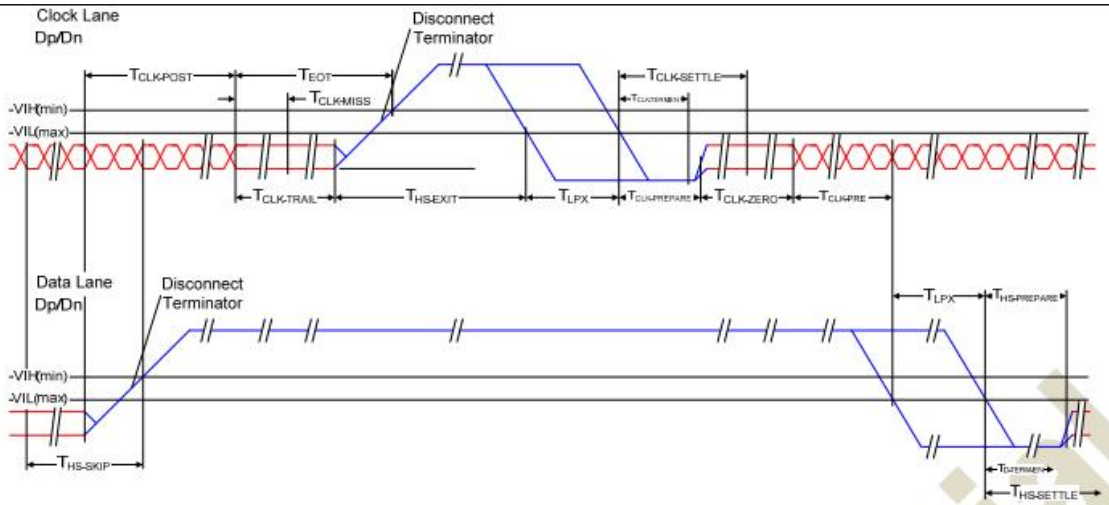


Figure 11.8: Switching the Clock Lane between Clock Transmission and Low-Power Mode

Parameter	Description	Min	Typ	Max	UNIT
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode.	60 + 52*UI	-	-	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8*UI	-	-	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38	-	95	ns
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300	-	-	ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination.	-	-	38	ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns

Vertical Timings

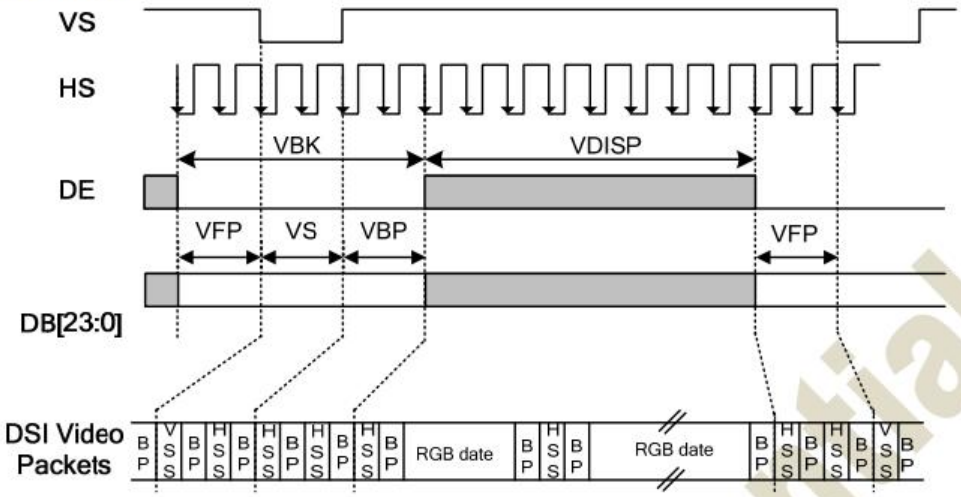


Figure 11.9: Vertical Timings for DPI I/F

Resolution=800x1280(T_A=25°C, IOVCC=1.8V, VCIP=2.8V, VCI=2.8V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical low pulse width	VS	-	2	4	200 Note(1)	Line
Vertical front porch	VFP	-	4	20	200	Line
Vertical back porch	VBP	-	2	10	200 Note(1)	Line
Vertical blanking period	VBK	VS+VBP+VFP	8	34	250	Line
Vertical active area	-	VDISP	-	1280	-	Line
Vertical Refresh rate	VRR	-	-	60	-	Hz

Note: (1) The VS and VBP pulse width are related to GIP start pulse and GIP clock pulse timing. The GIP start pulse and GIP clock pulse must be set at corresponding position for LCD normal display.

Horizontal Timings

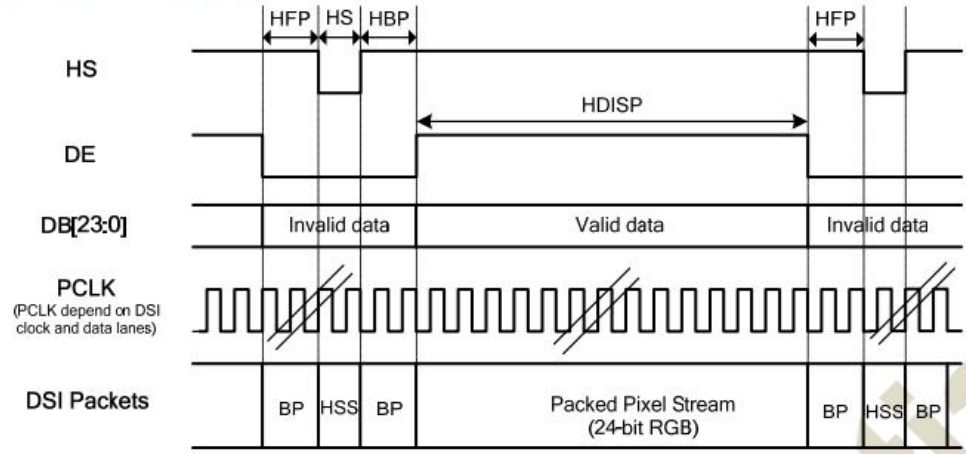


Figure 11.10: Horizontal Timing for DSI Video mode I/F

Resolution=800x1280 (T_A=25°C, IOVCC=1.8V, VCIP=VCI=VCCH=2.8V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HS low pulse width	HS	-	6	18	78	DCK
Horizontal back porch	HBP	-	5	18	78	DCK
Horizontal front porch	HFP	-	5	18	78	DCK
Horizontal blanking period	HBLK	HS+HBP+HFP	16	54 (Note1)	88	DCK
Horizontal active area	HDISP	-	-	800	-	DCK
Pixel Clock	PCLK	-	63.06 (Note2)	67.33 (Note2)	81.51 (Note2)	MHz

Note 1: HS+HBP > 0.5us.
Note 2: Pixel Clock = (HBLK+HDISP) * (VBK+VDISP) * Frame rate, Frame rate=60Hz.

8. Electro-Optical Characteristics

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time		Tr +Tf	θx = θy =0	---	25	35	ms	Note 1
Contrast Ratio		CR		800	1000	---	---	Note 2
Transmittance		T%		4.65	5.41	---	%	
Color Chromaticity (CIE1931)	White	W x	θx = θy =0	---	0.302	---	---	
		W y		---	0.329	---	---	
Viewing angle	θ_T		CR > 10	---	80	---	Deg.	Note 3
	θ_B			---	80	---		
	θ_L			---	80	---		
	θ_R			---	80	---		

*Note(1) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L255 / L0

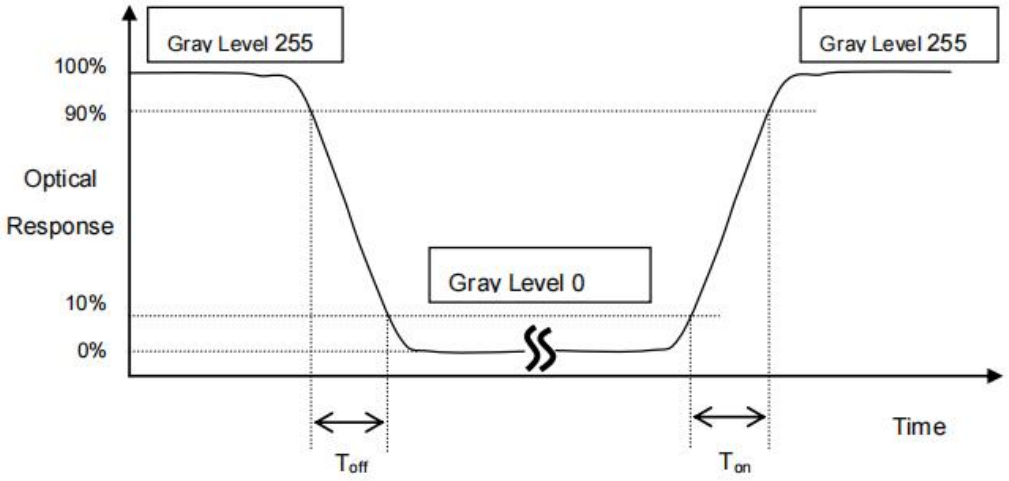
L255 : Luminance of gray level 255

L 0: Luminance of gray level 0

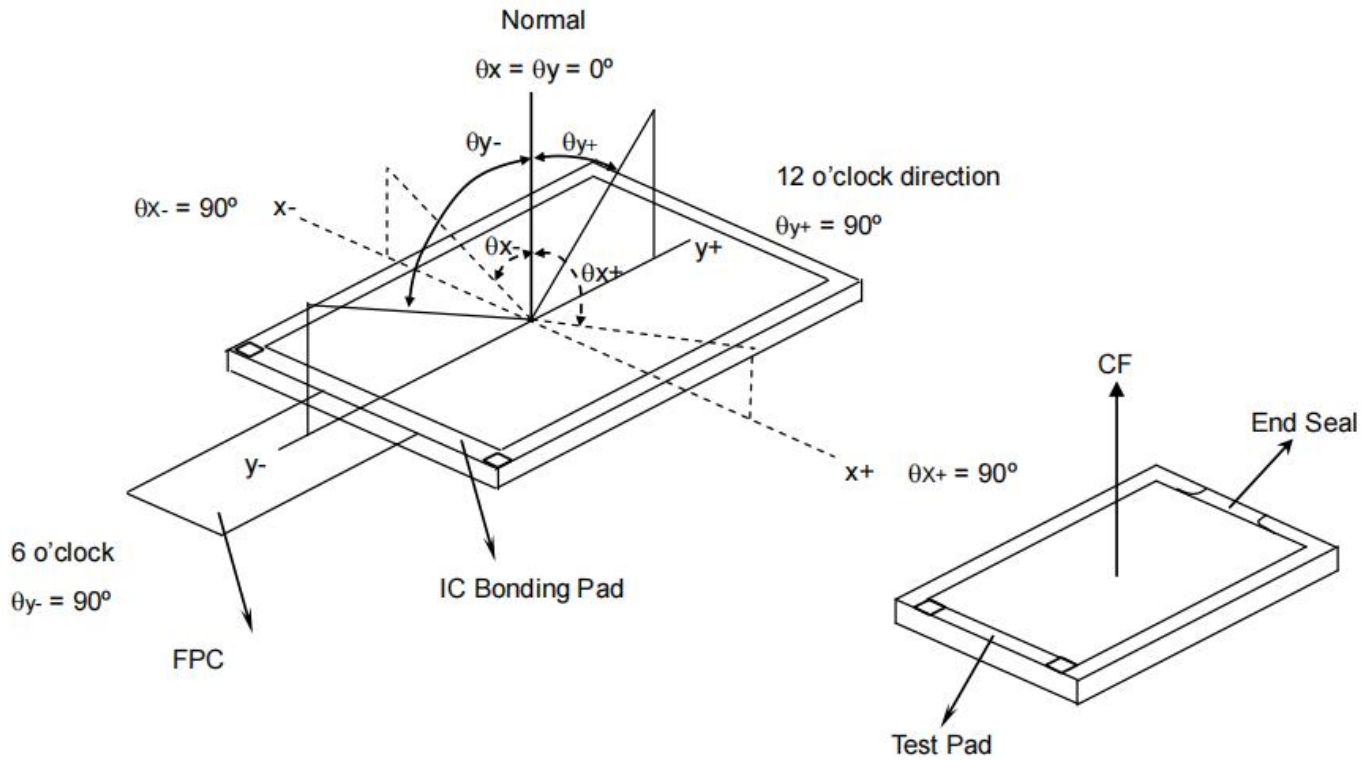
CR = CR (5)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (5).

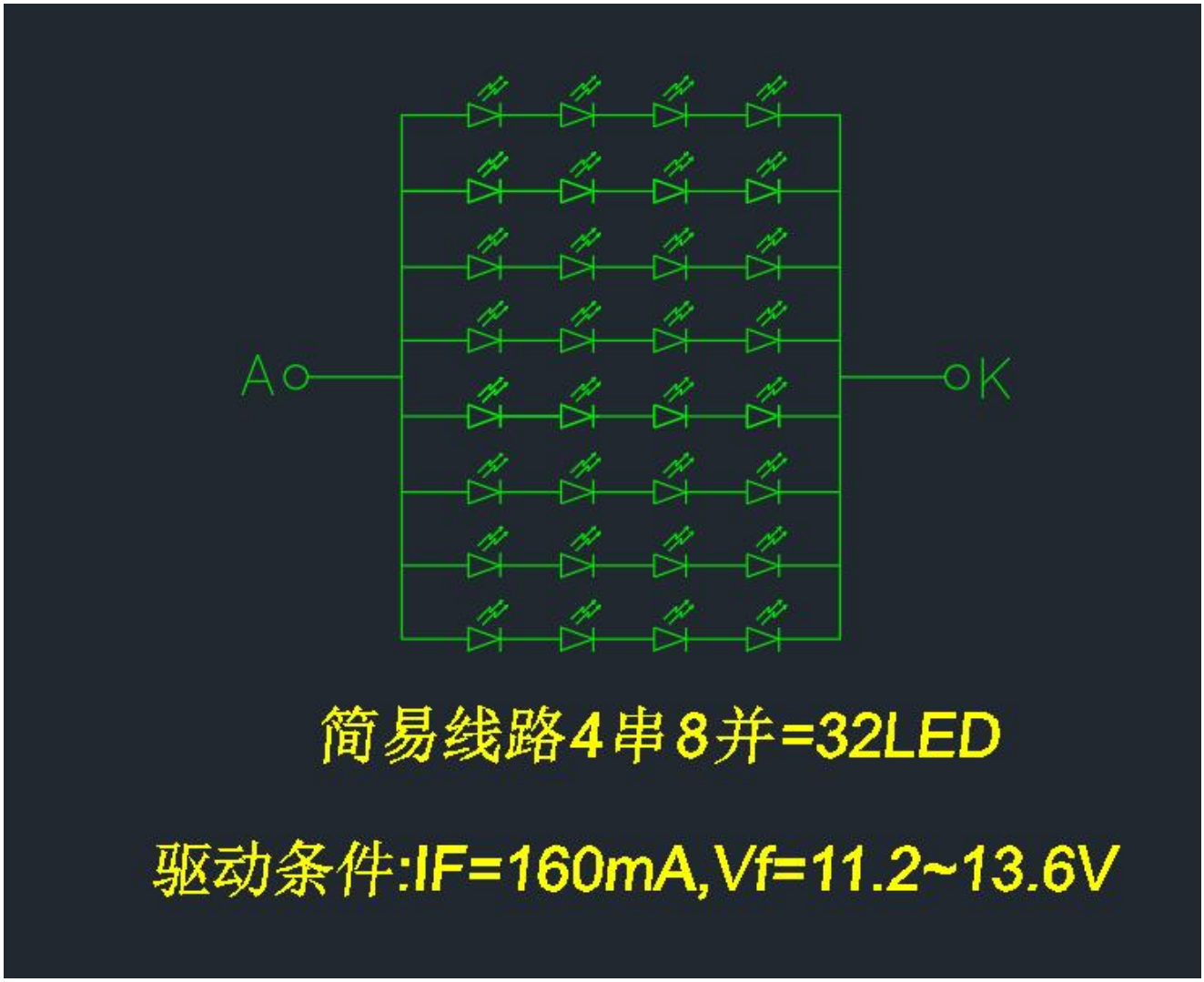
*Note (2) Definition of Response Time (T_{on}, T_{off}):



*Note(3) Definition of Viewing Angle



Backlight circuit



9.Records Of Version

Version	Revise Date	Page	Content
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