

PRODUCT SPECIFICATION **FOR LCD MODULE**

Revision: 1.0

Model No: LS0283I03-MPR-V1

Module Type: COG+FPC+B/L

APPROVED SIGNATURE

- ☒ Approved Product Specification only
- ☐ Approved Product Specification and Samples

<u>Prepared By</u>	<u>Checked By</u>	<u>Approved By</u>

Contents

目录

1. General Description	3
2. Physical Features	3
3. Mechanical Specification	3
4. Outline Dimension	4
5. Absolute Maximum Ratings	5
6. Electrical Characteristics	5
7. Module Function Description	6
8. Electro-Optical Characteristics	16
9. Inspection Standards	19
10. Records Of Version	26

1. General Description

LS0283I03-MPR-V1 is a transmissive type a-Si TFT-LCD (amorphous silicon thin film transistor liquid crystal display) module, which is composed of a TFT-LCD panel, a driver circuit and a backlight unit. The panel size is 2.83 inch and the resolution is 480(RGB)*640, the panel can display up to 16.7M colors.

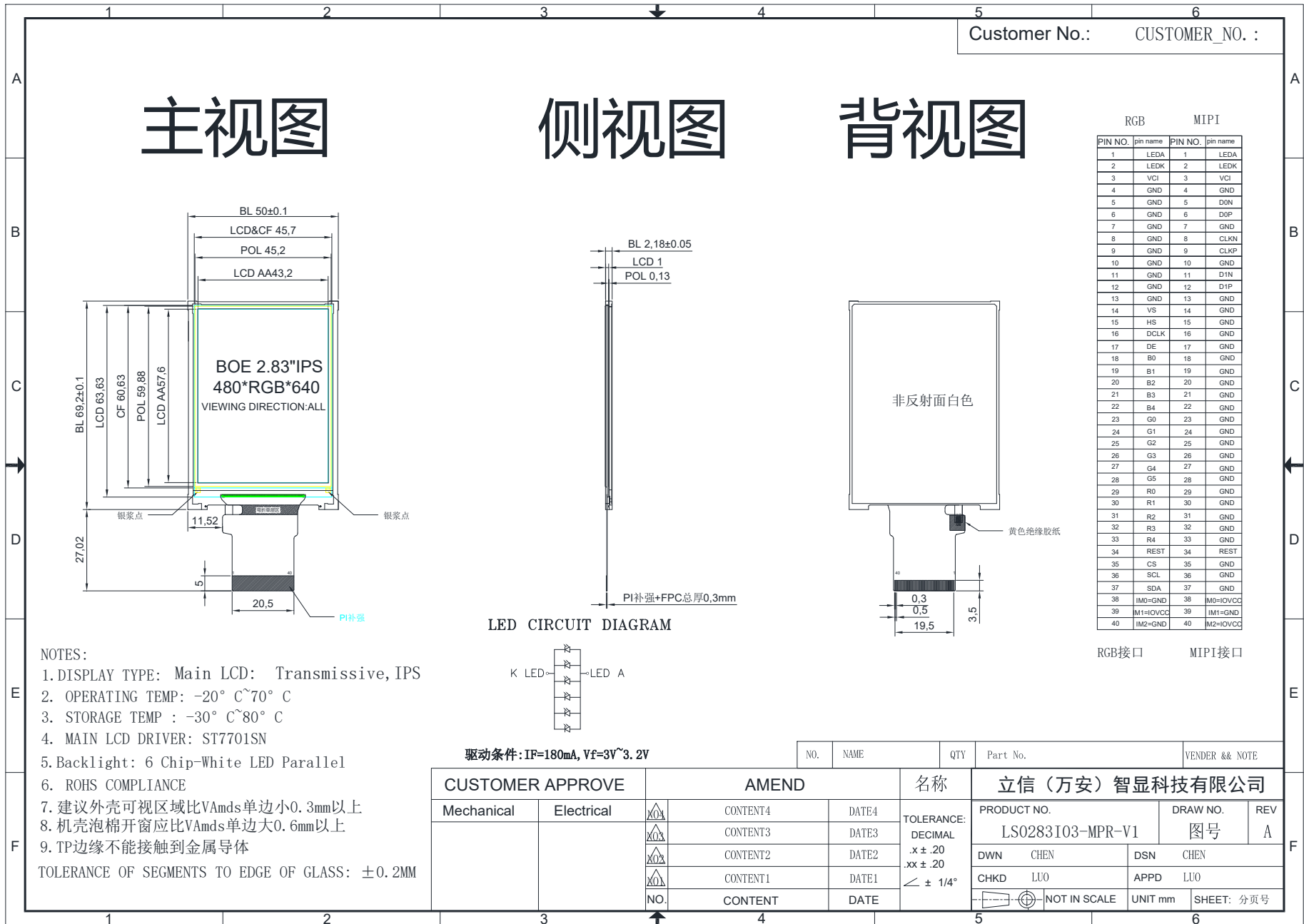
2. Physical Features

Display Mode	TFT-LCD Module
	Active matrix TFT, Transmissive type
Display Format	Graphic 480(RGB)×640 Dot-matrix
Input Data	18BIT RGB / MIPI
Viewing Direction (Grayscale Inversion)	Free (IPS)
Drive	ST7701SN

3. Mechanical Specification

Item	Specification	Unit
Module size (H×V×D)	50 ×69.2 ×2.18	mm
Number of dots	480(RGB) ×640	pixel
Active area (H×V)	43.2×57.6	mm

4.Outline Dimension



5. Absolute Maximum Ratings

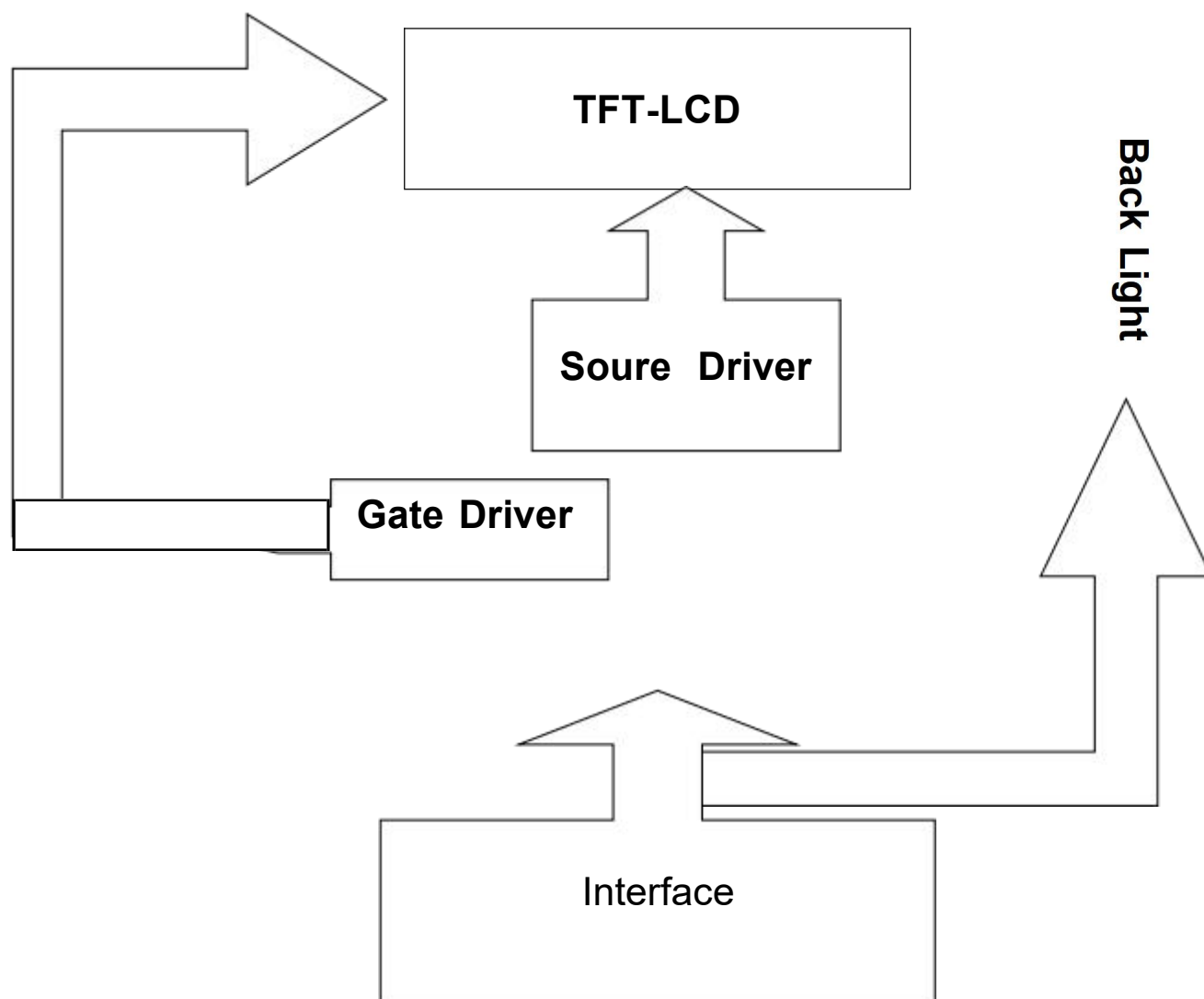
Item	Symbol	Min	Max	Unit	Remark
Supply voltage	VCC	-0.3	3.6	V	Note1 Note2
Supply voltage	IOVCC	-0.3	3.6	V	
Operating temperature	TOPR	-20	70	°C	
Storage temperature	TSTR	-30	80	°C	

6. Electrical Characteristics

Item		Symbol	Rating			Unit	Remark
			Min	Typ	Max		
Supply voltage		VCC	2.5	2.8	3.6	V	Note1
Supply voltage		IOVCC	1.65	2.8	3.3	V	
Input Voltage	L level	VIL	VSS	---	0.3*IOVCC	V	
	H level	VIH	0.7*IOVCC	---	IOVCC	V	

7. Module Function Description

7- 1. Block Diagram Of LCM



7-2. Pin Description

RGB

PinNo. Pin 序号	Symbol 符号	Function 功能描述
1	LED A	Backlight
2	LED K	Backlight
3	VCC(3.3V)	Power
4-13	GND	Ground
14	VSYNC	Vertical
15	HSYNC	Horizontal
16	DOTCLK	Data clock input
17	DE(ENABLE)	Data enable input.
18-22	B0-B4	Blue data
23-28	G0-G5	Green data
29-33	R0-R4	Red data
34	RESET	Reset signal pin
35	CS	Serial communication chip select
36	SCL	Serial command clock input
37	SDA	Serial command data input
38	GND	Ground
39	VCC	Power setting
40	GND	Ground

MIPI

PinNo. Pin 序号	Symbol 符号	Function 功能描述
1	LEDA	Backlight
2	LEDK	Backlight
3	VCC(3.3V)	Power
4	GND	Ground
5	DSI-D0N	DSI Data differential signal input pins. (Data lane 0)
6	DSID0P	D0DSI Data differential signal input pins. (Data lane0)
7	GND	Ground
8	DSI-CLK N	DSI CLOCK differential signal input pins
9	DSI-CLK P	DSI CLOCK differential signal input pins
10	GND	Ground
11	DSI-D1N	DSI Data differential signal input pins. (Data lane 1)
12	DSI-D1P	DSI Data differential signal input pins. (Data lane 1)
13-33	GND	Ground
34	RESET	Reset signal pin
35	CS	Serial communication chip select
36	SCL	Serial command clock input
37	SDA	Serial command data input
38	IOVCC	Power supply
39	GND	Ground
40	IOVCC	Power supply

7-3 Timing Characteristics

7.5.1 Serial Interface Characteristics (3-line serial):

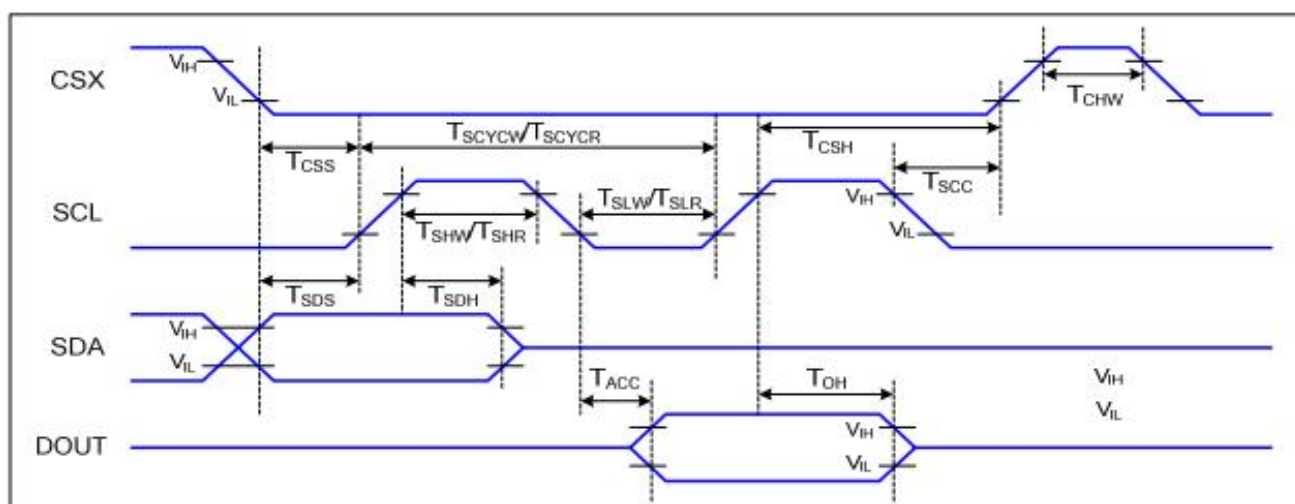


Figure 1 3-line serial Interface Timing Characteristics

VDDI=1.8, VDD=2.8, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	60		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	
	T_{SLW}	SCL "L" pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	

Table 4 3-line serial Interface Characteristics

Note : The rising time and falling time (T_r , T_f) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

7.5.3 RGB Interface Characteristics :

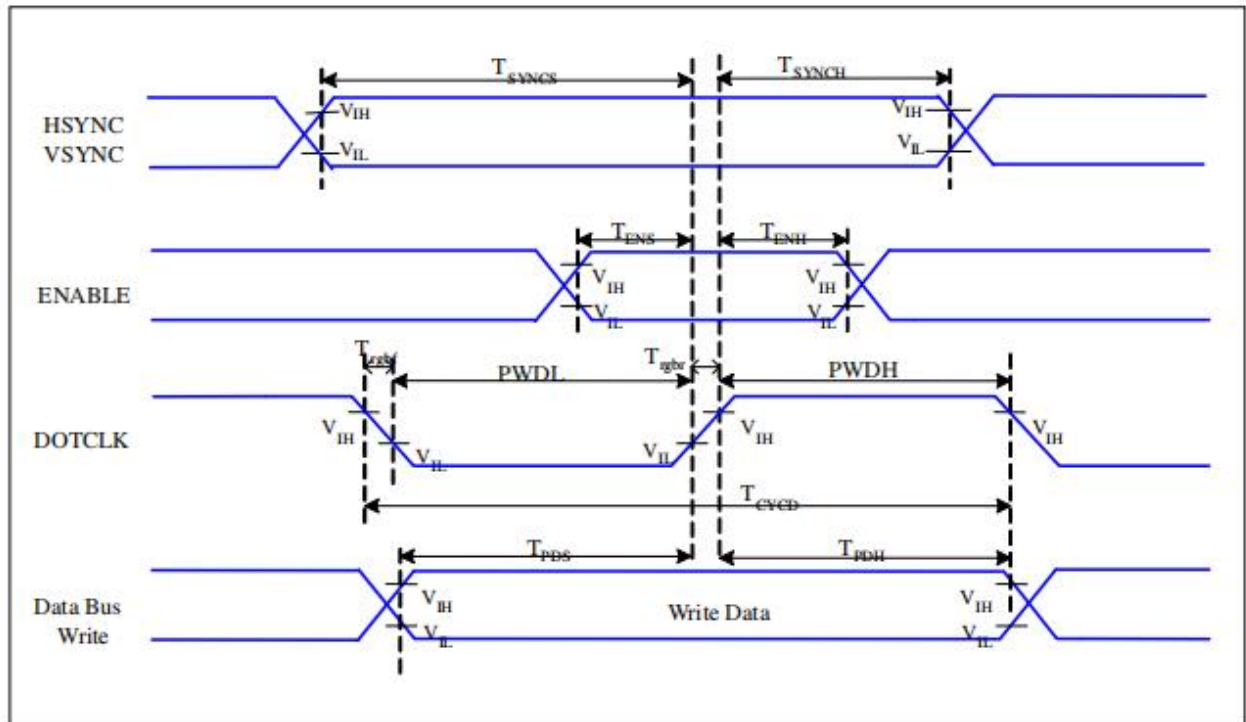


Figure 3 RGB Interface Timing Characteristics

VDDI=1.8, VDD=2.8, AGND=DGND=0V, $T_a=25^{\circ}\text{C}$

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	5	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	5	-	ns	
	T_{ENH}	Enable Hold Time	5	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	15	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	15	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	33	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	15	ns	
DB	T_{PDS}	PD Data Setup Time	5	-	ns	
	T_{PDH}	PD Data Hold Time	5	-	ns	

Table 6 18/16 Bits RGB Interface Timing Characteristics

7.5.5 Reset Timing:

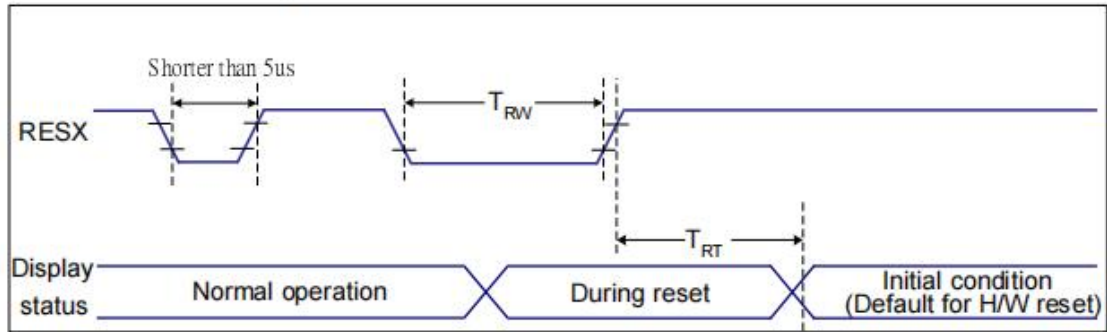


Figure 9 Reset Timing

VDDI=1.8, VDD=2.8, AGND=DGND=0V, $T_a=25^{\circ}\text{C}$

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120 (Note 1, 6, 7)	ms

Table 9 Reset Timing

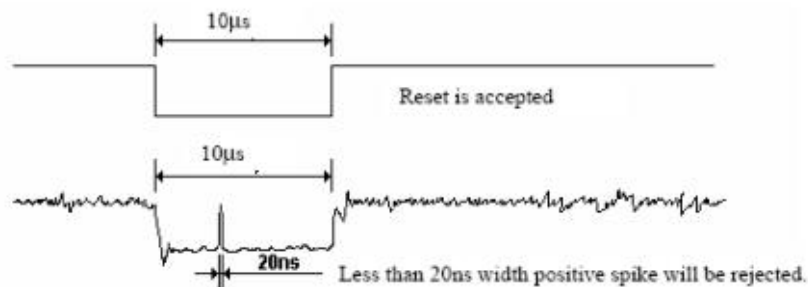
Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (t_{RT}) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out →mode. The display remains the blank state in Sleep In →mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

7.5.4 MIPI Interface Characteristics:

7.5.4.1 High Speed Mode



Figure 4 DSI clock channel timing

Figure 5 Rising and falling time on clock and data channel

$VDDI=1.8, VDD=2.8, AGND=DGND=0V, Ta=25\text{ }^{\circ}\text{C}$

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-CLK+/-	$2xUI_{INSTA}$	Double UI instantaneous	2.5	25	ns	
DSI-CLK+/-	UI_{INSTA} UI_{INSTB}	UI instantaneous halves	1.25	12.5	ns	$UI = UI_{INSTA} = UI_{INSTB}$
DSI-Dn+/-	t_{DS}	Data to clock setup time	0.15	-	UI	
DSI-Dn+/-	t_{DH}	Data to clock hold time	0.15	-	UI	

Table 7 Mipi Interface- High Speed Mode Timing Characteristics

7.5.4.2 Low Power Mode

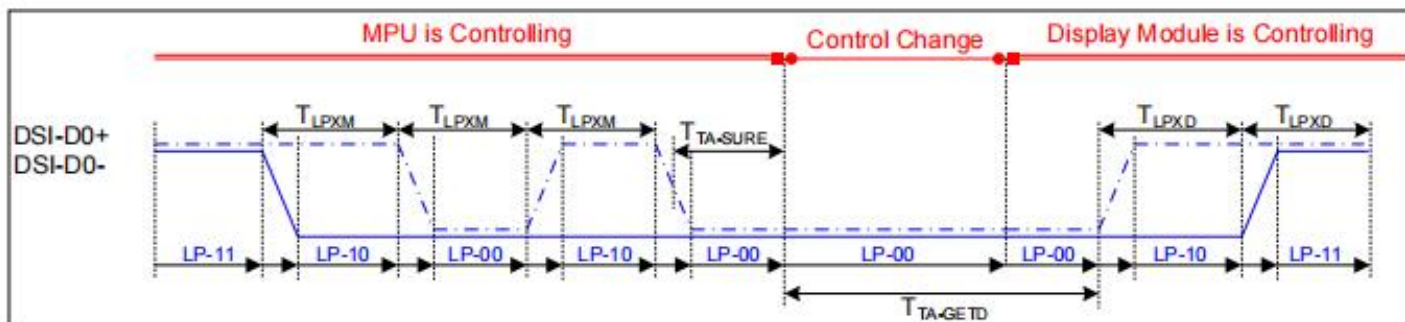


Figure 6 Bus Turnaround (BTA) from display module to MPU Timing

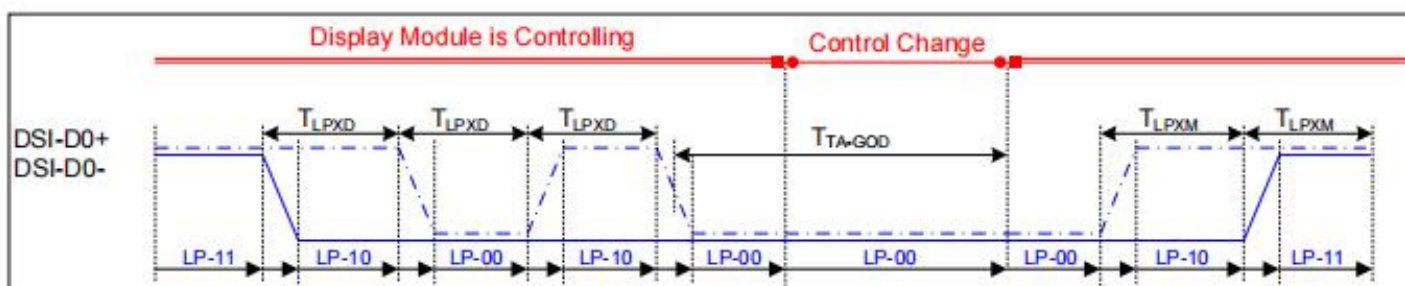


Figure 7 Bus Turnaround (BTA) from MPU to display module Timing

$VDDI=1.8, VDD=2.8, AGND=DGND=0V, Ta=25^{\circ}C$

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-D0+/-	TLPXM	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Input
DSI-D0+/-	TLPXD	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Output
DSI-D0+/-	TTA-SURED	Time-out before the MPU start driving	T_{LPXD}	$2 \times T_{LPXD}$	ns	Output
DSI-D0+/-	TTA-GETD	Time to drive LP-00 by display module	$5 \times T_{LPXD}$		ns	Input
DSI-D0+/-	TTA-GOD	Time to drive LP-00 after turnaround request-MPU	$4 \times T_{LPXD}$		ns	Output

Table 8 Mipi Interface Low Power Mode Timing Characteristics

7.5.4.3 DSI Bursts Mode

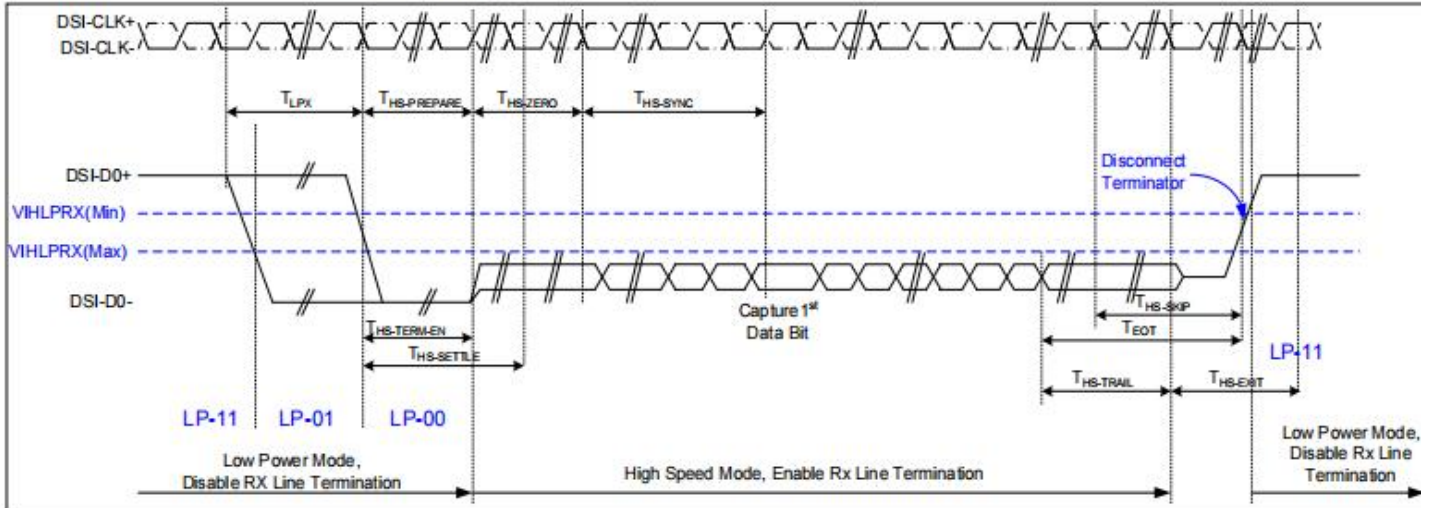


Figure 7 Data lanes-Low Power Mode to/from High Speed Mode Timing

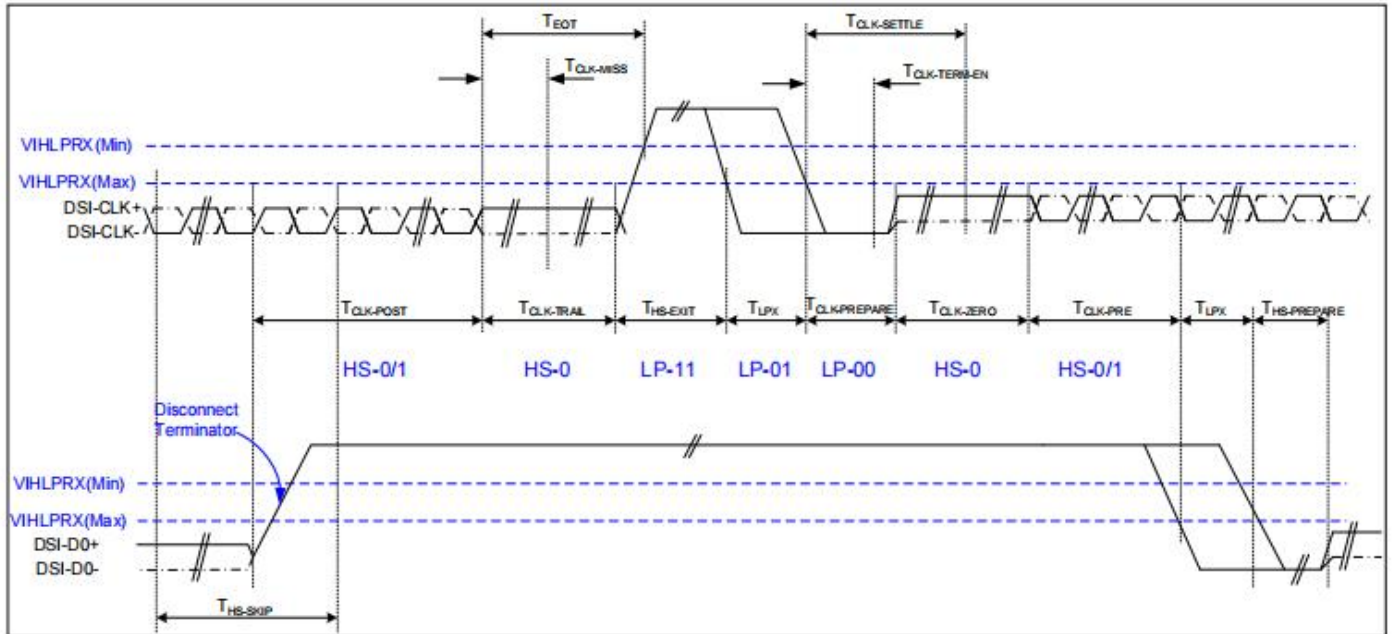


Figure 8 Clock lanes- High Speed Mode to/from Low Power Mode Timing

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
Low Power Mode to High Speed Mode Timing						
DSI-Dn+/-	TLPX	Length of any low power state period	50	-	ns	Input
DSI-Dn+/-	THS-PREPARE	Time to drive LP-00 to prepare for HS transmission	40+4 UI	85+6 UI	ns	Input
DSI-Dn+/-	THS-TERM-EN	Time to enable data receiver line termination measured from when Dn crosses VILMAX	-	35+4 UI	ns	Input
DSI-Dn+/-	THS-PREPARE + THS-ZERO	THS-PREPARE + time to drive HS-0 before the sync sequence	140+ 10UI	-	ns	Input
High Speed Mode to Low Power Mode Timing						
DSI-Dn+/-	THS-SKIP	Time-out at display module to ignore transition period of EoT	40	55+4 UI	ns	Input
DSI-Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-Dn+/-	THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4 UI	-	ns	Input
High Speed Mode to/from Low Power Mode Timing						
DSI-CLK+/-	TCLK-POS	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+5 2UI	-	ns	Input
DSI-CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns	Input
DSI-CLK+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS transmission	38	95	ns	Input
DSI-CLK+/-	TCLK-TERM-EN	Time-out at clock lan display module to enable HS transmission	--	38	ns	Input
DSI-CLK+/-	TCLK-PREPARE + TCLK-ZERO	Minimum lead HS-0 drive period before starting clock	300	-	ns	Input
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8UI	-	ns	Input
DSI-CLK+/-	TEOT	Time form start of TCLK-TRAIL period to start of LP-11 state	-	105n s+12 UI	ns	Input

8. Electro-Optical Characteristics

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time		Tr +Tf	$\theta_x = \theta_y = 0$	---	35	---	ms	Note 1
Contrast Ratio		CR		1000	1200	---	---	Note 2
Transmittance		T%		4.3	5.0	---	%	
Color Chromaticity (CIE1931)	White	W x	$\theta_x = \theta_y = 0$	---	TBD	---	---	
		W y		---	TBD	---	---	
Viewing angle	θ_T		CR > 10	80	85	---	Deg.	Note 3
	θ_B			80	85	---		
	θ_L			80	85	---		
	θ_R			80	85	---		

Notes : 1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see FIGURE 1).

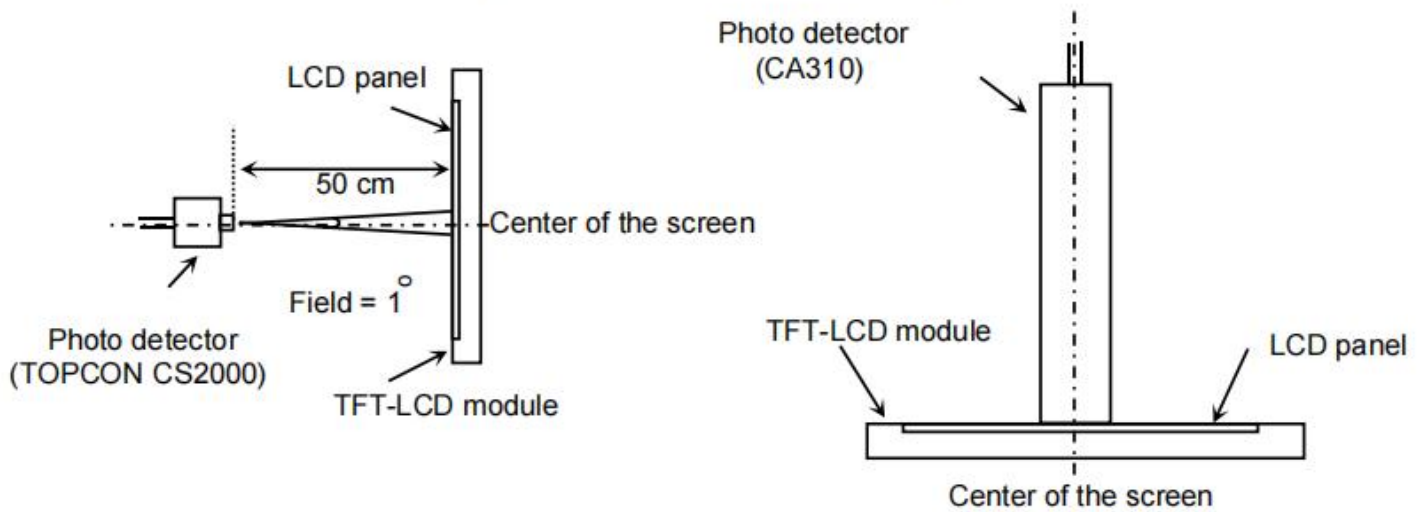
2. Contrast measurements shall be made at viewing angle of $\Theta = 0$ and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state . (see FIGURE 1) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. The color chromaticity coordinates specified in Table 5. shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.
4. The electro-optical response time measurements shall be made as FIGURE 2 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Tr, and 90% to 10% is Td.

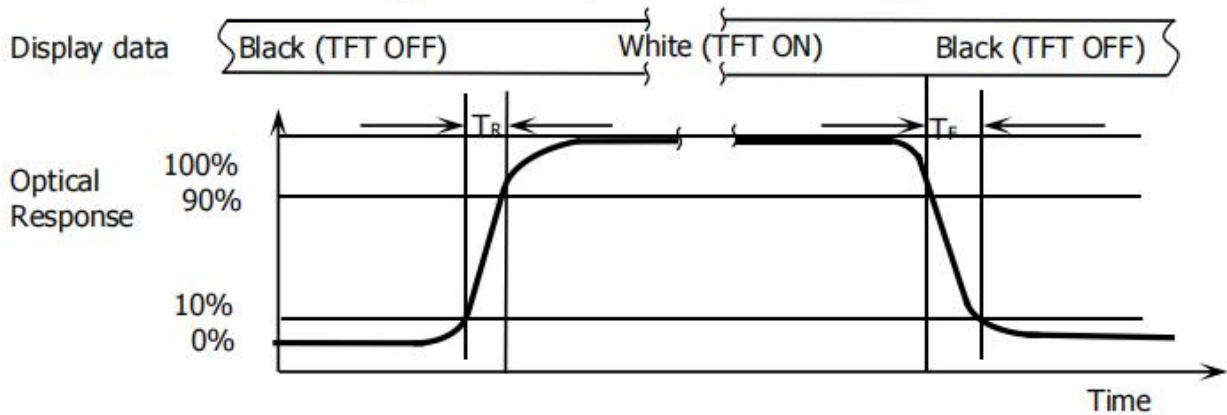
4.2 Optical measurements

Figure 1. Measurement Set Up



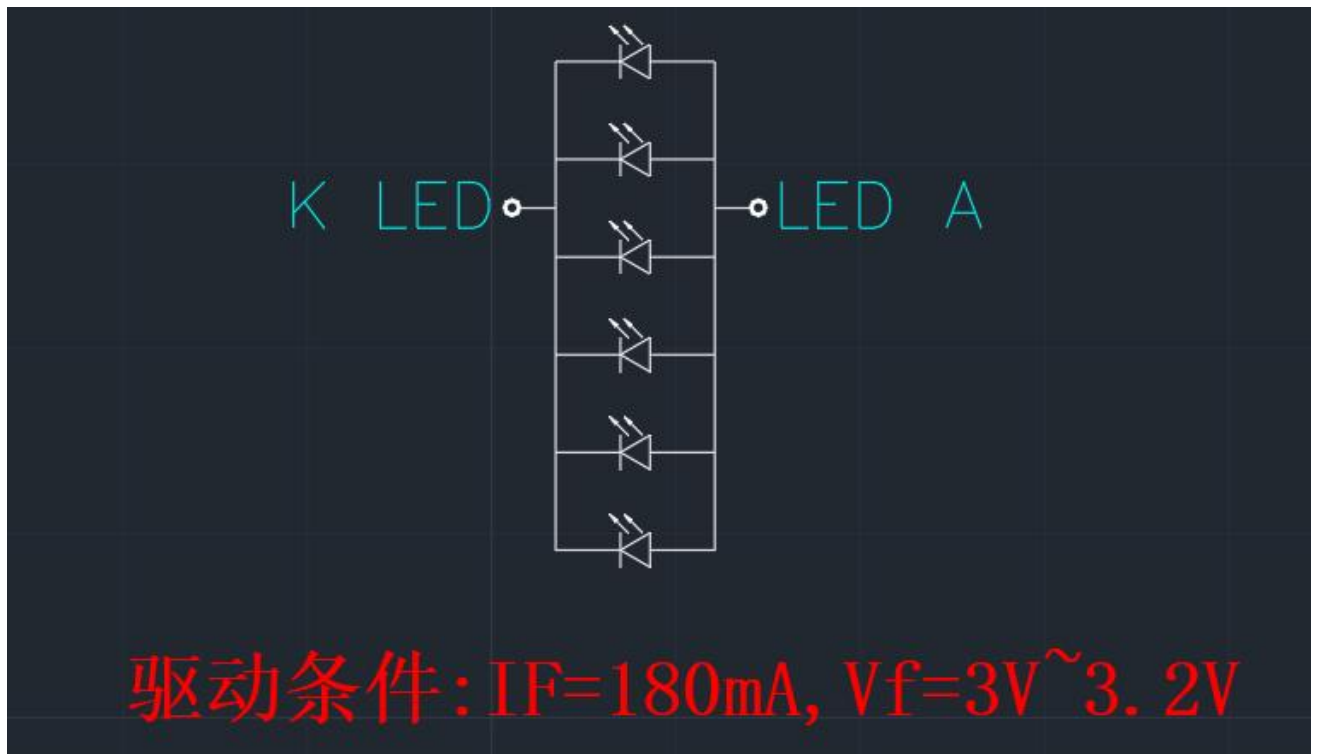
View angel range, uniformity, etc. measurement setup Flicker, measurement setup

Figure 2. Response Time Testing



The electro-optical response time measurements shall be made as shown in FIGURE 3 by switching the “data” input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is T_r and 90% to 10% is T_d .

Note(4) Backlight circuit



9. Inspection Standards

1. AQL(Acceptable Quality Level)

AQL of major and minor defect

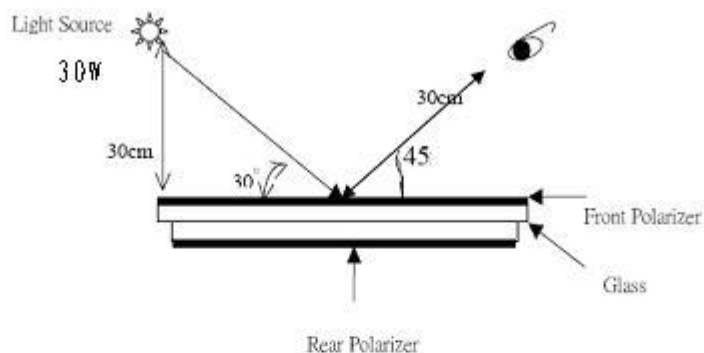
According to GB/T 2828-2003 ; , normal inspection, Class II

MAJOR DEFECT	MINOR DEFECT
0.65	1.5

2. Basic conditions for inspection

The LCM face to us, in normal environment, About an angle of incidence 30, a distance of 30cm with normal eye, with an angle of 45 degree to check the products without uncovering the film!

(As shown below)

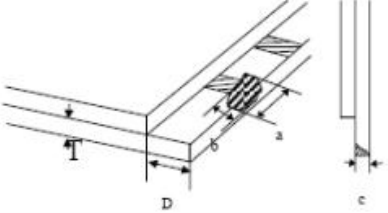
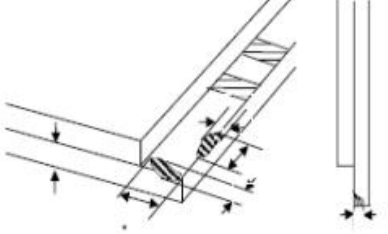


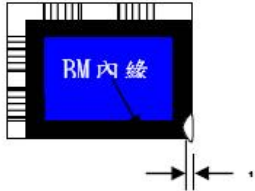
3. Inspection item and criteria

3.1 Visual inspection criterion in immobility

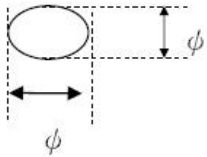
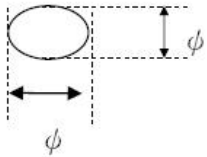
3.1.1 Glass defect

No	Defect item	Criteria	Remark
1	Dimension Unconformity (Major defect)	By Engineering Drawing	

No	Defect item	Criteria	Remark
2	Cracks (Major defect)	1.Linear cracks on panel 【Reject】 2. Nonlinear crack contrast by limited sample	
3	Glass extrude the conductive area (minor defect)	a: disregards and no influence assemblage 1) $b \leq 1/3$ Pin width(non bonding area) 【Accept】 2) bonding area $\leq 0.5\text{mm}$ 【Accept】	a:Length, b:Width
4	Pin-side , conductive area damaged (minor defect)	(a c : disregards) $b \leq 1/3$ of effective length for bonding electrode 【Accept】	a:Length, b:Width, c: Thickness  The diagram shows a 3D perspective of a rectangular panel with a pin attached to its side. Dimensions are labeled: 'a' for the length of the pin, 'b' for the width of the pin, 'c' for the thickness of the pin, and 'D' for the distance from the pin to the edge of the panel.
5	Pin-side , non-conductive area damaged (minor defect)	1) Damage area don't touch the ITO (Inclueling contraposition mark,except scribing mark) 【Accept】 2) $c < T$ $b \leq BM$ 1/3 of width 【Accept】 3) $c = T$ b not touch the seal glue 【Accept】 4) a disregards	a:Length, b:Width, c: Thickness  The diagram shows a 3D perspective of a rectangular panel with a pin attached to its side. Dimensions are labeled: 'a' for the length of the pin, 'b' for the width of the pin, 'c' for the thickness of the pin, and 'T' for the thickness of the panel.

No	Defect item	Criteria	Remark
6	Non-pin-side damage (minor defect)	$c < T$ 1) b exceeds 1/3 BM $c = T$ b not touch the seal glue 【Reject】 【Reject】	c : Thickness b: width of damage 

3.1.2 LCD appearance defect (View area)

No	Defect item	Criteria		Remark
1	Fiber 、glass cratch 、polarizer scratch/folded (minor defect)	Specification	Allowable	note1: L : Length , W : Width note2: disregard if out of AA 
		$0.05\text{mm} < W \leq 0.1\text{mm};$ $L \leq 3.0\text{mm}$	1	
		$W > 0.1\text{mm}; L > 3.0\text{mm}$	0	
2	Polarizer bubble 、 concave and convex (minor defect)	$\psi \leq 0.2\text{mm}$	disregard	note 1: $\psi = (L+W)/2$; L : Length , W : Width note2: disregard if out of AA 
		$0.2\text{mm} < \psi \leq 0.3\text{mm}$	2	
		$0.3\text{mm} < \psi \leq 0.5\text{mm}$	1	
		$0.5\text{mm} < \psi$	0	
3	Black dots 、dirty dots 、 impurities 、eyewinker (Major defect)	$\psi \leq 0.15\text{mm}$	disregard	note2: disregard if out of AA 
		$0.15\text{mm} < \psi \leq 0.25\text{mm}$	2	
		$0.25\text{mm} < \psi \leq 0.3\text{mm}$	1	
		$0.3\text{mm} < \psi$	0	
4	Polarizer prick (Major defect)	$\psi \leq 0.1\text{mm}$	disregard	note1: $\psi = (L+W)/2$; L= Length , W=Width note2: the distance between two dots > 5mm
		$0.1\text{mm} < \psi \leq 0.25\text{mm}$	3	
		$\psi > 0.25\text{mm}$	0	

3.1.3 .FPC

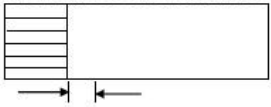
No	Defect item	Criteria		Remark
1	Copper screen peel (Major defect)	Copper screen peel 【 Reject】		
2	No release tape or peel (Major defect)	No release tape or peel 【 Reject】		
3	Dirty dot and impurity of FPC for customer using side (minor defect)	Specification	Allowable	note1: Cannot have stride ITO impurities
		$\psi \leq 0.25\text{mm}$	2	
		$\psi > 0.25$	0	

3.1.4 Black tape & Mara tape

1	FPC or H/S black tape shift (minor defect)	1.shift spec: 1)glue to the polarize 【 Reject】 2) IC bare 【 Reject】 2. left-and-right spec: 1) exceed of FPC edge or H-S edge 【 Reject】 2)IC bare 【 Reject】	
2	No black tape (Major defect)	No black tape 【 Reject】	
3	Tape position mistake (minor defect)	Not by engineering drawing 【 Reject】	
4	Mara tape defect (minor defect)	Peel before pulling the protecting film. 【 Reject】	

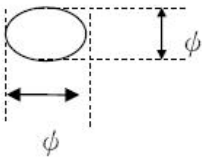
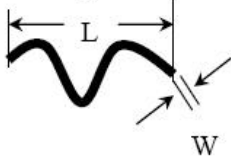
3.1.5 Silicon and Tuffy glue

No	Defect item	Criteria	Remark
1	Quantity of silicon (minor defect)	Uncover the ITO and circuit area. 【 Reject】	note: compared by engineering drawing.

No	Defect item	Criteria	Remark
2	Tuffy glue (minor defect)	1. Uncover the reveal copper area 【 Reject】 2. Cover layer 0.3mm(Min) ~ 3.0mm(Max) 【 accept】	note:if customer has special requirement , refer to the technical document. 
3	Depth of glue covering (minor defect)	Depth of glue covering overtop front Polarizer 【 Reject】	Except of the special requirement °

3.2 Electrical criteria

No	Defect item	Criteria	Remark
1	No display (Major defect)	No display 【 Reject】	
2	Missing line (Major defect)	Missing line 【 Reject】	
3	Seg-com light and dark (Major defect)	Seg-com light and dark 【 Reject】	ND filter 2% test
4	No display in immobility (Major defect)	No display in immobility 【 Reject】	
5	Flicker of Pattern (Major defect)	Flicker of Pattern 【 Reject】	
6	Mura (Major defect)	ND filter 2% test	
7	Over current (Major defect)	Over current 【 Reject】	
8	Voltage out of specification (Major defect)	Voltage out of specification 【 Reject】	
9	Pattern blur ,error code (Major defect)	Pattern blur ,error code 【 Reject】	
10	Dark light, Flicker (Major defect)	Dark light, Flicker 【 Reject】	

No	Defect item	Criteria	Remark	
11	Black/White dots 、 Dirty dots 、 eyewinker (Major defect)	Specification	Allowable	Note1: disregard if out of AA 
		$\psi \leq 0.15\text{mm}$	disregard	
		$0.15\text{mm} < \psi \leq 0.25\text{mm}$	2	
		$0.25\text{mm} < \psi \leq 0.3\text{mm}$	1	
		$0.3\text{mm} < \psi$	0	
12	Fiber 、 glass cratch 、 polarizer scratch/folded (minor defect)	$W \leq 0.03\text{mm}$	disregard	note1: L : Length 、 W : Width note2: disregard if out of AA 
		$0.03\text{mm} < W \leq 0.05\text{mm} ;$ $L \leq 3.0\text{mm}$	2	
		$0.05\text{mm} < W \leq 0.1\text{mm} ;$ $L \leq 3.0\text{mm}$	1	
		$W > 0.1\text{mm} ; L > 3.0\text{mm}$	0	

10.Records Of Version

Version	Revise Date	Page	Content
00	2025-4-27	all	New released