PRODUCT SPECIFICATION FOR LCD MODULE

Revision: 1.0

Model No: LS035I01-R-V1

Module Type: COG+FPC+B/L

APPROVED SIGNATURE

■ Approved Product Specification only

□ Approved Product Specification and Samples

Prepared By	Checked By	Approved By

Contents

目录

1. General Description

LS035I01-R-V1 is a transmissive type a-Si TFT-LCD (amorphous silicon thin film transistor liquid crystal display) module, which is composed of a TFT-LCD panel, a driver circuit and a backlight unit. The panel size is 3.5 inch and the resolution is 320(RGB)*480, the panel can display up to 16.7M colors.

2. Physical Features

Display Mode	TFT-LCD Module
	Active matrix TFT, Transmissive type
Display Format	Graphic 320(RGB)×480 Dot-matrix
Input Data	18 bit RGB
Viewing Direction （Grayscale Inversion）	Free（IPS）
Drive	ILI9488

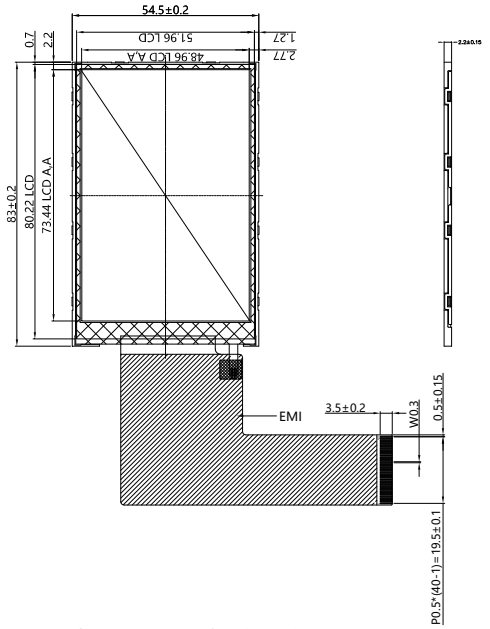
3. Mechanical Specification

Item	Specification	Unit
Module size (H×V×D)	51.96 ×80.22 ×0.8	mm
Number of dots	320(RGB) ×480	pixel
Active area (H×V)	48.96×73.44	mm

4. Outline Dimension

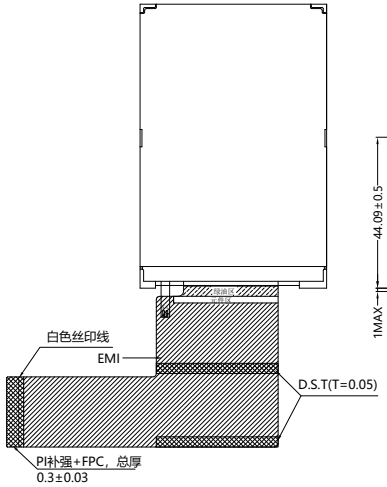
Customer No.: CUSTOMER_NO.:

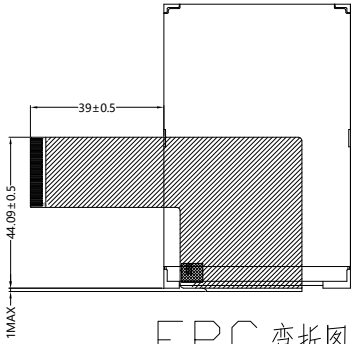
正面图



侧面图

背面图





FPC弯折图

FPC弯折出货

接口定义：

01	LEDK	40	SDI
02	LEDA	39	SCK
03	GND	38	CS
04	VCC	37	RESET
05	NC	36	GND
06	NC	35	NC
07	R2	34	DEN
08	R3	33	VSYNC
09	R4	32	HSYNC
10	R5	31	NC
11	R6	30	PCLK
12	R7	29	GND
13	NC	28	B7
14	NC	27	B6
15	G2	26	B5
16	G3	25	B4
17	G4	24	B3
18	G5	23	B2
19	G6	22	NC
20	G7	21	NC

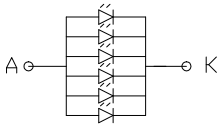
MDS/VA: MDS VIEWING AREA

NOTES:

1.DISPLAY TYPE: Main LCD: Transmissive,IPS
2. OPERATING TEMP: -10°C~60°C
3. STORAGE TEMP : -20°C~70°C
4. MAIN LCD DRIVER: ILI9488
5.Backlight: 6 Chip-White LED Parallel
6. ROHS COMPLIANCE
7.建议外壳可视区域比VAmds单边小0.3mm以上
8.机壳泡棉开窗应比VAmds单边大0.6mm以上
9.TP边缘不能接触到金属导体

TOLERANCE OF SEGMENTS TO EDGE OF GLASS: ±0.2MM

LED CIRCUIT DIAGRAM



驱动条件:IF=120mA,Vf=2.8~3.2V(TYP)

NO.	NAME	QTY	Part No.	VENDER && NOTE

CUSTOMER APPROVE		AMEND			名称	立信（万安）智显科技有限公司		
Mechanical	Electrical	X04	CONTENT4	DATE4	TOLERANCE: DECIMAL .x ± .20 .xx ± .20 ∠ ± 1/4°	PRODUCT NO. 规格 LS035I01-R-V1	DRAW NO. 图号	REV 版本
		X03	CONTENT3	DATE3		DWN 出图人	DSN 设计人	
		X02	CONTENT2	DATE2		CHKD 校对人	APPD 批准人	
		X01	CONTENT1	DATE1		NOT IN SCALE	UNIT mm	SHEET: 分页号
		NO.	CONTENT	DATE				

5. Absolute Maximum Ratings

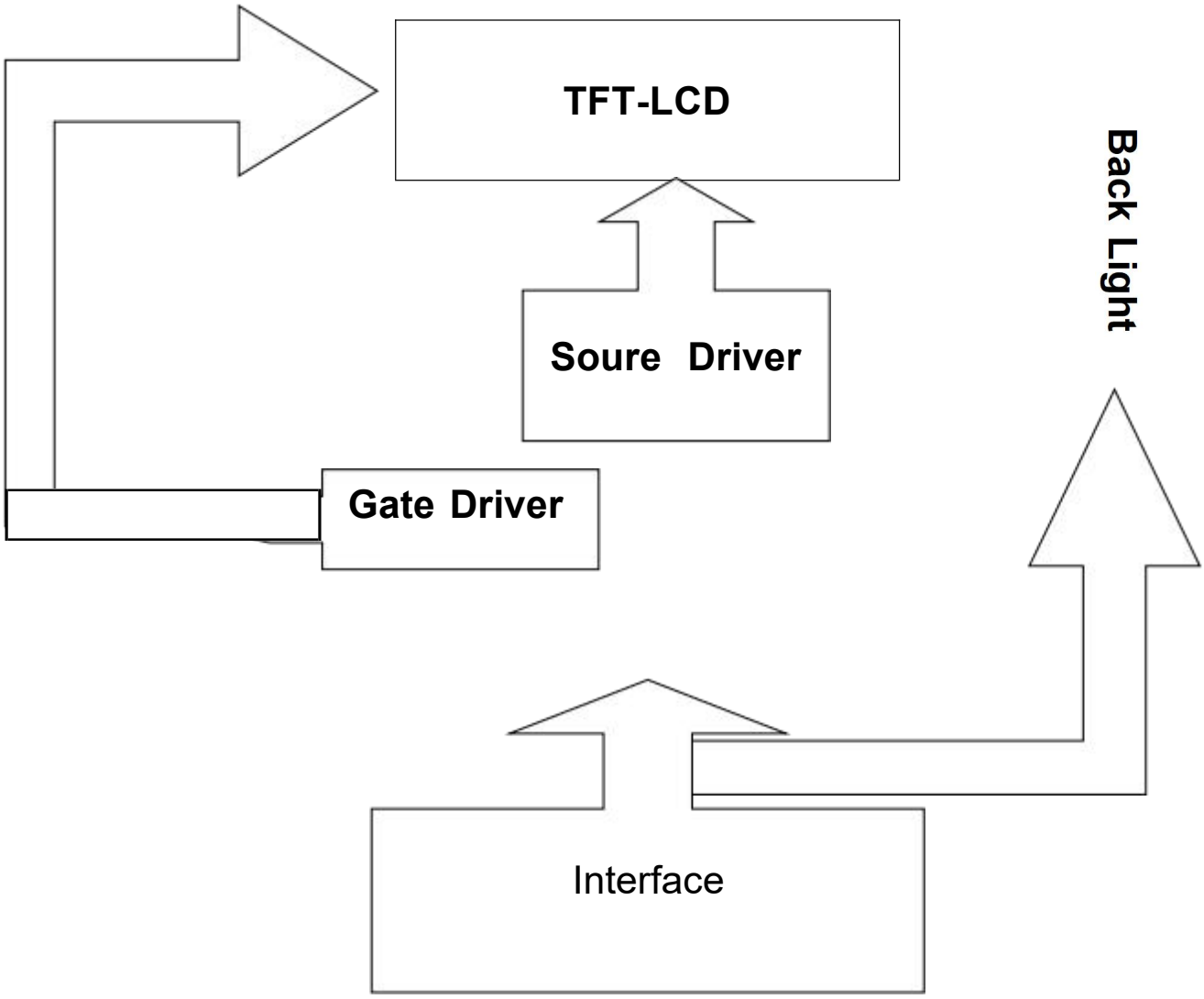
Item	Symbol	Min	Max	Unit	Remark
Supply voltage	VCC	-0.3	3.3	V	Note1 Note2
Supply voltage	IOVCC	-0.3	3.3	V	
Operating temperature	TOPR	-10	60	℃	
Storage temperature	TSTR	-20	70	℃	

6. Electrical Characteristics

Item		Symbol	Rating			Unit	Remark
			Min	Typ	Max		
Supply voltage		VCC	2.5	2.8	3.3	V	Note1
Supply voltage		IOVCC	1.65	1.8	3.3	V	
Input Voltage	L level	VIL	-0.3	---	0.3*IOVCC	V	
	H level	VIH	0.7*IOVCC	---	IOVCC	V	

7. Module Function Description

7-1. Block Diagram Of LCM



7-2. Pin Description

PIN NO.	Symbol	I/O	Description
1	LEDK	P	Power for LED backlight cathode
2	LEDA	P	Power for LED backlight anode
3	GND	P	Power ground
4	VCC	P	Power voltage
5-6	NC		
7-12	R2-R7	I	Red data
13-14	NC		
15-20	G2-G7	I	Green data
21-22	NC		
23-28	B2-B7	I	Blue data
29	GND	P	Power ground
30	PCLK	I	Pixel clock
31	NC		
32	HSYNC	I	Horizontal sync signal
33	VSYNC	I	Vertical sync signal
34	DEN	I	Data enable
35	NC		
36	GND	P	Power ground
37	RESET	I	Reset signal pin
38	CS	I	chip select signa
39	SCK	I	Serial clock input
40	SDI	I/O	Serial data input

7-3 Timing Characteristics

7.3.1 RGB Interface Characteristics

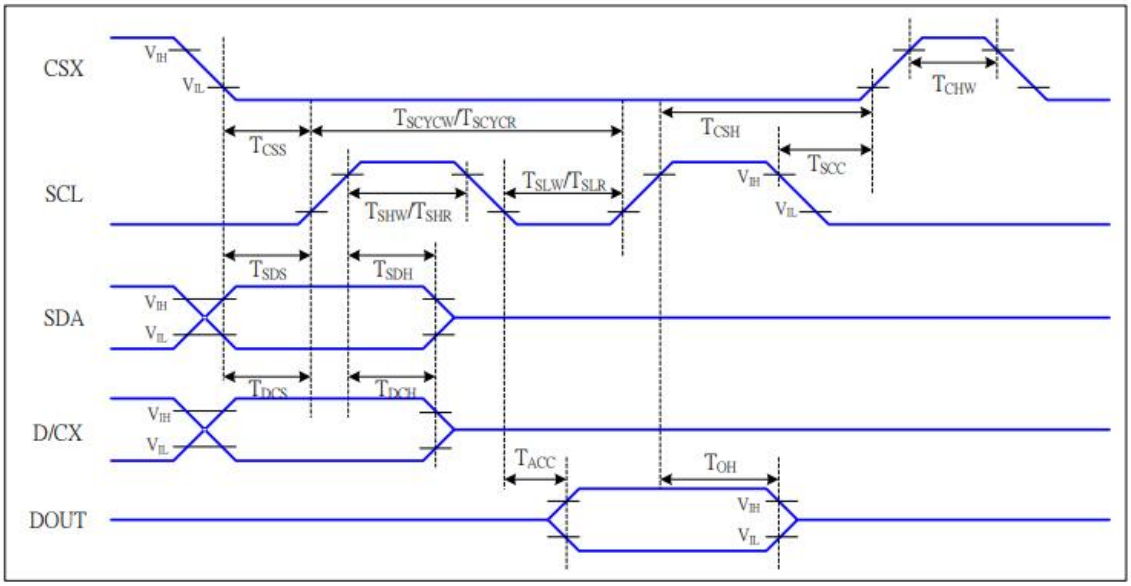


Figure 5 4-line serial Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	TBD	-	ns	
	T_{CSH}	Chip select hold time (write)	TBD	-	ns	
	T_{CSS}	Chip select setup time (read)	TBD	-	ns	
	T_{SCC}	Chip select hold time (read)	TBD	-	ns	
	T_{CHW}	Chip select “H” pulse width	TBD	-	ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	TBD	-	ns	-write command & data ram
	T_{SHW}	SCL “H” pulse width (Write)	TBD	-	ns	
	T_{SLW}	SCL “L” pulse width (Write)	TBD	-	ns	
	T_{SCYCR}	Serial clock cycle (Read)	TBD	-	ns	-read command & data ram
	T_{SHR}	SCL “H” pulse width (Read)	TBD	-	ns	
	T_{SLR}	SCL “L” pulse width (Read)	TBD	-	ns	
D/CX	T_{DCS}	D/CX setup time	TBD	-	ns	
	T_{DCH}	D/CX hold time	TBD	-	ns	
SDA (DIN)	T_{SDS}	Data setup time	TBD	-	ns	
	T_{SDH}	Data hold time	TBD	-	ns	
DOUT	T_{ACC}	Access time	TBD	TBD	ns	For maximum CL=30pF
	T_{OH}	Output disable time	TBD	TBD	ns	For minimum CL=8pF

7.3.2 RGB Interface Timing

The timing chart of 16-/18-/24-bit DPI interface mode is illustrated in Figure 19.

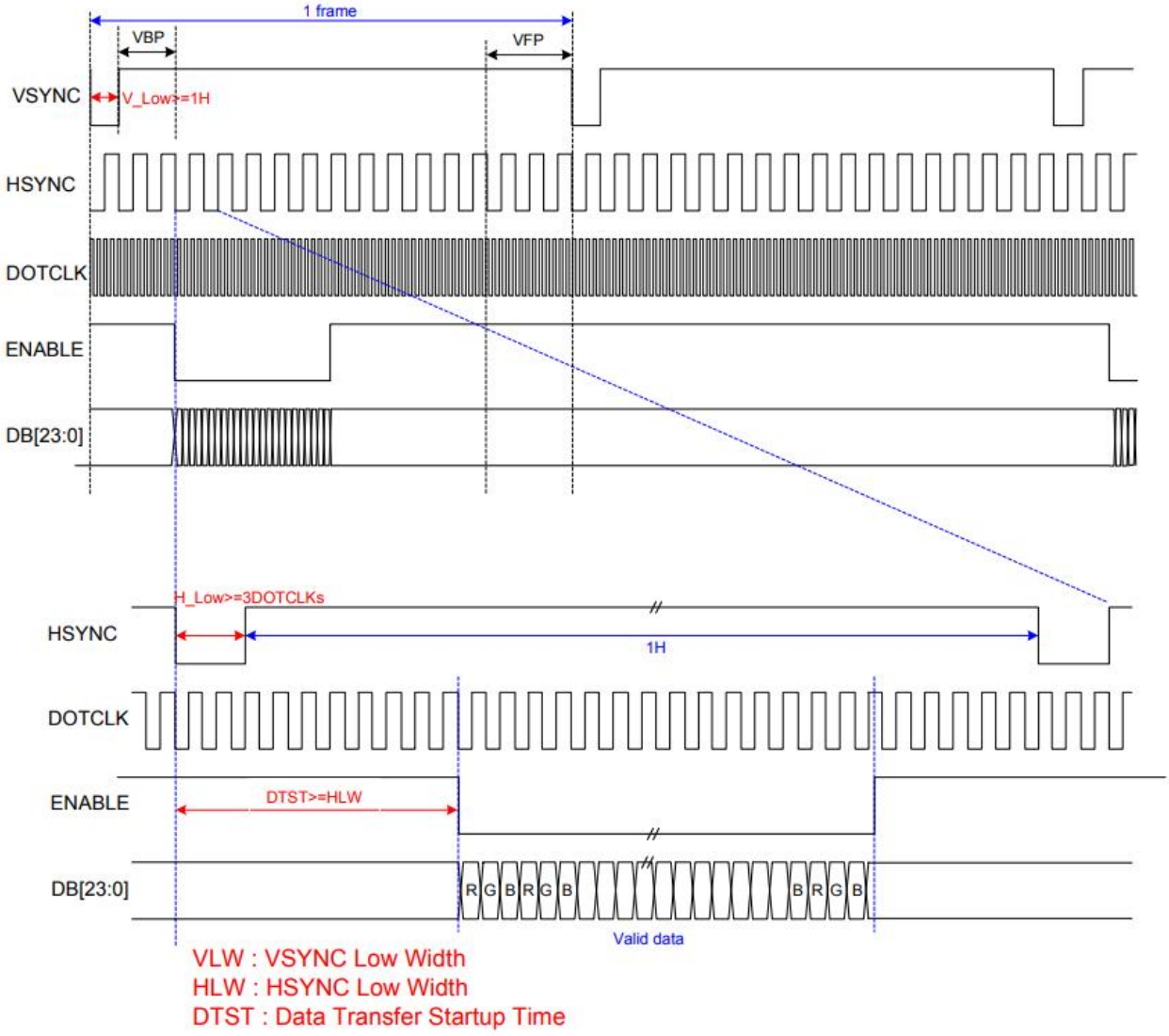
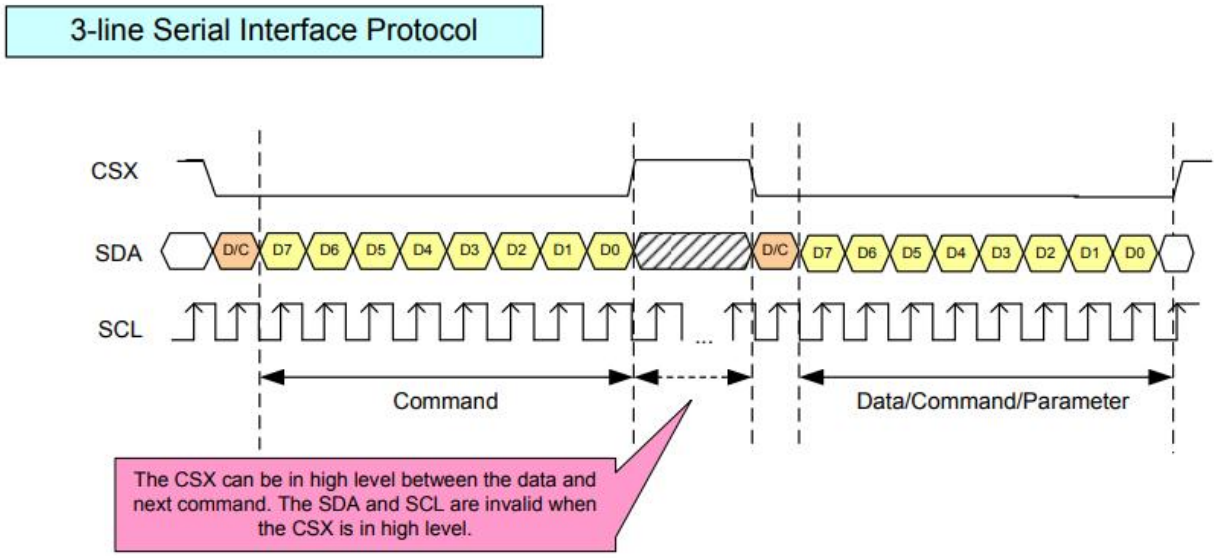


Figure 19: DPI Interface Timing Diagram

Note: VSPL = 0, HSPL = 0, DPL = 0 and EPL = 0 of Interface Mode Control B0h command.

7.3.3 SPI Interface Timing

The host drives the CSX pin to low and sets the D/CX bit on the SDA pin. The bit is read by the ILI9488 on the first rising edge of the SCL signal. On the next falling edge of the SCL, the MSB data bit (D7) is set on the SDA pin by the host. On the next falling edge of the SCL, the next bit (D6) is set on the SDA pin. If the optional D/CX signal is used, a byte is eight read cycles long. The 3-/4-line serial interface writing sequences are described in Figure 7 and Figure 8 below.

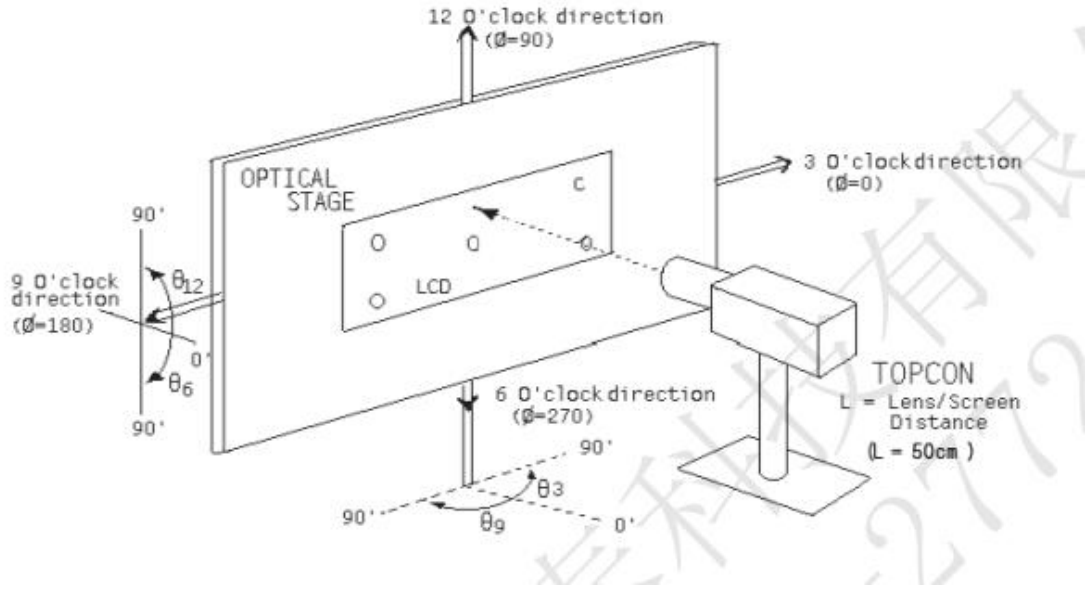


8. Electro-Optical Characteristics

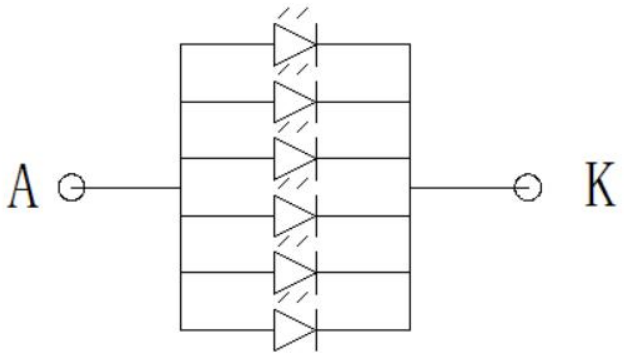
Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time		Tr +Tf	θx = θy =0	---	25	35	ms	Note 1
Contrast Ratio		CR		---	1000	---	---	Note 2
Transmittance		T%		3.45	4.05	---	%	
Color Chromaticity (CIE1931)	White	W x	θx = θy =0	---	0.304	---	---	
		W y		---	0.332	---	---	
Viewing angle	θ_T		CR > 10	---	85	---	Deg.	Note 3
	θ_B			---	85	---		
	θ_L			---	85	---		
	θ_R			---	85	---		
Luminance (I_F = 120mA)		L			TBD	---	cd/m2	Note4

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

Note (3) Definition of Viewing Angle:



Note(4) Backlight circuit



驱动条件：IF=120mA, Vf=2.8~3.2V(TYP)

9.Records Of Version

Version	Revise Date	Page	Content
00	2024-2-2	ALL	New released