PRODUCT SPECIFICATION FOR LCD MODULE

Revision: 1.0`

Model No: LS028T10-M-V1

Module Type: COG+FPC+B/L

APPROVED SIGNATURE

■ Approved Product Specification only

□ Approved Product Specification and Samples

Prepared By	Checked By	Approved By

Contents

目录

1. General Description

LS028T10-M-V1 is a transmissive type a-Si TFT-LCD (amorphous silicon thin film transistor liquid crystal display) module, which is composed of a TFT-LCD panel, a driver circuit and a backlight unit. The panel size is 2.8 inch and the resolution is 240(RGB)*320, the panel can display up to 262k colors.

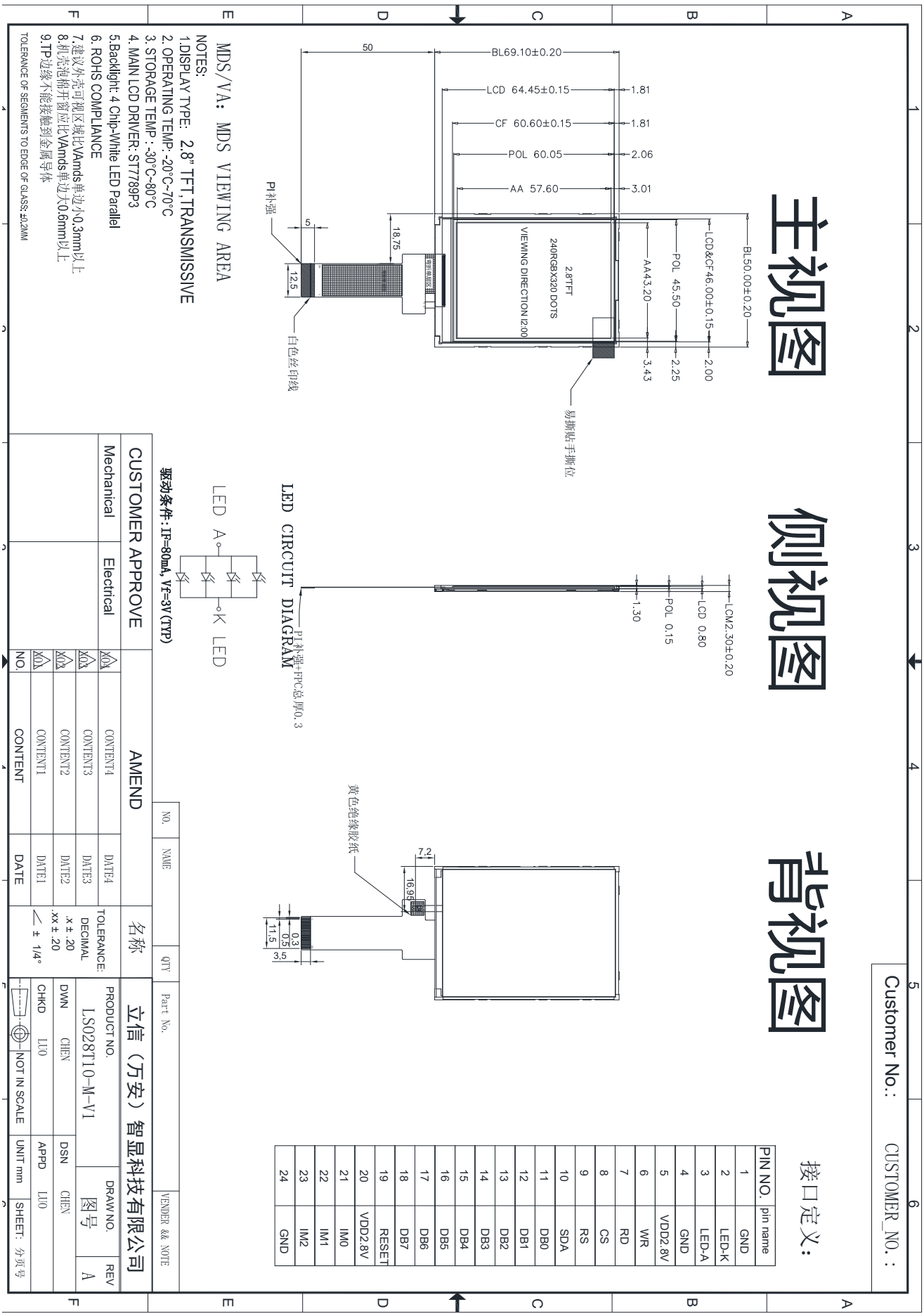
2. Physical Features

Display Mode	TFT-LCD Module
	Active matrix TFT, Transmissive type
Display Format	Graphic 240(RGB)×320 Dot-matrix
Input Data	8bit 8080 /SPI
Viewing Direction （Grayscale Inversion）	TN
Drive	ST7789P3

3. Mechanical Specification

Item	Specification	Unit
Module size (H×V×D)	50.0 ×69.1 ×2.3	mm
Number of dots	240(RGB) ×320	pixel
Active area (H×V)	43.2×57.6	mm

4. Outline Dimension



5. Absolute Maximum Ratings

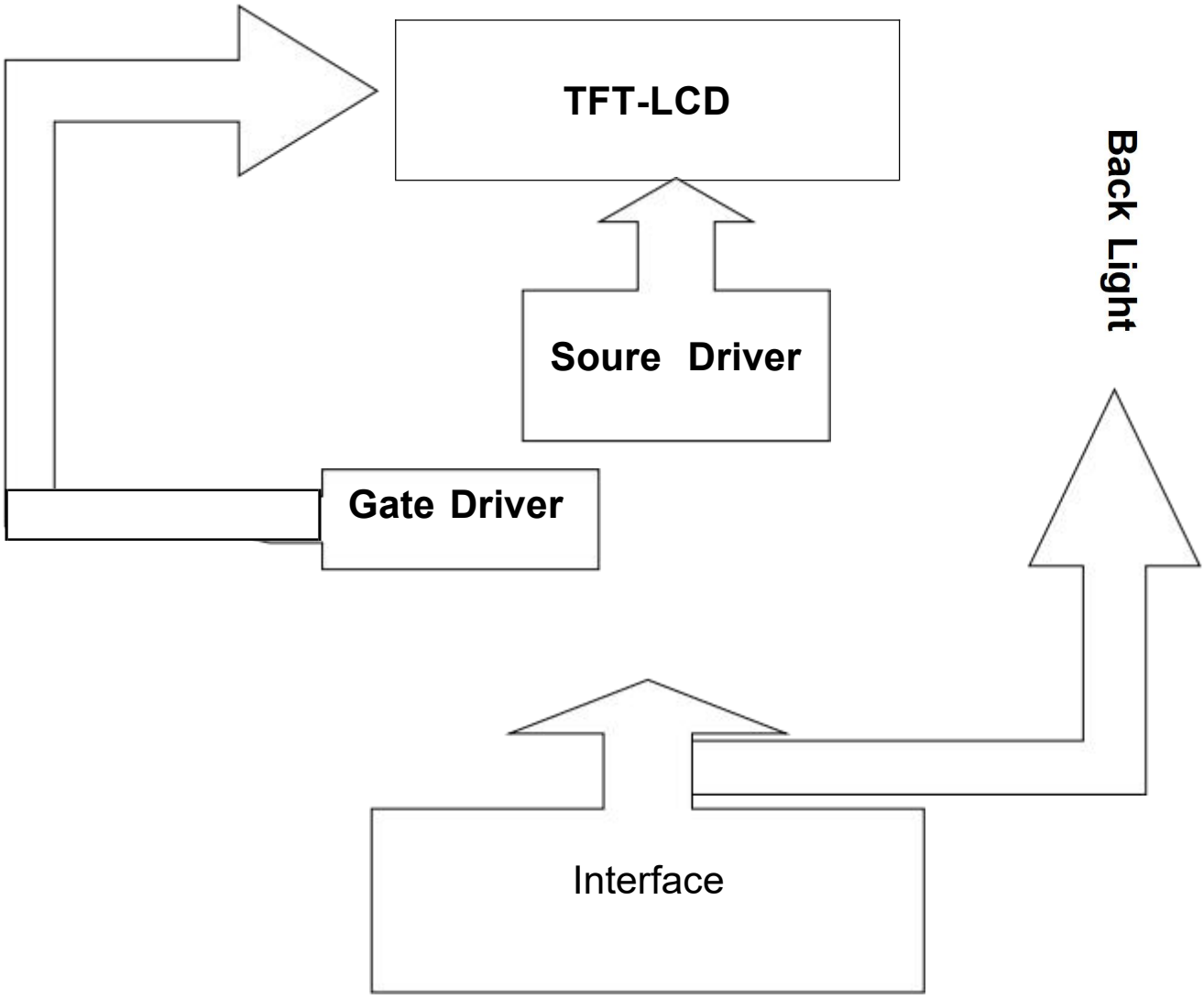
Item	Symbol	Min	Max	Unit	Remark
Supply voltage	VCC	-0.3	4.6	V	Note1 Note2
Supply voltage	IOVCC	-0.3	4.6	V	
Operating temperature	TOPR	-10	60	℃	
Storage temperature	TSTR	-20	70	℃	

6. Electrical Characteristics

Item		Symbol	Rating			Unit	Remark
			Min	Typ	Max		
Supply voltage		VCC	2.4	2.75	3.3	V	Note1
Supply voltage		IOVCC	1.65	1.8	3.3	V	
Input Voltage	L level	VIL	0	---	0.3*IOVCC	V	
	H level	VIH	0.7*IOVCC	---	IOVCC	V	

7. Module Function Description

7-1. Block Diagram Of LCM



7-2. Pin Description

PIN NO.	Symbol	I/O	Description
1	GND		Ground
2	LEDK		Power for LED backlight cathode
3	LEDA		Power for LED backlight anode
4	GND		Ground
5	VDD2.8V		Power Supply
6	WR		Write enable in MCU parallel interface. - Display data/command selection pin in 4-line serial interface. - Second Data lane in 2 data lane serial interface. -If not used, please fix this pin at VDDI or DGND.
7	RD		Read enable in 8080 MCU parallel interface. -If not used, please fix this pin at VDDI or DGND.
8	CS		Chip selection pin . Low enable. High disable
9	RS		-Display data/command selection pin in parallel interface. -This pin is used to be serial interface clock.(SCL) DCX='1': display data or parameter. DCX='0': command data. -If not used, please fix this pin at VDDI or DGND.
10	SDA		-When IM3: Low, SPI interface input/output pin. -When IM3: High, SPI interface input pin. -The data is latched on the rising edge of the SCL signal. -If not used, please fix this pin at VDDI or DGND level.
11	DB0		parallel interface data bus
12	DB1		parallel interface data bus
13	DB2		parallel interface data bus
14	DB3		parallel interface data bus
15	DB4		parallel interface data bus
16	DB5		parallel interface data bus
17	DB6		parallel interface data bus
18	DB7		parallel interface data bus
19	RESET		This signal will reset the device and it must be applied to properly initialize the chip.

<table>
<tr><td>20</td><td>VDD2.8V</td><td></td><td>Power Supply</td></tr>
<tr><td>21</td><td>IM0</td><td></td><td rowspan="3"><table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>MPU Interface Mode</th><th>Data pin</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>80-8bit parallel I/F</td><td>DB[7:0]</td></tr>
<tr><td colspan="6"></td></tr>
<tr><td rowspan="2">0</td><td rowspan="2">1</td><td rowspan="2">0</td><td rowspan="2">1</td><td>3-line 9bit serial I/F</td><td>SDA: in/out</td></tr>
<tr><td>2 data lane serial I/F</td><td>SDA: in/out
WRX: in</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>4-line 8bit serial I/F</td><td>SDA: in/out</td></tr>
</table></td></tr>
<tr><td>22</td><td>IM1</td><td></td></tr>
<tr><td>23</td><td>IM2</td><td></td></tr>
<tr><td>24</td><td>GND</td><td></td><td>Ground</td></tr>
</table>

7-3 Timing Characteristics

7.4.1 8080 Series MCU Parallel Interface Characteristics: 9/8-bit Bus

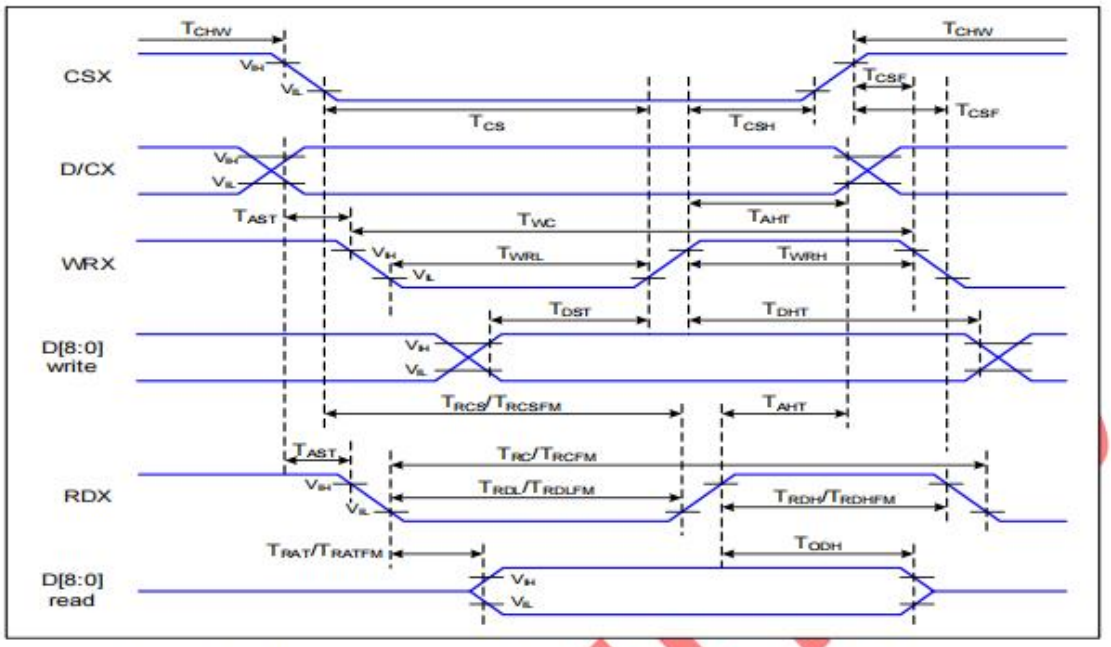


Figure 1 Parallel Interface Timing Characteristics (8080-Series MCU Interface)

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T_{AST}	Address setup time	TBD	-	ns	-
	T_{AHT}	Address hold time (Write/Read)	TBD	-	ns	
CSX	T_{CHW}	Chip select "H" pulse width	TBD	-	ns	-
	T_{CS}	Chip select setup time (Write)	TBD	-	ns	
	T_{RCS}	Chip select setup time (Read ID)	TBD	-	ns	
	T_{RCSFM}	Chip select setup time (Read FM)	TBD	-	ns	
	T_{CSF}	Chip select wait time (Write/Read)	TBD	-	ns	
	T_{CSH}	Chip select hold time	TBD	-	ns	
WRX	T_{WC}	Write cycle	TBD	-	ns	
	T_{WRH}	Control pulse "H" duration	TBD	-	ns	
	T_{WRL}	Control pulse "L" duration	TBD	-	ns	
RDX (ID)	T_{RC}	Read cycle (ID)	TBD	-	ns	When read ID data
	T_{RDH}	Control pulse "H" duration (ID)	TBD	-	ns	
	T_{RDL}	Control pulse "L" duration (ID)	TBD	-	ns	
RDX (FM)	T_{RCFM}	Read cycle (FM)	TBD	-	ns	When read from frame memory
	T_{RDHFM}	Control pulse "H" duration (FM)	TBD	-	ns	
	T_{RDLFM}	Control pulse "L" duration (FM)	TBD	-	ns	
D[8:0]	T_{DST}	Data setup time	TBD	-	ns	For CL=30pF

	T_{DHT}	Data hold time	TBD	-	ns	
	T_{RAT}	Read access time (ID)	-	TB-D	ns	
	T_{RATFM}	Read access time (FM)	-	TBD	ns	
	T_{ODH}	Output disable time	TBD	TBD	ns	

Table 4 8080 Parallel Interface Characteristics

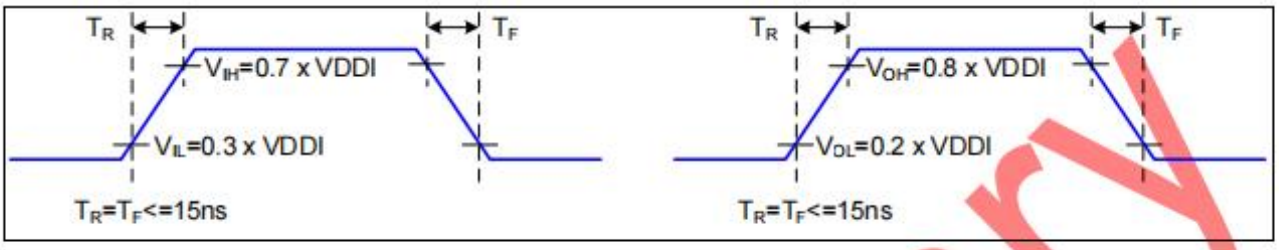


Figure 2 Rising and Falling Timing for I/O Signal

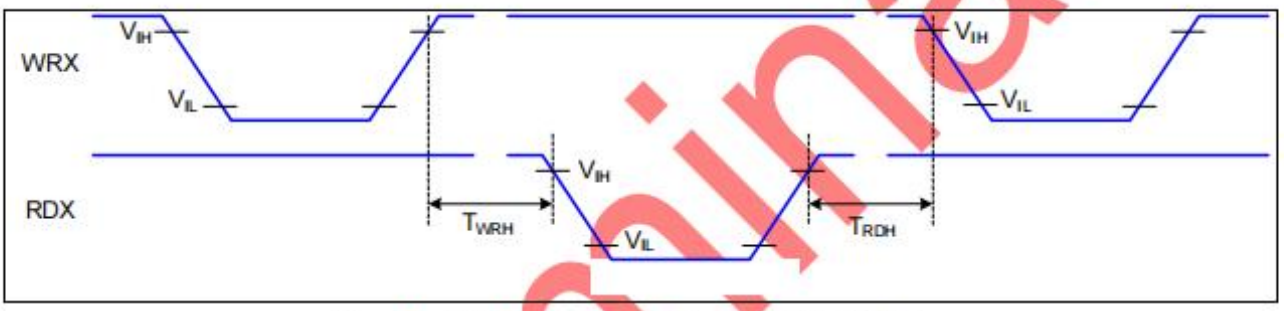


Figure 3 Write-to-Read and Read-to-Write Timing

Note: The rising time and falling time (Tr, Tf) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

7.4.2 Serial Interface Characteristics (3-line serial):

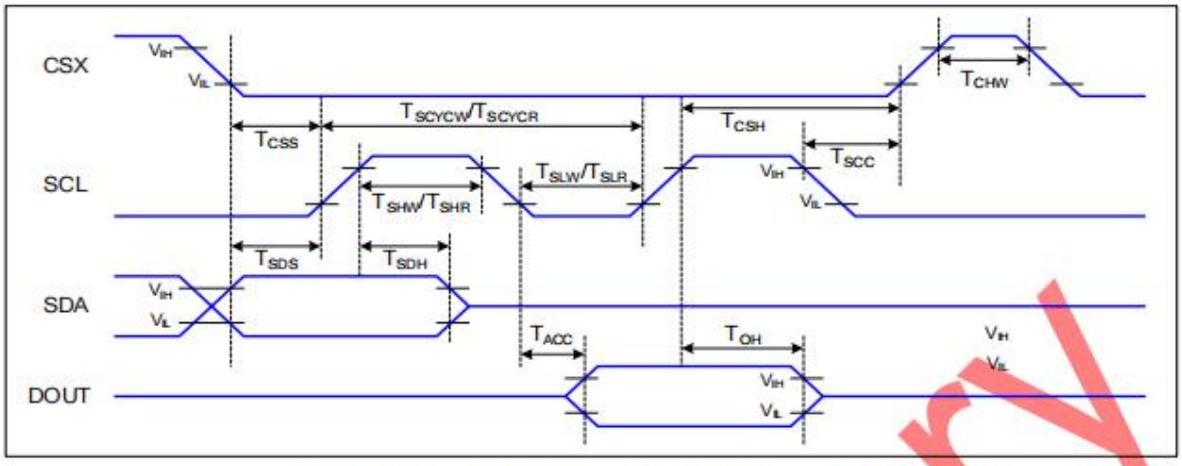


Figure 4 3-line serial Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	TBD	-	ns	
	T_{CSH}	Chip select hold time (write)	TBD	-	ns	
	T_{CSS}	Chip select setup time (read)	TBD	-	ns	
	T_{SCC}	Chip select hold time (read)	TBD	-	ns	
	T_{CHW}	Chip select "H" pulse width	TBD	-	ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	TBD	-	ns	
	T_{SHW}	SCL "H" pulse width (Write)	TBD	-	ns	
	T_{SLW}	SCL "L" pulse width (Write)	TBD	-	ns	
	T_{SCYCR}	Serial clock cycle (Read)	TBD	-	ns	
	T_{SHR}	SCL "H" pulse width (Read)	TBD	-	ns	
	T_{SLR}	SCL "L" pulse width (Read)	TBD	-	ns	
SDA (DIN)	T_{SDS}	Data setup time	TBD	-	ns	
	T_{SDH}	Data hold time	TBD	-	ns	
DOUT	T_{ACC}	Access time	TBD	TBD	ns	For maximum CL=30pF
	T_{OH}	Output disable time	TBD	TBD	ns	For minimum CL=8pF

Table 5 3-line serial Interface Characteristics

Note1 : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Note2 : In the read sequence of Serial interface, the 500nsec delay time is needed between read command and first read clock.

7.4.3 Serial Interface Characteristics (4-line serial):

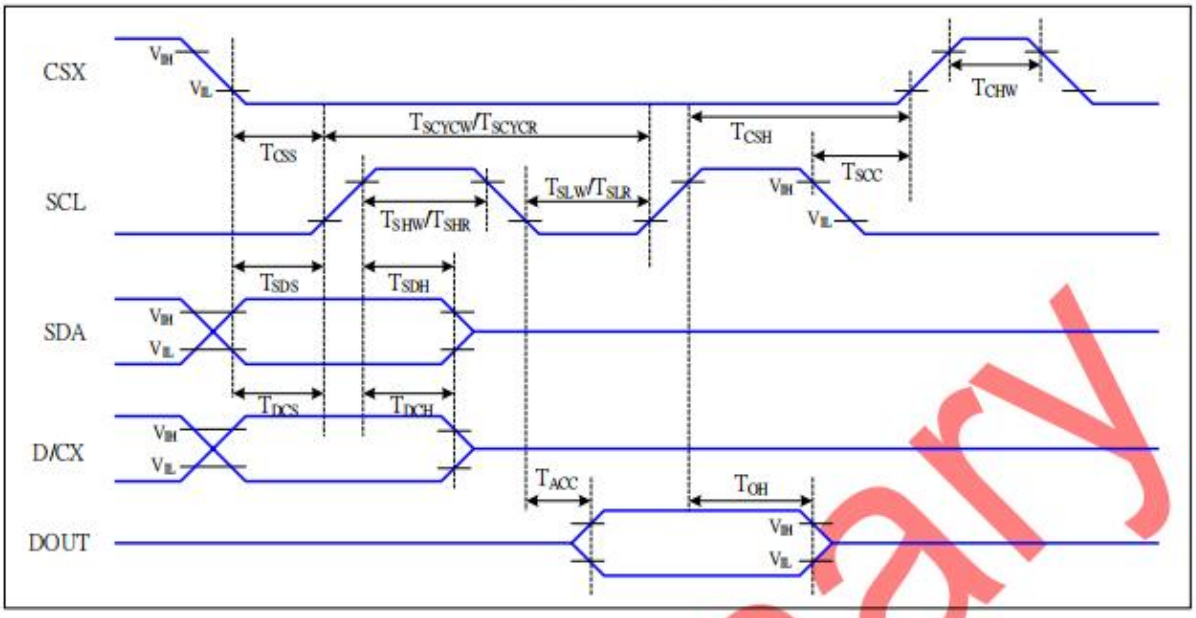


Figure 5 4-line serial Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	TBD	-	ns	
	T_{CSH}	Chip select hold time (write)	TBD	-	ns	
	T_{CSS}	Chip select setup time (read)	TBD	-	ns	
	T_{SCC}	Chip select hold time (read)	TBD	-	ns	
	T_{CHW}	Chip select “H” pulse width	TBD	-	ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	TBD	-	ns	-write command & data ram
	T_{SHW}	SCL “H” pulse width (Write)	TBD	-	ns	
	T_{SLW}	SCL “L” pulse width (Write)	TBD	-	ns	
	T_{SCYCR}	Serial clock cycle (Read)	TBD	-	ns	-read command & data ram
	T_{SHR}	SCL “H” pulse width (Read)	TBD	-	ns	
	T_{SLR}	SCL “L” pulse width (Read)	TBD	-	ns	
D/CX	T_{DCS}	D/CX setup time	TBD	-	ns	
	T_{DCH}	D/CX hold time	TBD	-	ns	
SDA (DIN)	T_{SDS}	Data setup time	TBD	-	ns	
	T_{SDH}	Data hold time	TBD	-	ns	
DOUT	T_{ACC}	Access time	TBD	TBD	ns	For maximum CL=30pF
	T_{OH}	Output disable time	TBD	TBD	ns	For minimum CL=8pF

Table 6 4-line serial Interface Characteristics

Note1 : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

7.4.5 Reset Timing:

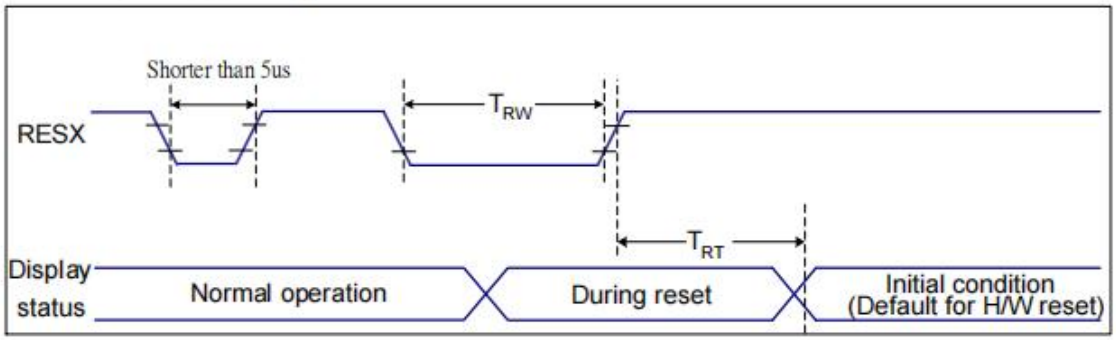


Figure 7 Reset Timing

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120 (Note 1, 6, 7)	ms

Table 9 Reset Timing

Notes:

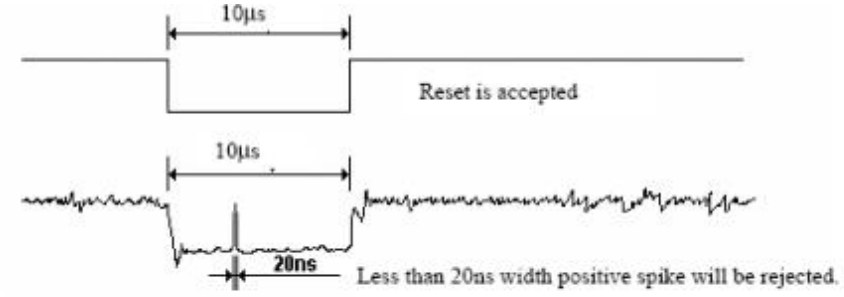
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

8. Electro-Optical Characteristics

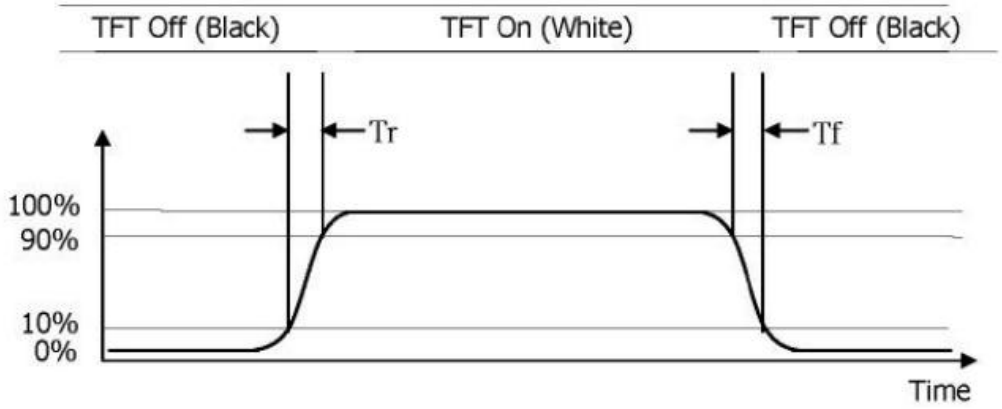
Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time		Tr +Tf	θx = θy =0	---	16	25	ms	Note 1
Contrast Ratio		CR		300	500	---	---	Note 2
Transmittance		T%		5.9	4.7	---	%	
Color Chromaticity (CIE1931)	White	W x	θx = θy =0	---	0.304	---	---	
		W y		---	0.344	---	---	
Viewing angle	θ_T		CR > 10	35	45	---	Deg.	Note 3
	θ_B			35	45	---		
	θ_L			35	50	---		
	θ_R			20	20	---		
Luminance (I_F = 80mA)		L		---	350	---	cd/m2	Note4

Note :

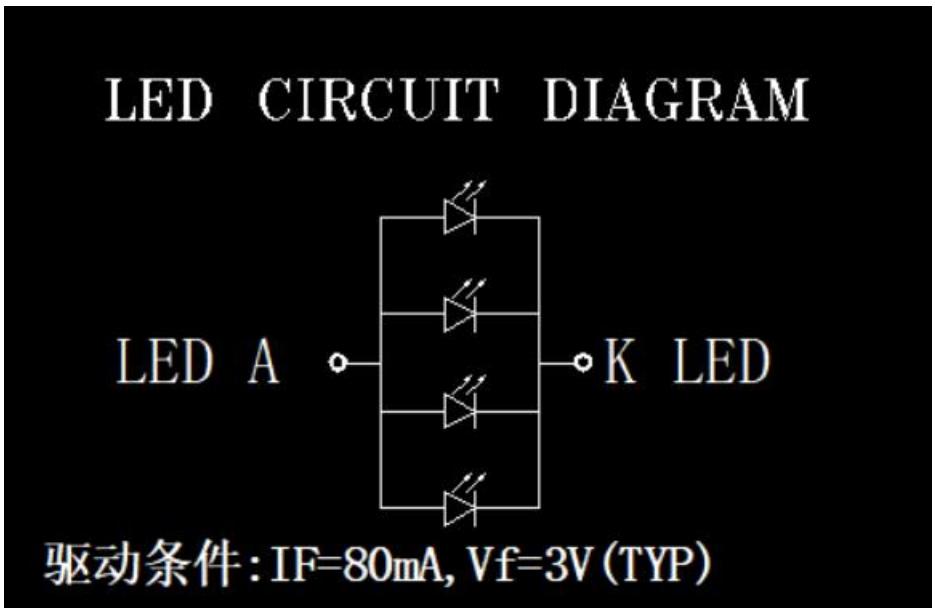
1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface.
2. Contrast measurements shall be made at viewing angle of θ= 0° and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (See FIGURE 1 shown in Appendix) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Center Luminance of white is defined as the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in FIGURE 4 for a total of the measurements per display.
4. The White luminance uniformity on LCD surface is then expressed as : ΔY = Minimum Luminance of 9 Points or 5 points / Maximum Luminance of 9 Points or 5 points(See FIGURE 2).
5. The color chromaticity coordinates specified in Table 5. shall be calculated from the spectral data measured with C light. Measurements shall be made at the center of the panel.
6. The electro-optical response time measurements shall be made as FIGURE 5 shown in Appendix by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Td, and 90% to 10% is Tr.



Note(4) Backlight circuit



9.Records Of Version

Version	Revise Date	Page	Content
00	2025-5-12	ALL	New released