PRODUCT SPECIFICATION FOR LCD MODULE

Revision: 1.0

Model No: LS024T04-M-V2

Module Type: COG+FPC+B/L

APPROVED SIGNATURE

■ Approved Product Specification only

□ Approved Product Specification and Samples

Prepared By	Checked By	Approved By

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1. General Description

LS024T04-M-V2 is a transmissive type a-Si TFT-LCD (amorphous silicon thin film transistor liquid crystal display) module, which is composed of a TFT-LCD panel, a driver circuit and a backlight unit. The panel size is 2.4 inch and the resolution is 240(RGB)*320, the panel can display up to 262k colors.

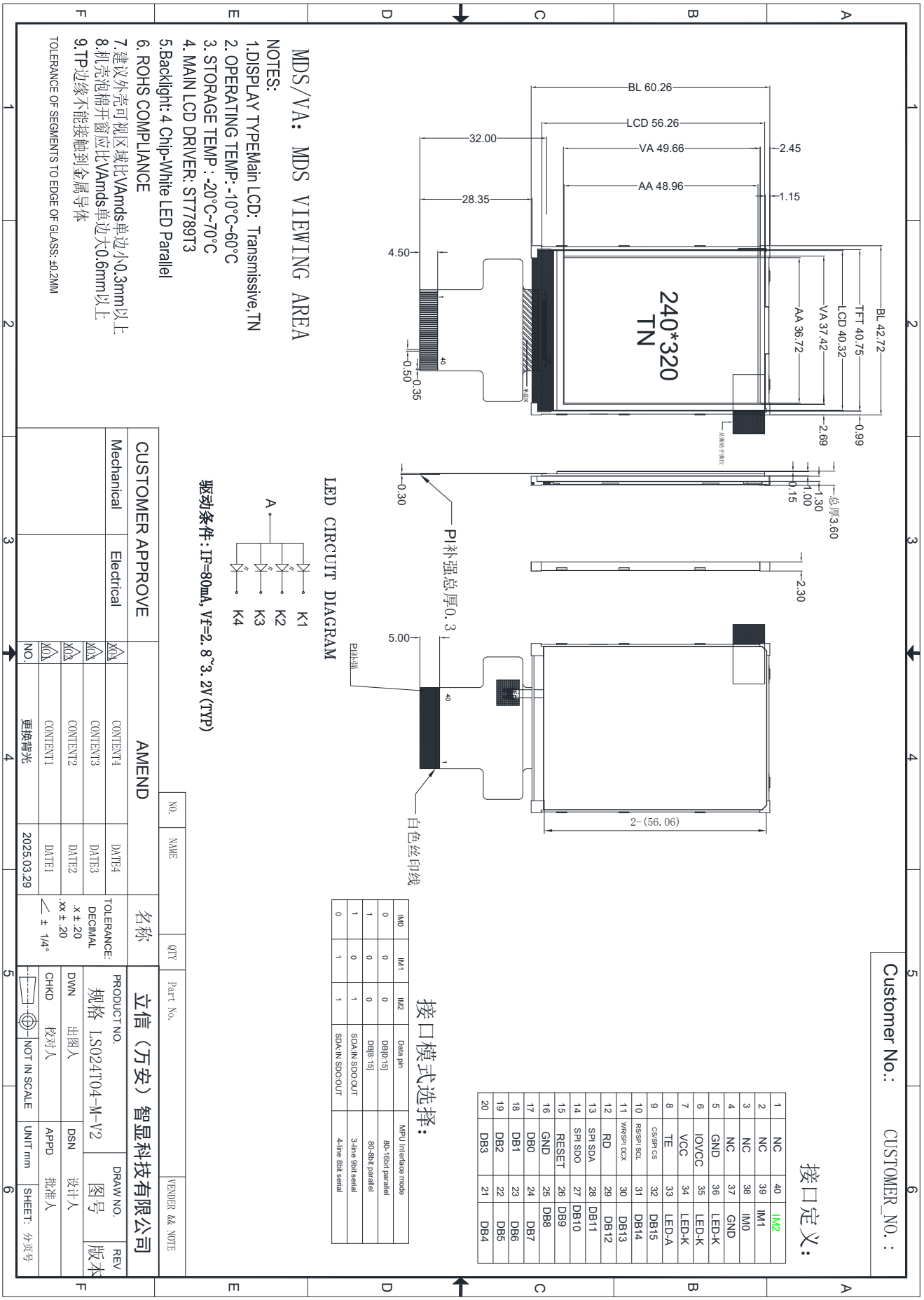
2. Physical Features

Display Mode	TFT-LCD Module
	Active matrix TFT, Transmissive type
Display Format	Graphic 240(RGB)×320 Dot-matrix
Input Data	3 线串口/4 线串口/8 bits /16bits parallel interface
Viewing Direction （Grayscale Inversion）	TN
Drive	ST7789T3

3. Mechanical Specification

Item	Specification	Unit
Module size (H×V×D)	42.72 ×60.26 ×2.15	mm
Number of dots	240(RGB) ×320	pixel
Active area (H×V)	36.72×48.96	mm

4. Outline Dimension



5. Absolute Maximum Ratings

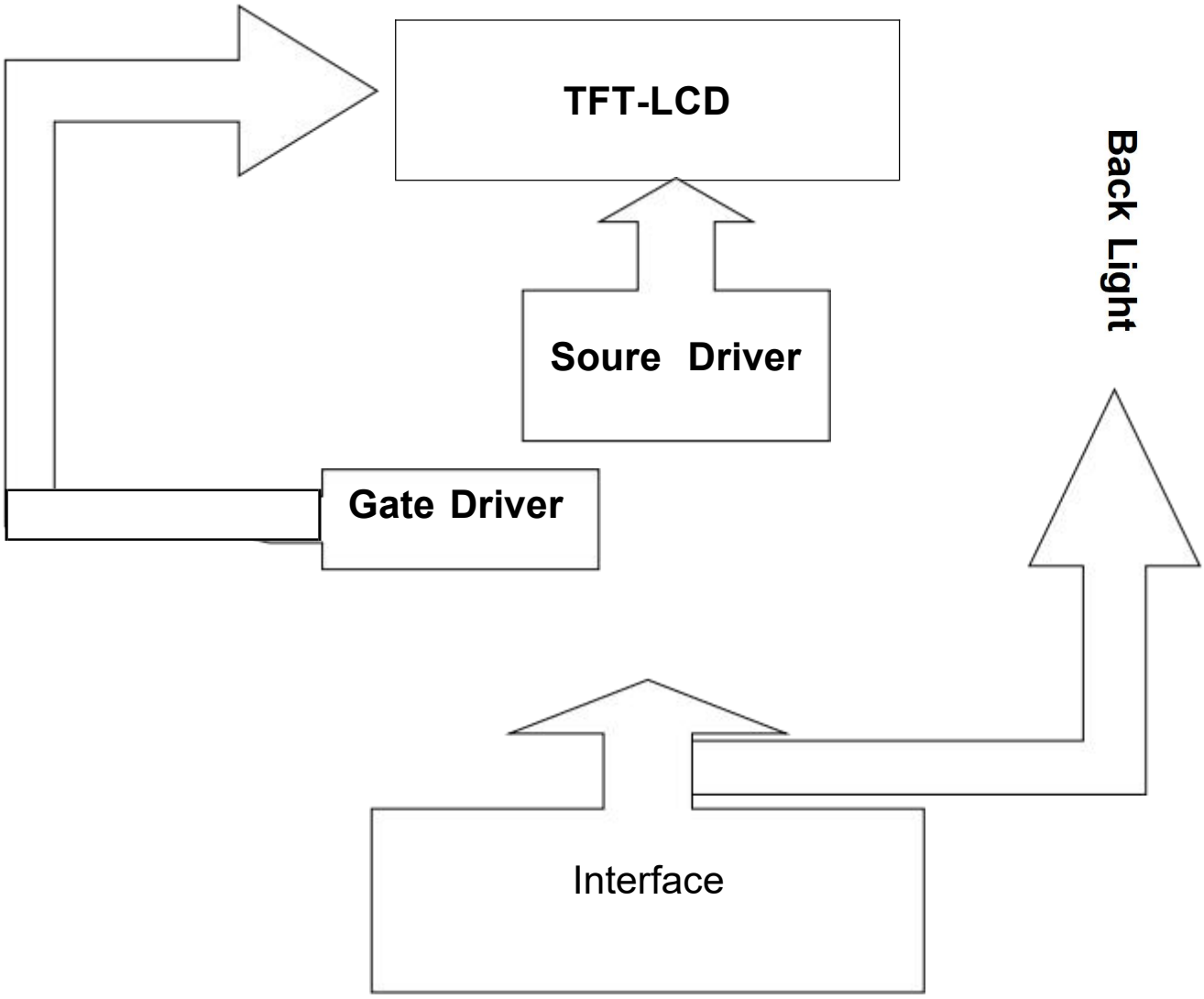
Item	Symbol	Min	Max	Unit	Remark
Supply voltage	VCC	-0.3	4.6	V	Note1 Note2
Supply voltage	IOVCC	-0.3	4.6	V	
Operating temperature	TOPR	-20	70	℃	
Storage temperature	TSTR	-30	80	℃	

6. Electrical Characteristics

Item		Symbol	Rating			Unit	Remark
			Min	Typ	Max		
Supply voltage		VCC	2.4	2.75	3.3	V	Note1
Supply voltage		IOVCC	1.65	1.8	3.3	V	
Input Voltage	L level	VIL	0	---	0.3*IOVCC	V	
	H level	VIH	0.7*IOVCC	---	IOVCC	V	

7. Module Function Description

7-1. Block Diagram Of LCM



7-2. Pin Description

PIN No.	Symbol	Description
1	NC	
2	NC	
3	NC	
4	NC	
5	GND	Ground （接地脚）
6	IOVCC	Power supply for LCM（2.8V-3.3V） （屏供电脚）
7	VCI	Power supply for LCM（2.8V-3.3V） （屏供电脚）
8	FMARK	Tearing effect output pin to synchronize MPU to frame writing, activated by S/W command. When this pin is not activated, this pin is low. If not used, open this pin. (帧同信号,不用时悬空)
9	CS/SPI CS	Chip select pin ("Low" enable) （屏驱动芯片片选脚，低电平有效）
10	RS/SPI SCL/SCK	This pin is used to select "Data or Command" in the parallel interface or serial data interface. (用于并口或者串口) Parallel(并口): When RS= '1', data is selected.(选择数据) When RS= '0', command is selected.(选择寄存器) Serial(串口): This pin is used serial interface clock in 3-wire 9-bit / 4-wire 8-bit serial data interface. (3线串口或者4线串口的时钟信号)

		If not used, this pin should be connected to IOVCC or GND. (不用时接 IOVCC 或者接地)
11	WR/A0(4 线)	Serves as a write signal and writes data at the rising edge. - 4-line system (D/CX): Serves as command or parameter select. *Fix to*IOVCC *level when not in use.* （并口的写控制脚或者 4 线串口的寄存器/数据选择， 不用时接 IOVCC）
12	RD	Serves as a read signal and MCU read data at the rising edge. *Fix to* IOVCC *level when not in use.* （并口的读控制脚,不用时接 IOVCC）
13	SPI SDI/SDA	Serial input signal. The data is applied on the rising edge of the SCL signal. If not used, fix this pin at IOVCC or GND (串口数据输入信号,不用时接 IOVCC 或者接地)
14	SPI SDO	Serial output signal. The data is outputted on the falling edge of the SCL signal. If not used, open this pin (串口数据输出信号， 不用时悬空)
15	RESET	LCM Reset pin Signal is active low. （屏复位脚,低电平复位）
16	GND	Ground （接地脚）
17-24	DB0-DB7	Data bus *Fix to* GND *level when not in use* (低 8 位数据线,不用时接地)
25-32	DB8-DB15	Data bus *Fix to* GND *level when not in use* (高 8 位数据线,不用时接地)
33	A	Anode of Backlight (3.0V-3.4V Typical:3.2V) （背光正极供电脚,电压范围:3.0-3.4V,典型值:3.2V）
34-36	K	Cathode of Backlight （背光负极供电脚）
37	GND	Ground （接地脚）

38	IM0	Select the MCU interface mode
39	IM1	
40	IM2	**NOTE:** D[8:1]即低 8 位数据线 DB7-DB0D D[17:10]即高 8 位数据线 DB15-DB8

IM0	IM1	IM2	Data pin	MPU Interface Mode
0	0	0	DB[0:15]	80-16bit paralle
1	0	0	DB[8:15]	80-8bit parallel
1	0	1	SDA:IN SDO:OUT	3-line 9bit serial
0	1	1	SDA:IN SDO:OUT	4-line 8bit serial

7-3 Timing Characteristics

7.4.1 8080 Series MCU Parallel Interface Characteristics: 18/16/9/8-bit Bus

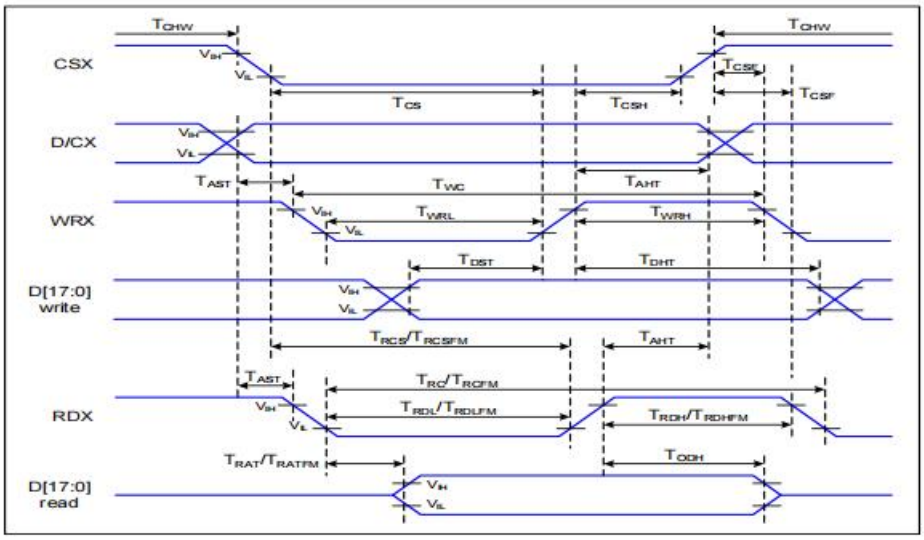


Figure 1 Parallel Interface Timing Characteristics (8080-Series MCU Interface)

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T_{AST}	Address setup time	0		ns	-
	T_{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T_{CHW}	Chip select "H" pulse width	0		ns	-
	T_{CS}	Chip select setup time (Write)	15		ns	
	T_{RCS}	Chip select setup time (Read ID)	45		ns	
	T_{RCSFM}	Chip select setup time (Read FM)	355		ns	
	T_{CSF}	Chip select wait time (Write/Read)	10		ns	
	T_{CSH}	Chip select hold time	10		ns	
WRX	T_{WC}	Write cycle	66		ns	
	T_{WRH}	Control pulse "H" duration	15		ns	
	T_{WRL}	Control pulse "L" duration	15		ns	
RDX (ID)	T_{RC}	Read cycle (ID)	160		ns	When read ID data
	T_{RDH}	Control pulse "H" duration (ID)	90		ns	
	T_{RDL}	Control pulse "L" duration (ID)	45		ns	
RDX (FM)	T_{RCFM}	Read cycle (FM)	450		ns	When read from frame memory
	T_{RDHFM}	Control pulse "H" duration (FM)	90		ns	
	T_{RDLFM}	Control pulse "L" duration (FM)	355		ns	
D[17:0]	T_{DST}	Data setup time	10		ns	For CL=30pF
	T_{DHT}	Data hold time	10		ns	
	T_{RAT}	Read access time (ID)		40	ns	
	T_{RATFM}	Read access time (FM)		340	ns	
	T_{ODH}	Output disable time	20	80	ns	

Table 4 8080 Parallel Interface Characteristics

7.4.2 Serial Interface Characteristics (3-line serial):

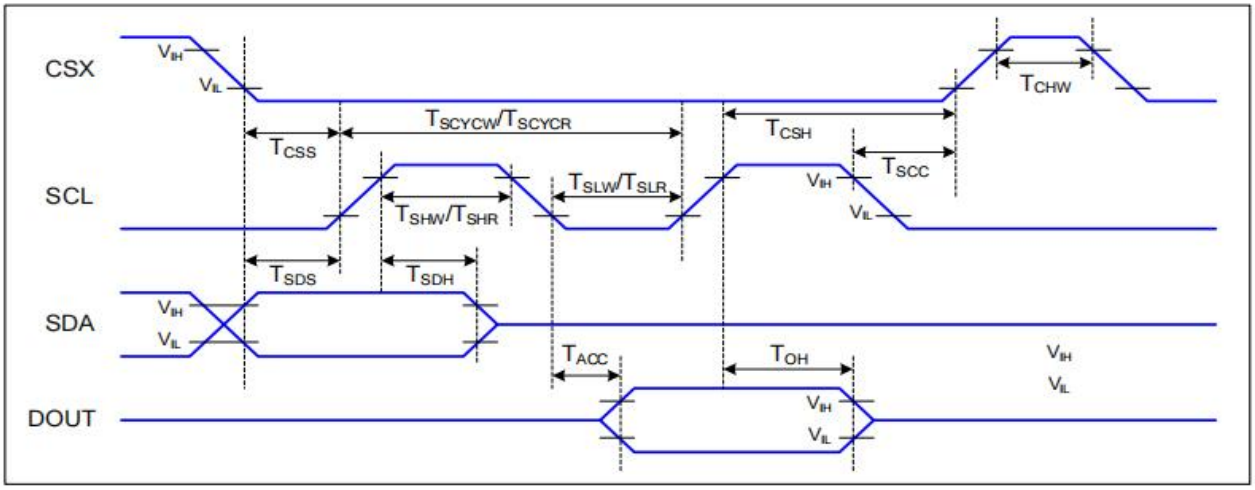


Figure 4 3-line serial Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select “H” pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	16		ns	
	T_{SHW}	SCL “H” pulse width (Write)	7		ns	
	T_{SLW}	SCL “L” pulse width (Write)	7		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL “H” pulse width (Read)	60		ns	
	T_{SLR}	SCL “L” pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	7		ns	
	T_{SDH}	Data hold time	7		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

Table 5 3-line serial Interface Characteristics

Note1 : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals

Note2: In the read sequence of serial interface, the 500nsec delay time is needed between read command and first read clock..

7.4.3 Serial Interface Characteristics (4-line serial):

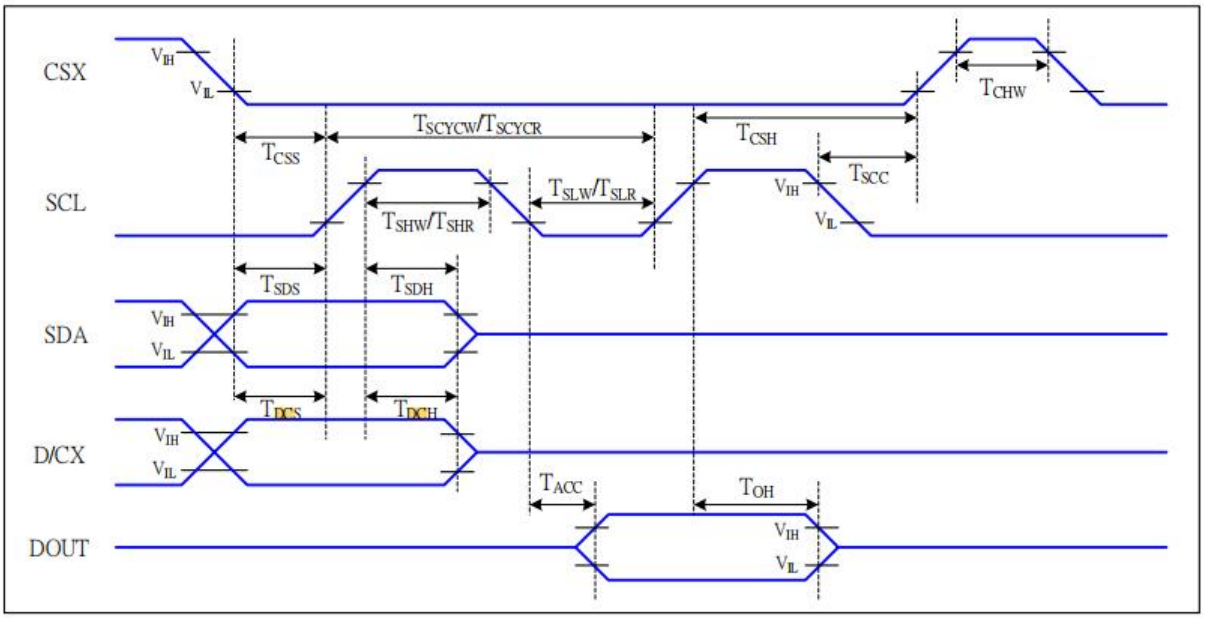


Figure 5 4-line serial Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select “H” pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	16		ns	-write command & data ram
	T_{SHW}	SCL “H” pulse width (Write)	7		ns	
	T_{SLW}	SCL “L” pulse width (Write)	7		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	-read command & data ram
	T_{SHR}	SCL “H” pulse width (Read)	60		ns	
	T_{SLR}	SCL “L” pulse width (Read)	60		ns	
D/CX	T_{DCS}	D/CX setup time	10		ns	
	T_{DCH}	D/CX hold time	10		ns	
SDA (DIN)	T_{SDS}	Data setup time	7		ns	
	T_{SDH}	Data hold time	7		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

Table 6 4-line serial Interface Characteristics

8. Electro-Optical Characteristics

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time		Tr +Tf	θx = θy =0	---	30	---	ms	Note 1
Contrast Ratio		CR		---	250	---	---	Note 2
Transmittance		T%		4.5	5	---	%	
Color Chromaticity (CIE1931)	White	W x	θx = θy =0	---	0.308	---	---	
		W y		---	0.325	---	---	
Viewing angle	θ_T		CR > 10	---	45	---	Deg.	Note 3
	θ_B			---	20	---		
	θ_L			---	45	---		
	θ_R			---	45	---		
Luminance (I_F = 80mA)		L			TBD	---	cd/m2	Note4

Note 1: Ambient temperature = 25°C.

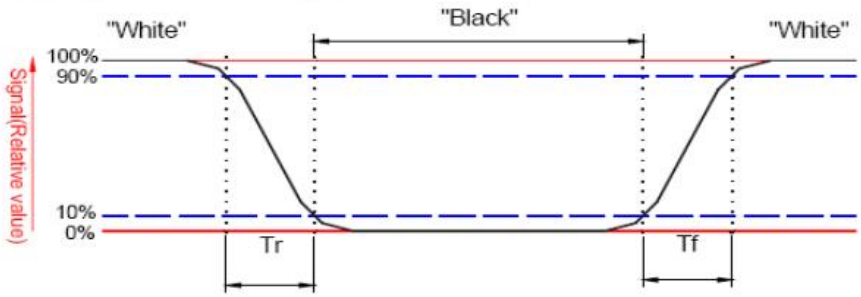
Note 2: To be measured with a viewing cone of 2°by Topcon luminance meter BM-5A.

Note 3: To be measured with Otsuta chromaticity meter LCF-2100M，CF only measure under C light simulation.

Note 4: CTC shipping status is cell without polarizer. Transmittance of Specification is cell with polarizer

Note 5: Definition of response time:

The output signals of TRD-100 are measured when the input signals are changed to “White” (falling time) and from “White” to “Black” (rising time), respectively. The interval is between the 10% and 90% of amplitudes. Refer to figure as below.

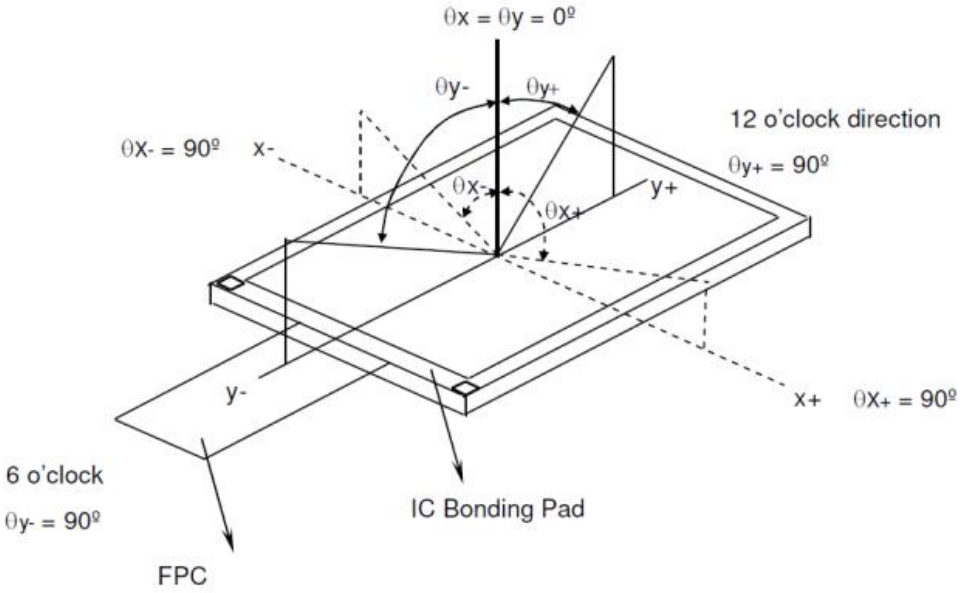


Note 6: Definition of contrast ratio:

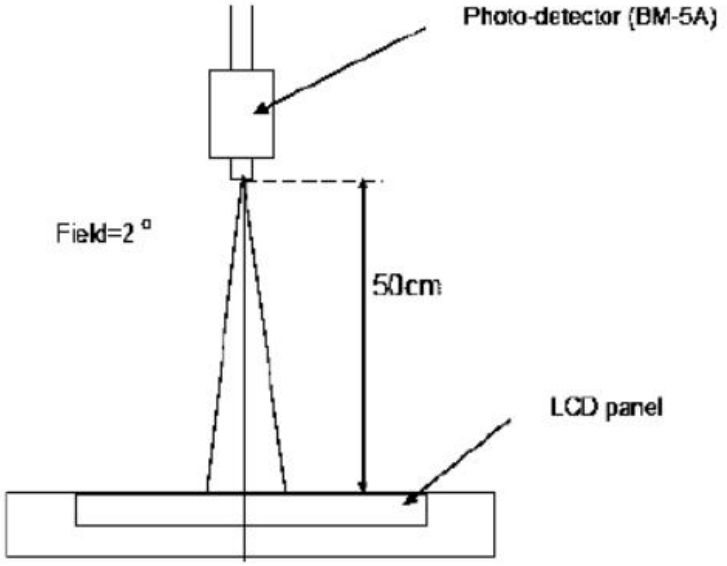
Contrast ratio is calculated by the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "white" state}}{\text{Brightness on the "black" state}}$$

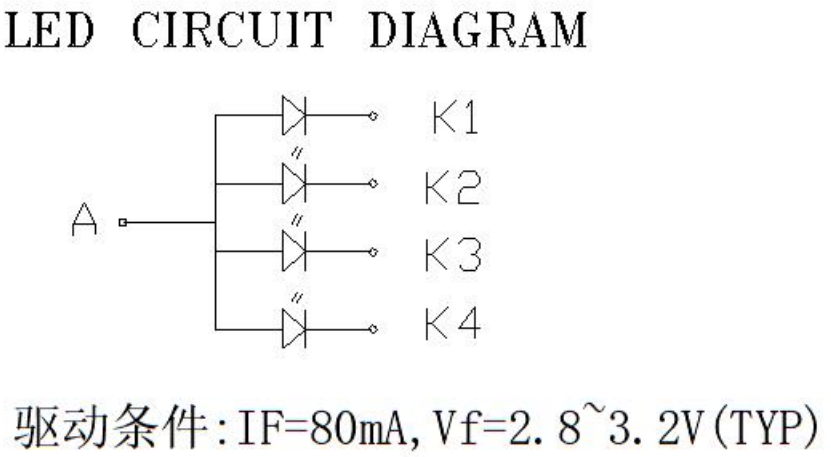
Note 7: Definition of viewing angle



Note 8: Optical characteristic measurement setup.



Note(4) Backlight circuit



9.Records Of Version

Version	Revise Date	Page	Content
00	2024-3-30	ALL	New released