

PRODUCT SPECIFICATION **FOR LCD MODULE**

Revision: 1.0

Model No: LSC020I09-R-V2

Module Type: COG+FPC+B/L+CTP

APPROVED SIGNATURE

- ☒ Approved Product Specification only
- ☐ Approved Product Specification and Samples

<u>Prepared By</u>	<u>Checked By</u>	<u>Approved By</u>

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1. General Description

LSC020I09-R-V2 is a transmissive type a-Si TFT-LCD (amorphous silicon thin film transistor liquid crystal display) module, which is composed of a TFT-LCD panel, a driver circuit and a backlight unit. The panel size is 2.0 inch and the resolution is 240(RGB)*320, the panel can display up to 262k colors.

2. Physical Features

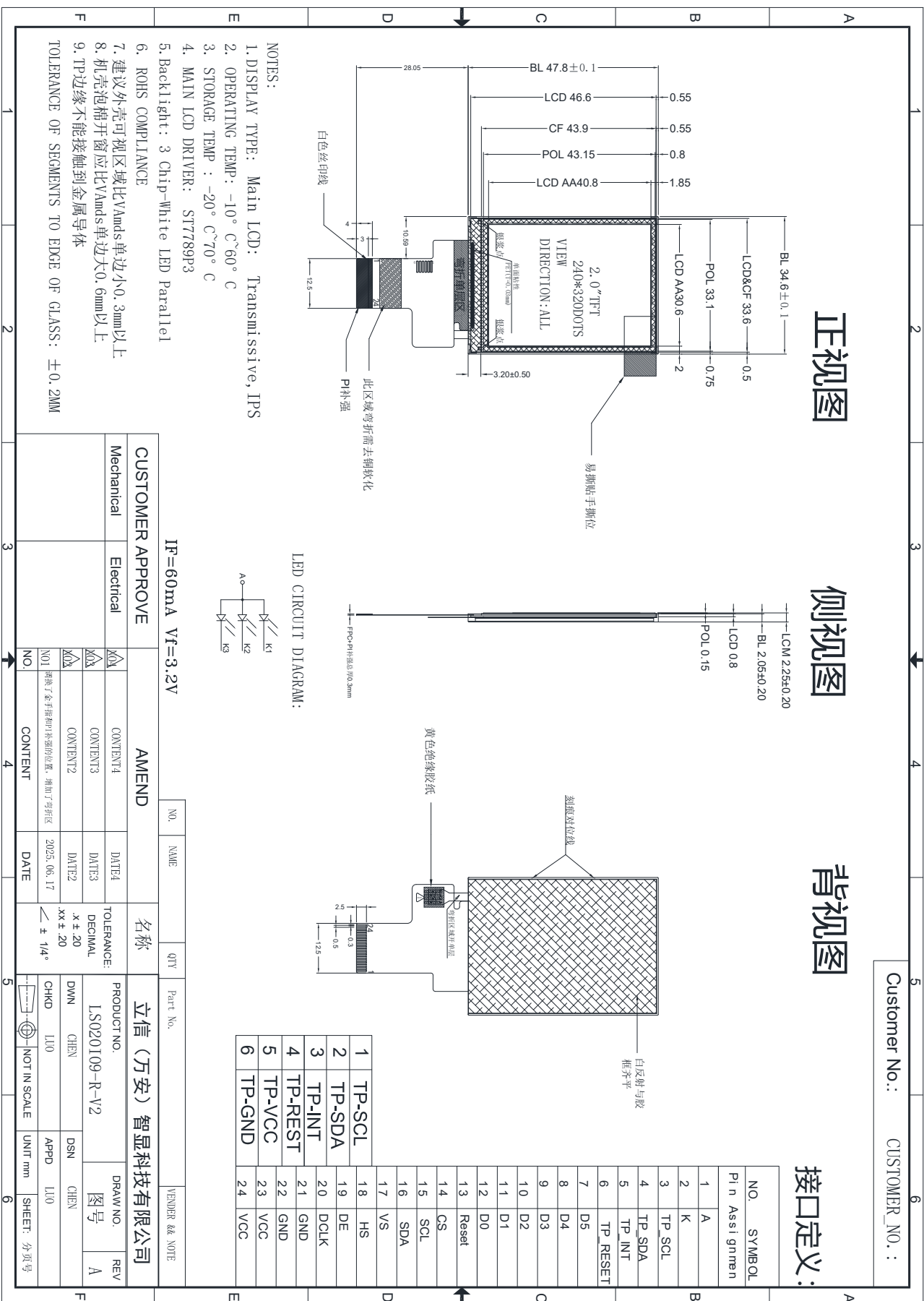
Display Mode	TFT-LCD Module
	Active matrix TFT, Transmissive type
Display Format	Graphic 240(RGB)×320 Dot-matrix
Input Data	6 RGB
Viewing Direction (Grayscale Inversion)	IPS
Drive	ST7789P3

3. Mechanical Specification

Item	Specification	Unit
Module size (H×V×D)	39.24 ×59.24 ×3.38	mm
Number of dots	240(RGB) ×320	pixel
Active area (H×V)	30.6×40.8	mm

4. Outline Dimension

LCM



5. Absolute Maximum Ratings

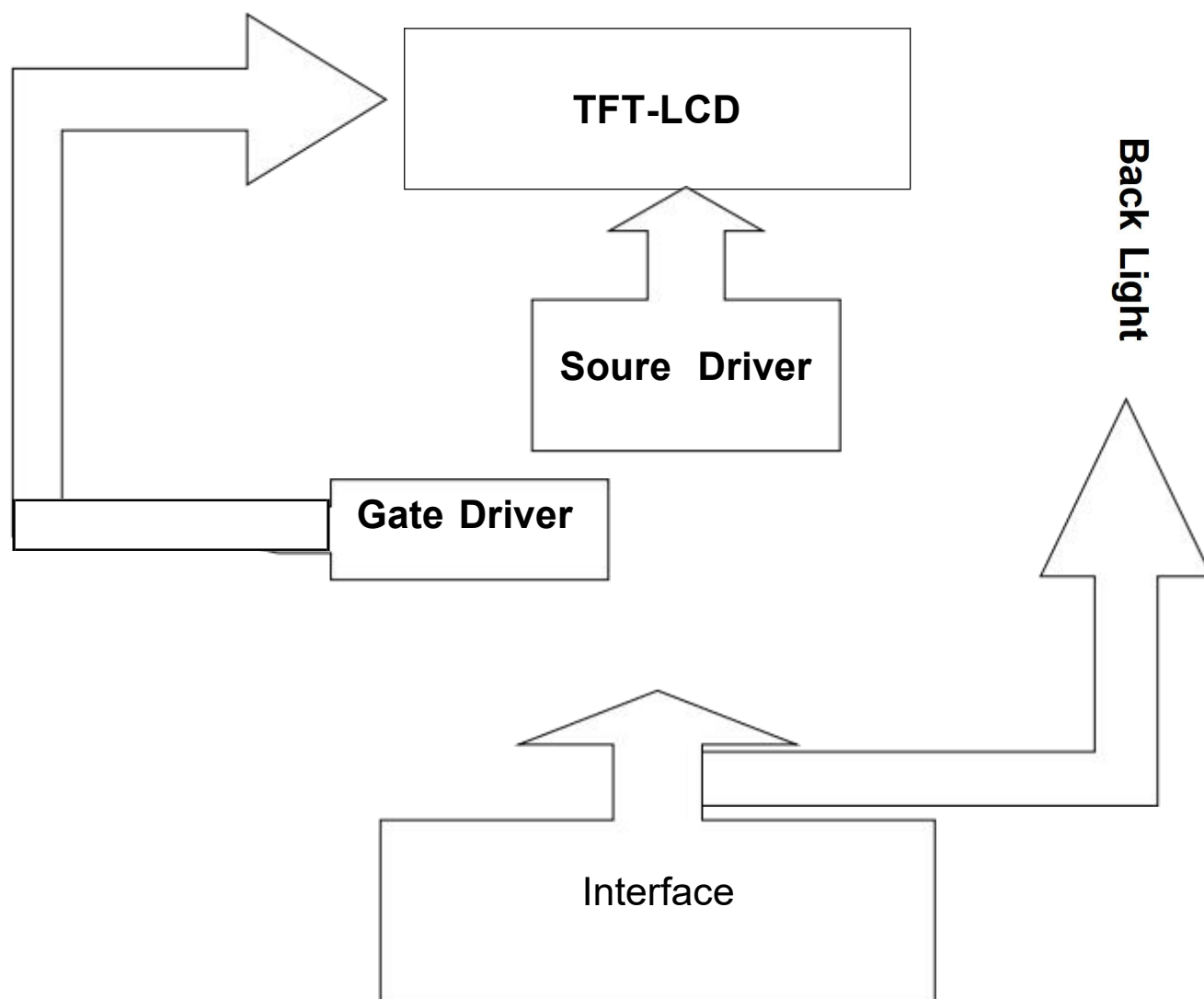
Item	Symbol	Min	Max	Unit	Remark
Supply voltage	VDD	-0.3	4.6	V	Note1 Note2
Operating temperature	TOPR	-10	60	°C	
Storage temperature	TSTR	-20	70	°C	

6. Electrical Characteristics

Item		Symbol	Rating			Unit	Remark
			Min	Typ	Max		
Supply voltage		VDD	2.4	2.8	3.3	V	Note1
Input Voltage	L level	VIL	0	---	0.3*IOVCC	V	
	H level	VIH	0.7*IOVCC	---	IOVCC	V	

7. Module Function Description

7-1. Block Diagram Of LCM



7-2. Pin Description

PIN NO.	Symbol	I/O	Description
1	A	P	Back light anode +
2	K	P	Back light cathode -
3	TP_SCL	I	SCL pin for TP
4	TP_SDA	I	SDA pin for TP
5	TP_INT	I	Interrupt signal for TP
6	TP_RESET	I	Reset Pin for TP
7	D5	I	data bus
8	D4	I	data bus
9	D3	I	data bus
10	D2	I	data bus
11	D1	I	data bus
12	D0	I	data bus
13	RESET	I	Reset signal
14	CS	I	Chip select pin
15	SCL	I	serial interface clock
16	SDA	I	Serial data input
17	VS	I	Vertical (Frame) synchronizing input signal for RGB interface operation.
18	HS	I	Horizontal (Line) synchronizing input signal for RGB interface operation
19	DE	I	Data enable signal for RGB interface operation.
20	DCLK	I	Dot clock signal for RGB interface operation.
21	GND	P	Ground
22	GND	P	Ground
23	VCC	P	Power supply 2.8~3.3V
24	VCC	P	Power supply 2.8~3.3V

7-3 Timing Characteristics

7.4.2 Serial Interface Characteristics (3-line serial):

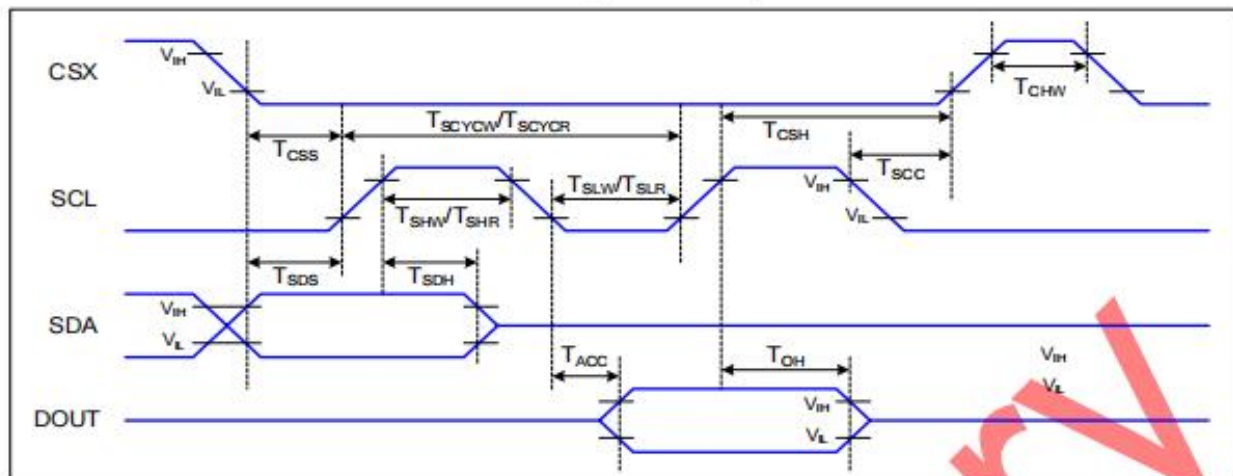


Figure 4 3-line serial Interface Timing Characteristics

$V_{DDI}=1.65$ to $3.3V$, $V_{DD}=2.4$ to $3.3V$, $AGND=DGND=0V$, $T_a=25^{\circ}C$

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	TBD	-	ns	
	T_{CSH}	Chip select hold time (write)	TBD	-	ns	
	T_{CSS}	Chip select setup time (read)	TBD	-	ns	
	T_{SCC}	Chip select hold time (read)	TBD	-	ns	
	T_{CHW}	Chip select "H" pulse width	TBD	-	ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	TBD	-	ns	
	T_{SHW}	SCL "H" pulse width (Write)	TBD	-	ns	
	T_{SLW}	SCL "L" pulse width (Write)	TBD	-	ns	
	T_{SCYCR}	Serial clock cycle (Read)	TBD	-	ns	
	T_{SHR}	SCL "H" pulse width (Read)	TBD	-	ns	
	T_{SLR}	SCL "L" pulse width (Read)	TBD	-	ns	
SDA (DIN)	T_{SDS}	Data setup time	TBD	-	ns	
	T_{SDH}	Data hold time	TBD	-	ns	
DOUT	T_{ACC}	Access time	TBD	TBD	ns	For maximum $CL=30pF$
	T_{OH}	Output disable time	TBD	TBD	ns	For minimum $CL=8pF$

Table 5 3-line serial Interface Characteristics

Note1 : The rising time and falling time (T_r , T_f) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of V_{DDI} for Input signals.

Note2 : In the read sequence of Serial interface, the 500nsec delay time is needed between read command and first read clock.

7.4.4 RGB Interface Characteristics:

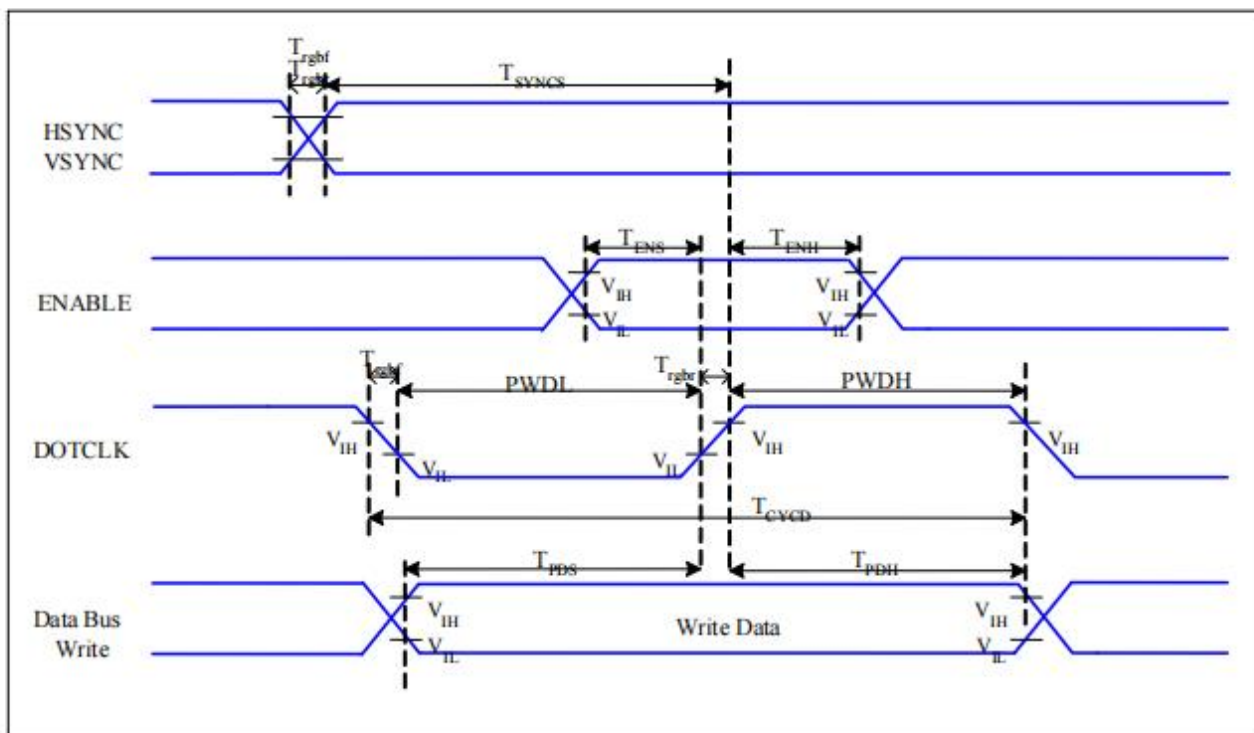


Figure 6 RGB Interface Timing Characteristics

$V_{DDI}=1.65$ to $3.3V$, $V_{DD}=2.4$ to $3.3V$, $AGND=DGND=0V$, $T_a=25^{\circ}C$

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	TBD	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	TBD	-	ns	
	T_{ENH}	Enable Hold Time	TBD	-	ns	
DOTCLK	$PWDH$	DOTCLK High-level Pulse Width	TBD	-	ns	
	$PWDL$	DOTCLK Low-level Pulse Width	TBD	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	TBD	-	ns	
	T_{trghf} , T_{trghf}	DOTCLK Rise/Fall time	-	TBD	ns	
DB	T_{PDS}	PD Data Setup Time	TBD	-	ns	
	T_{PDH}	PD Data Hold Time	TBD	-	ns	

Table 7 6 Bits RGB Interface Timing Characteristics

7.4.5 Reset Timing:

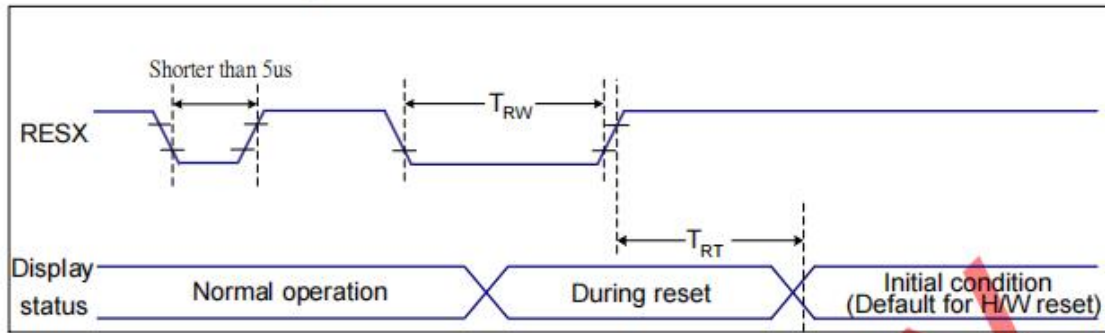


Figure 7 Reset Timing

$V_{DDI}=1.65$ to $3.3V$, $V_{DD}=2.4$ to $3.3V$, $AGND=DGND=0V$, $T_a=25^{\circ}C$

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	TBD	-	us
	TRT	Reset cancel	-	TBD (Note 1, 5)	ms
			-	TBD (Note 1, 6, 7)	ms

Table 8 Reset Timing

Notes:

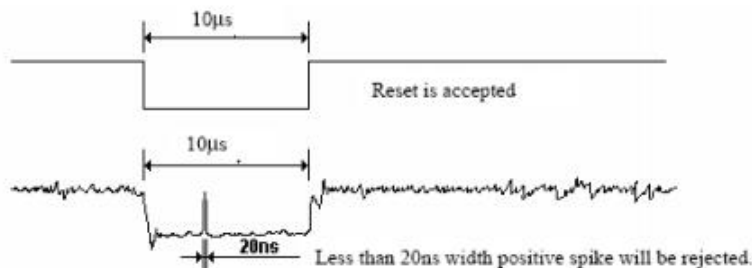
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is H/W reset cancel time (t_{RT}) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

8. Electro-Optical Characteristics

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time		Tr +Tf	$\theta_x = \theta_y = 0$	---	30	35	ms	Note 1
Contrast Ratio		CR		800	1000	---	---	Note 2
Transmittance		T%		---	4.5	---	%	
Color Chromaticity (CIE1931)	White	W x	$\theta_x = \theta_y = 0$	---	0.302	---	---	
		W y		---	0.319	---	---	
Viewing angle	θ_T		CR > 10	---	85	---	Deg.	Note 3
	θ_B			---	85	---		
	θ_L			---	85	---		
	θ_R			---	85	---		
Luminance ($I_F = 60mA$)		L		---	TBD	---	cd/m2	Note4

Notes : 1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see FIGURE 1).

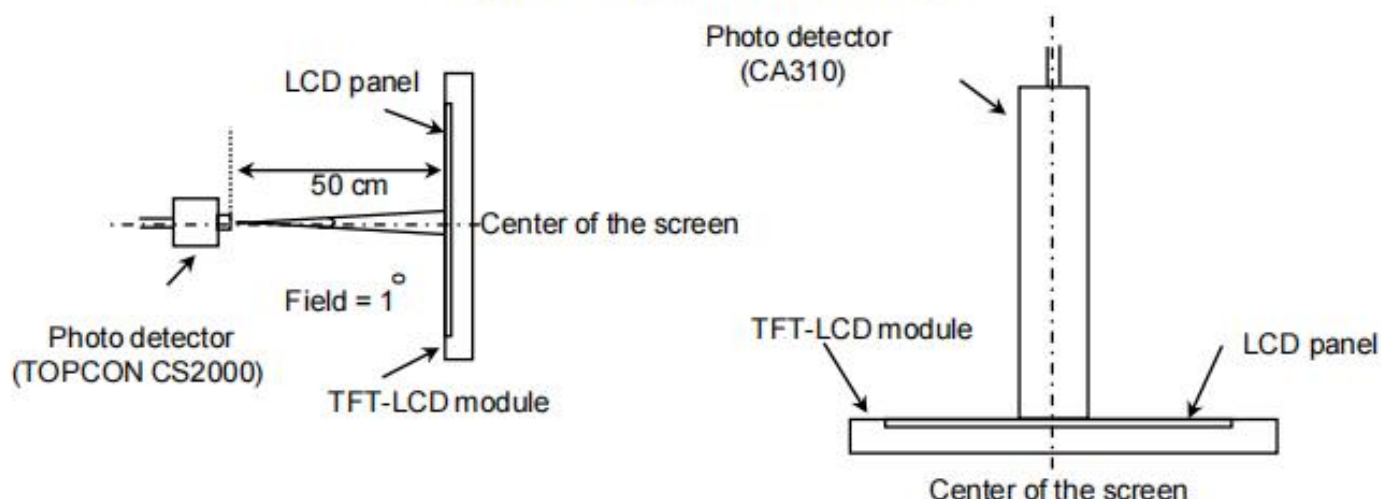
2. Contrast measurements shall be made at viewing angle of $\Theta = 0$ and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state . (see FIGURE 1) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. The color chromaticity coordinates specified in Table 5. shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.
4. The electro-optical response time measurements shall be made as FIGURE 2 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Tr, and 90% to 10% is Td.

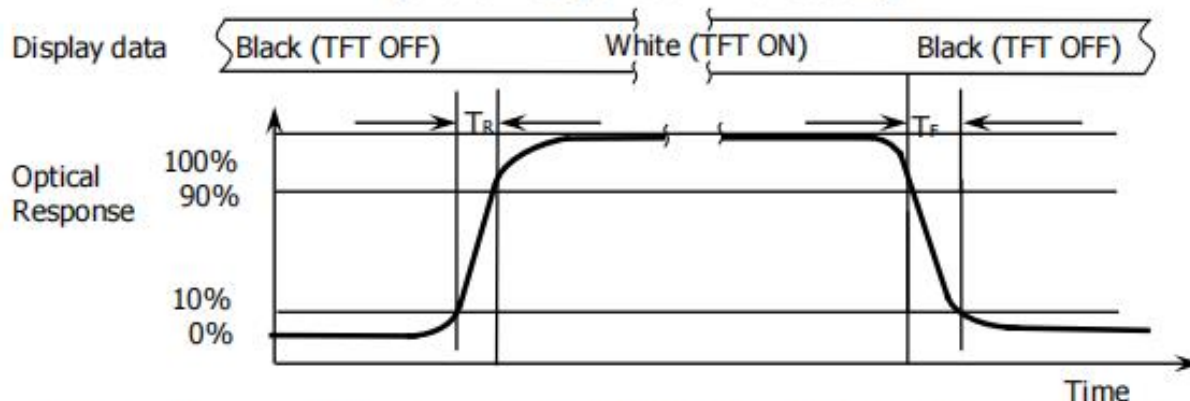
4.2 Optical measurements

Figure 4. Measurement Set Up



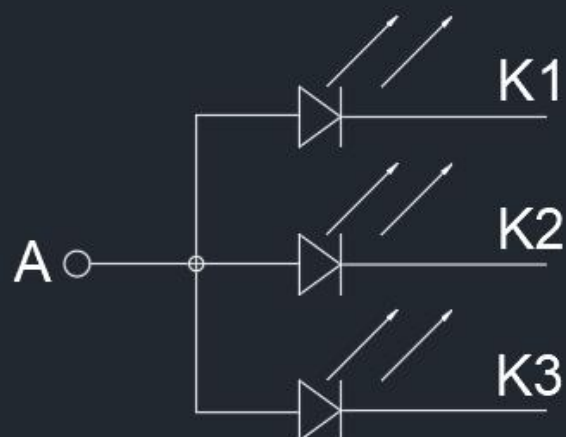
View angel range, uniformity, etc. measurement setup Flicker, measurement setup

Figure 5. Response Time Testing



The electro-optical response time measurements shall be made as shown in FIGURE 3 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is T_r and 90% to 10% is T_d .

Note(4) Backlight circuit



$$I_F = 60\text{mA} \quad V_f = 3.2\text{V}$$

9. Inspection Standards

1. AQL(Acceptable Quality Level)

AQL of major and minor defect

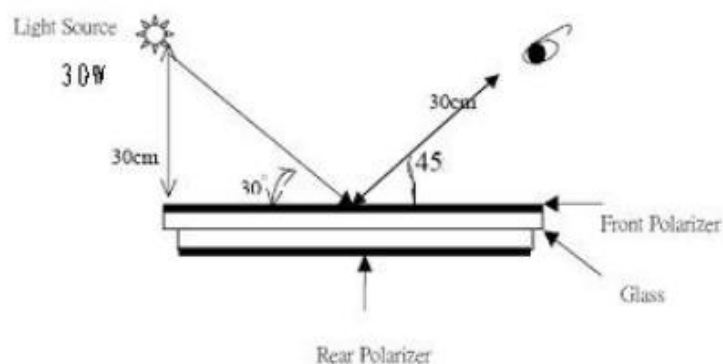
According to GB/T 2828-2003 ; , normal inspection, Class II

MAJOR DEFECT	MINOR DEFECT
0.65	1.5

2. Basic conditions for inspection

The LCM face to us, in normal environment, About an angle of incidence 30°, a distance of 30cm with normal eye, with an angle of 45 degree to check the products without uncovering the film!

(As shown below)

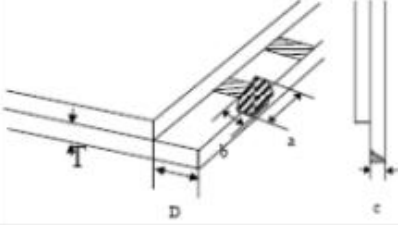
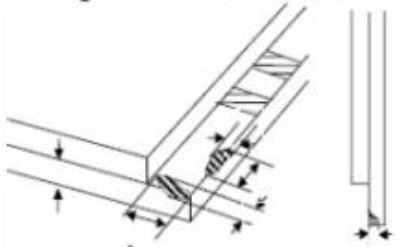


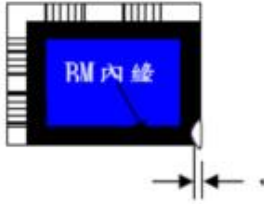
3. Inspection item and criteria

3.1 Visual inspection criterion in immobility

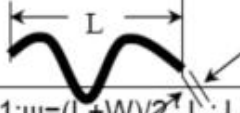
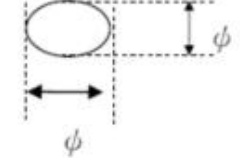
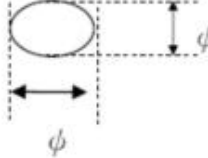
3.1.1 Glass defect

No	Defect item	Criteria	Remark
1	Dimension Unconformity (Major defect)	By Engineering Drawing	

No	Defect item	Criteria	Remark
2	Cracks (Major defect)	1.Linear cracks on panel 【 Reject】 2. Nonlinear crack contrast by limited sample	
3	Glass extrude the conductive area (minor defect)	a: disregards and no influence assemblage 1) $b \leq 1/3$ Pin width(non bonding area) 【 Accept】 2) bonding area $\leq 0.5\text{mm}$ 【 Accept】	a:Length, b:Width
4	Pin-side , conductive area damaged (minor defect)	(a c : disregards) $b \leq 1/3$ of effective length for bonding electrode 【 Accept】	a:Length·b:Width·c:Thickness 
5	Pin-side , non-conductive area damaged (minor defect)	1) Damage area don't touch the ITO (Incluing contraposition mark,except scribing mark) 【 Accept】 2) $c < T$ $b \leq BM$ 1/3 of width 【 Accept】 3) $c = T$ b not touch the seal glue 【 Accept】 4) a disregards	a:Length·b:Width·c:Thickness 

No	Defect item	Criteria	Remark
6	Non-pin-side damage (minor defect)	$c < T$	c : Thickness b : width of damage 
		1) b exceeds 1/3 BM	
		【Reject】	
		$c = T$ b not touch the seal glue 【Reject】	

3.1.2 LCD appearance defect (View area)

No	Defect item	Criteria		Remark
1	Fiber 、glass cratch 、polarizer scratch/folded (minor defect)	Specification	Allowable	note1: L : Length , W : Width note2: disregard if out of AA 
		$0.05\text{mm} < W \leq 0.1\text{mm};$ $L \leq 3.0\text{mm}$	1	
		$W > 0.1\text{mm}; L > 3.0\text{mm}$	0	
2	Polarizer bubble 、 concave and convex (minor defect)	$\psi \leq 0.2\text{mm}$	disregard	note 1: $\psi = (L+W)/2$; L : Length , W : Width note2: disregard if out of AA 
		$0.2\text{mm} < \psi \leq 0.3\text{mm}$	2	
		$0.3\text{mm} < \psi \leq 0.5\text{mm}$	1	
		$0.5\text{mm} < \psi$	0	
3	Black dots 、dirty dots 、 impurities 、eyewinker (Major defect)	$\psi \leq 0.15\text{mm}$	disregard	note2: disregard if out of AA 
		$0.15\text{mm} < \psi \leq 0.25\text{mm}$	2	
		$0.25\text{mm} < \psi \leq 0.3\text{mm}$	1	
		$0.3\text{mm} < \psi$	0	
4	Polarizer prick (Major defect)	$\psi \leq 0.1\text{mm}$	disregard	note1: $\psi = (L+W)/2$; L = Length , W = Width note2: the distance between two dots $> 5\text{mm}$
		$0.1\text{mm} < \psi \leq 0.25\text{mm}$	3	
		$\psi > 0.25\text{mm}$	0	

3.1.3 .FPC

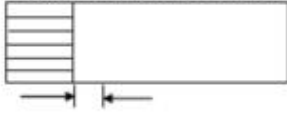
No	Defect item	Criteria		Remark
1	Copper screen peel (Major defect)	Copper screen peel 【 Reject】		
2	No release tape or peel (Major defect)	No release tape or peel 【 Reject】		
3	Dirty dot and impurity of FPC for customer using side (minor defect)	Specification	Allowable	note1: Cannot have stride ITO impurities
		$\psi \leq 0.25\text{mm}$	2	
		$\psi > 0.25$	0	

3.1.4 Black tape & Mara tape

1	FPC or H/S black tape shift (minor defect)	1.shift spec: 1)glue to the polarize 【 Reject】 2) IC bare 【 Reject】 2. left-and-right spec: 1) exceed of FPC edge or H-S edge 【 Reject】 2)IC bare 【 Reject】	
2	No black tape (Major defect)	No black tape 【 Reject】	
3	Tape position mistake (minor defect)	Not by engineering drawing 【 Reject】	
4	Mara tape defect (minor defect)	Peel before pulling the protecting film. 【 Reject】	

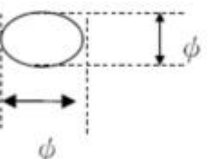
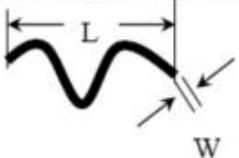
3.1.5 Silicon and Tuffy glue

No	Defect item	Criteria	Remark
1	Quantity of silicon (minor defect)	Uncover the ITO and circuit area. 【 Reject】	note: compared by engineering drawing.

No	Defect item	Criteria	Remark
2	Tuffy glue (minor defect)	1. Uncover the reveal copper area 【Reject】 2. Cover layer 0.3mm(Min) ~ 3.0mm(Max) 【accept】	note:if customer has special requirement , refer to the technical document. 
3	Depth of glue covering (minor defect)	Depth of glue covering overtop front Polarizer 【Reject】	Except of the special requirement .

3.2 Electrical criteria

No	Defect item	Criteria	Remark
1	No display (Major defect)	No display 【Reject】	
2	Missing line (Major defect)	Missing line 【Reject】	
3	Seg-com light and dark (Major defect)	Seg-com light and dark 【Reject】	ND filter 2% test
4	No display in immobility (Major defect)	No display in immobility 【Reject】	
5	Flicker of Pattern (Major defect)	Flicker of Pattern 【Reject】	
6	Mura (Major defect)	ND filter 2% test	
7	Over current (Major defect)	Over current 【Reject】	
8	Voltage out of specification (Major defect)	Voltage out of specification 【Reject】	
9	Pattern blur ,error code (Major defect)	Pattern blur ,error code 【Reject】	
10	Dark light, Flicker (Major defect)	Dark light, Flicker 【Reject】	

No	Defect item	Criteria	Remark	
11	Black/White dots · Dirty dots · eyewinker (Major defect)	Specification	Allowable	Note1: disregard if out of AA 
		$\psi \leq 0.15\text{mm}$	disregard	
		$0.15\text{mm} < \psi \leq 0.25\text{mm}$	2	
		$0.25\text{mm} < \psi \leq 0.3\text{mm}$	1	
		$0.3\text{mm} < \psi$	0	
12	Fiber · glass cratch · polarizer scratch/folded (minor defect)	$W \leq 0.03\text{mm}$	disregard	note1: L : Length · W : Width note2: disregard if out of AA 
		$0.03\text{mm} < W \leq 0.05\text{mm} ;$ $L \leq 3.0\text{mm}$	2	
		$0.05\text{mm} < W \leq 0.1\text{mm} ;$ $L \leq 3.0\text{mm}$	1	
		$W > 0.1\text{mm} ; L > 3.0\text{mm}$	0	

10.Records Of Version

Version	Revise Date	Page	Content
00	2025-6-18	ALL	New released