PRODUCT SPECIFICATION FOR LCD MODULE

Revision: 1.0

Model No: LS024T32-M-V1

Module Type: COG+FPC+B/L

APPROVED SIGNATURE

■ Approved Product Specification only

□ Approved Product Specification and Samples

Prepared By	Checked By	Approved By

Contents

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1. General Description

LS024T32-M-V1 is a transmissive type a-Si TFT-LCD (amorphous silicon thin film transistor liquid crystal display) module, which is composed of a TFT-LCD panel, a driver circuit and a backlight unit. The panel size is 2.4 inch and the resolution is 240(RGB)*320, the panel can display up to 262k colors.

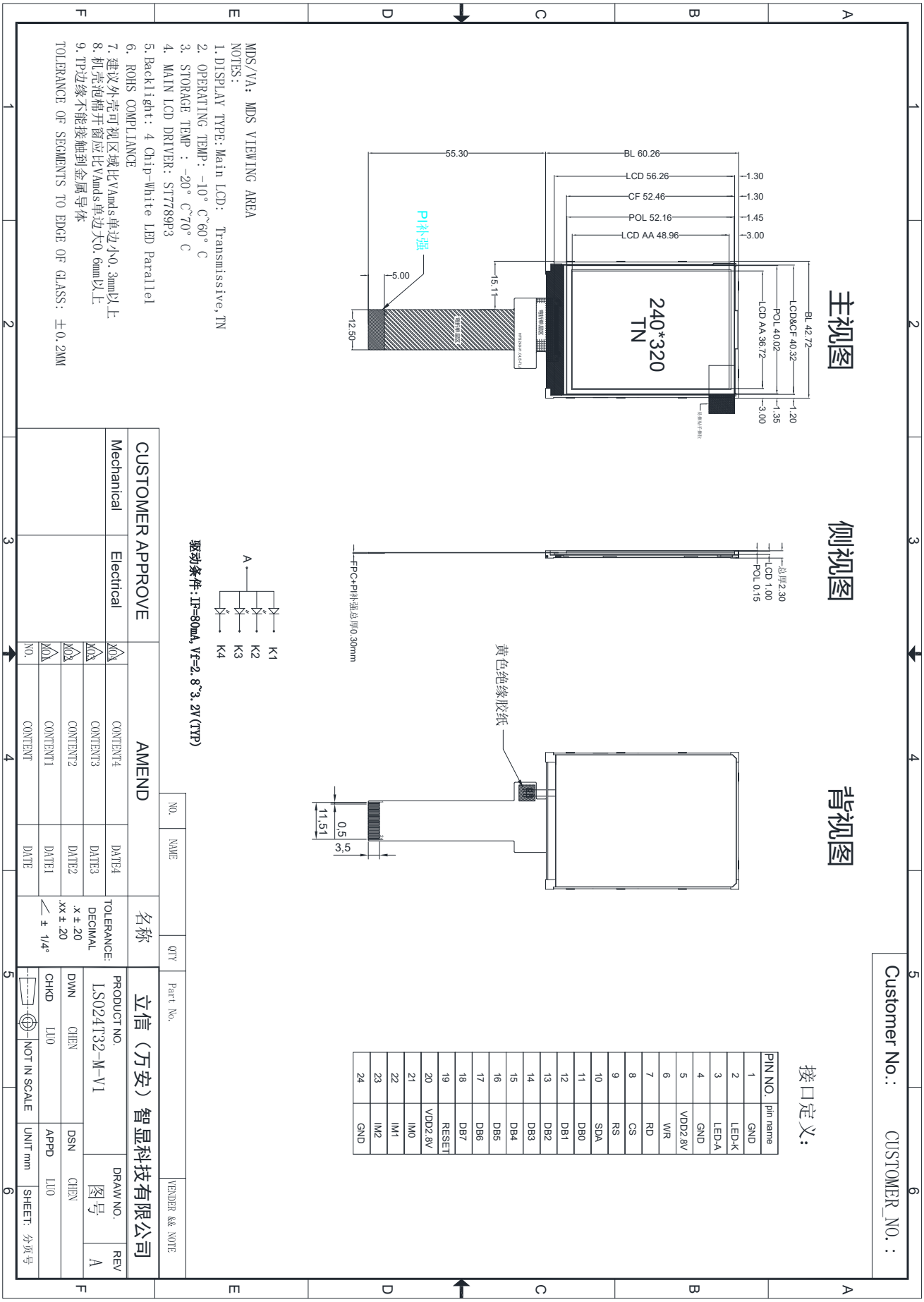
2. Physical Features

Display Mode	TFT-LCD Module
	Active matrix TFT, Transmissive type
Display Format	Graphic 240(RGB)×320 Dot-matrix
Input Data	8bit 8080 /SPI
Viewing Direction （Grayscale Inversion）	TN
Drive	ST7789P3

3. Mechanical Specification

Item	Specification	Unit
Module size (H×V×D)	42.72 ×60.26 ×2.3	mm
Number of dots	240(RGB) ×320	pixel
Active area (H×V)	36.72×48.96	mm

4. Outline Dimension



5. Absolute Maximum Ratings

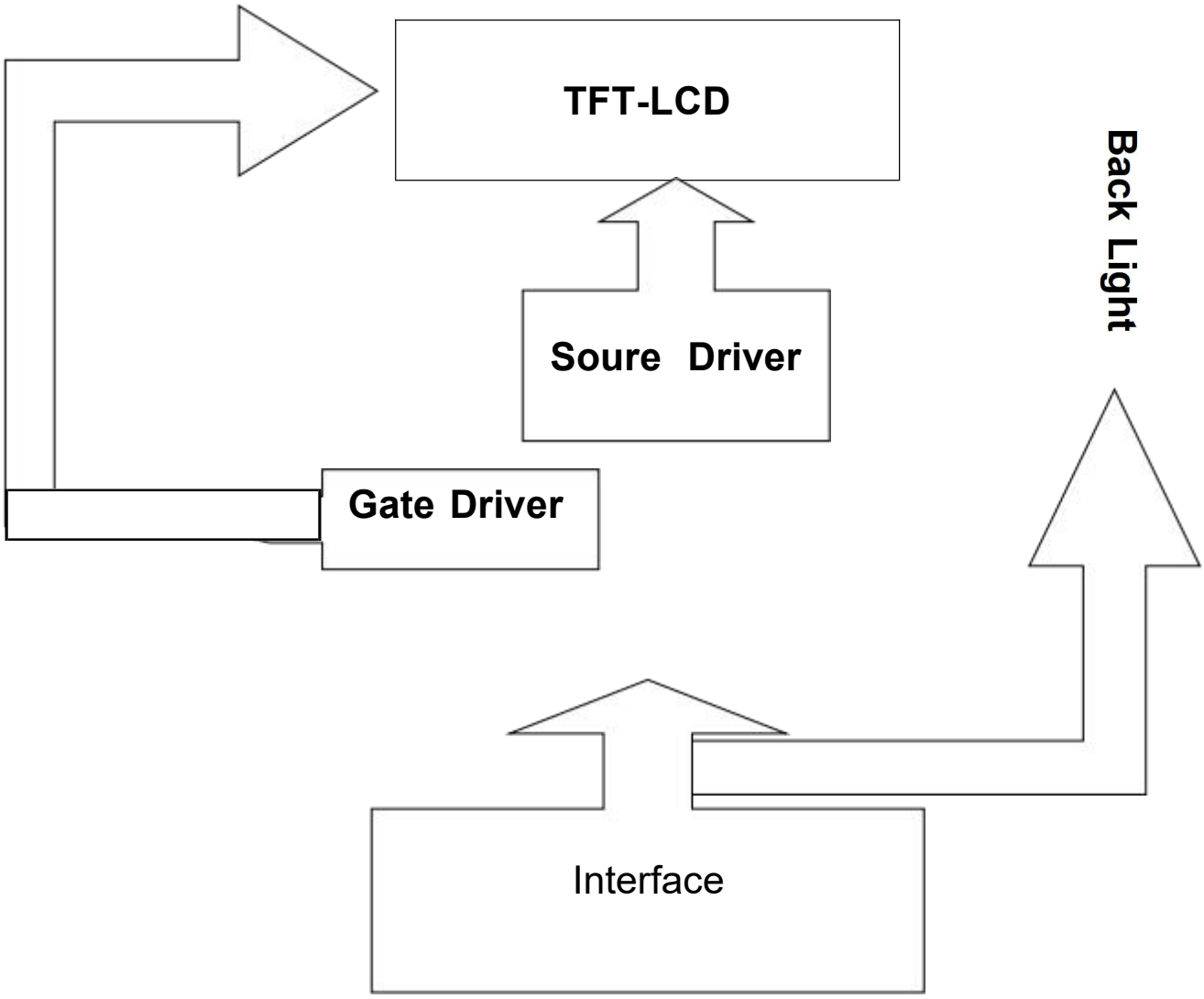
Item	Symbol	Min	Max	Unit	Remark
Supply voltage	VDD	-0.3	4.6	V	Note1 Note2
Operating temperature	TOPR	-20	70	℃	
Storage temperature	TSTR	-30	80	℃	

6. Electrical Characteristics

Item		Symbol	Rating			Unit	Remark
			Min	Typ	Max		
Supply voltage		VDD	2.4	2.8	3.3	V	Note1
Input Voltage	L level	VIL	0	---	0.3*IOVCC	V	
	H level	VIH	0.7*IOVCC	---	IOVCC	V	

7. Module Function Description

7-1. Block Diagram Of LCM



7-2. Pin Description

PIN NO.	Symbol	I/O	Description
1	GND		Ground
2	LEDK		Power for LED backlight cathode
3	LEDA		Power for LED backlight anode
4	GND		Ground
5	VDD2.8V		Power Supply
6	WR		Write enable in MCU parallel interface. - Display data/command selection pin in 4-line serial interface. - Second Data lane in 2 data lane serial interface. -If not used, please fix this pin at VDDI or DGND.
7	RD		Read enable in 8080 MCU parallel interface. -If not used, please fix this pin at VDDI or DGND.
8	CS		Chip selection pin . Low enable. High disable
9	RS		-Display data/command selection pin in parallel interface. -This pin is used to be serial interface clock.(SCL) DCX='1': display data or parameter. DCX='0': command data. -If not used, please fix this pin at VDDI or DGND.
10	SDA		-When IM3: Low, SPI interface input/output pin. -When IM3: High, SPI interface input pin. -The data is latched on the rising edge of the SCL signal. -If not used, please fix this pin at VDDI or DGND level.
11	DB0		parallel interface data bus
12	DB1		parallel interface data bus
13	DB2		parallel interface data bus
14	DB3		parallel interface data bus
15	DB4		parallel interface data bus
16	DB5		parallel interface data bus
17	DB6		parallel interface data bus
18	DB7		parallel interface data bus
19	RESET		This signal will reset the device and it must be applied to properly initialize the chip.

<table>
<tr><td>20</td><td>VDD2.8V</td><td></td><td>Power Supply</td></tr>
<tr><td>21</td><td>IM0</td><td></td><td rowspan="3"><table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>MPU Interface Mode</th><th>Data pin</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>80-8bit parallel I/F</td><td>DB[7:0]</td></tr>
<tr><td colspan="6"></td></tr>
<tr><td rowspan="2">0</td><td rowspan="2">1</td><td rowspan="2">0</td><td rowspan="2">1</td><td>3-line 9bit serial I/F</td><td>SDA: in/out</td></tr>
<tr><td>2 data lane serial I/F</td><td>SDA: in/out
WRX: in</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>4-line 8bit serial I/F</td><td>SDA: in/out</td></tr>
</table></td></tr>
<tr><td>22</td><td>IM1</td><td></td></tr>
<tr><td>23</td><td>IM2</td><td></td></tr>
<tr><td>24</td><td>GND</td><td></td><td>Ground</td></tr>
</table>

7-3 Timing Characteristics

7.4.1 8080 Series MCU Parallel Interface Characteristics: 9/8-bit Bus

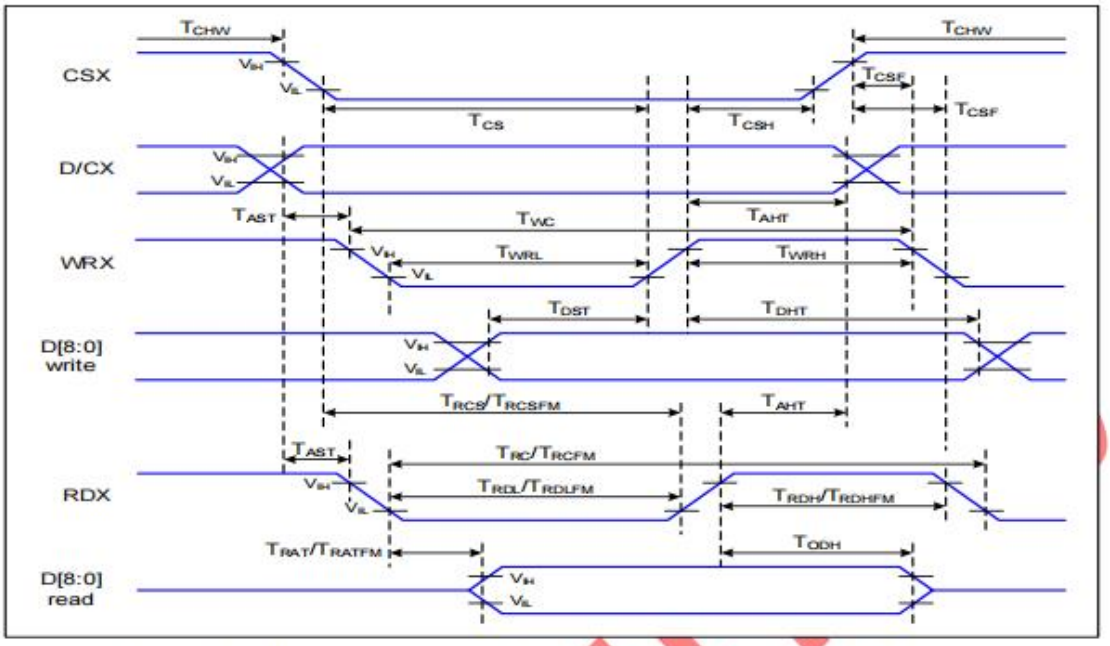


Figure 1 Parallel Interface Timing Characteristics (8080-Series MCU Interface)

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T_{AST}	Address setup time	TBD	-	ns	-
	T_{AHT}	Address hold time (Write/Read)	TBD	-	ns	
CSX	T_{CHW}	Chip select "H" pulse width	TBD	-	ns	-
	T_{CS}	Chip select setup time (Write)	TBD	-	ns	
	T_{RCS}	Chip select setup time (Read ID)	TBD	-	ns	
	T_{RCSFM}	Chip select setup time (Read FM)	TBD	-	ns	
	T_{CSF}	Chip select wait time (Write/Read)	TBD	-	ns	
	T_{CSH}	Chip select hold time	TBD	-	ns	
WRX	T_{WC}	Write cycle	TBD	-	ns	
	T_{WRH}	Control pulse "H" duration	TBD	-	ns	
	T_{WRL}	Control pulse "L" duration	TBD	-	ns	
RDX (ID)	T_{RC}	Read cycle (ID)	TBD	-	ns	When read ID data
	T_{RDH}	Control pulse "H" duration (ID)	TBD	-	ns	
	T_{RDL}	Control pulse "L" duration (ID)	TBD	-	ns	
RDX (FM)	T_{RCFM}	Read cycle (FM)	TBD	-	ns	When read from frame memory
	T_{RDHFM}	Control pulse "H" duration (FM)	TBD	-	ns	
	T_{RDLFM}	Control pulse "L" duration (FM)	TBD	-	ns	
D[8:0]	T_{DST}	Data setup time	TBD	-	ns	For CL=30pF

	T_{DHT}	Data hold time	TBD	-	ns	
	T_{RAT}	Read access time (ID)	-	TB-D	ns	
	T_{RATFM}	Read access time (FM)	-	TBD	ns	
	T_{ODH}	Output disable time	TBD	TBD	ns	

Table 4 8080 Parallel Interface Characteristics

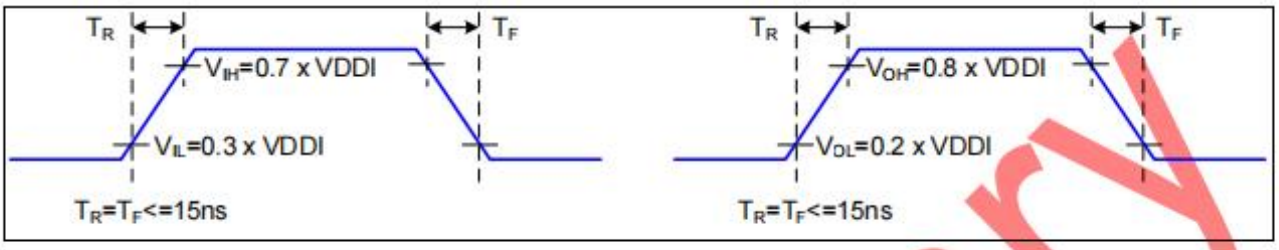


Figure 2 Rising and Falling Timing for I/O Signal

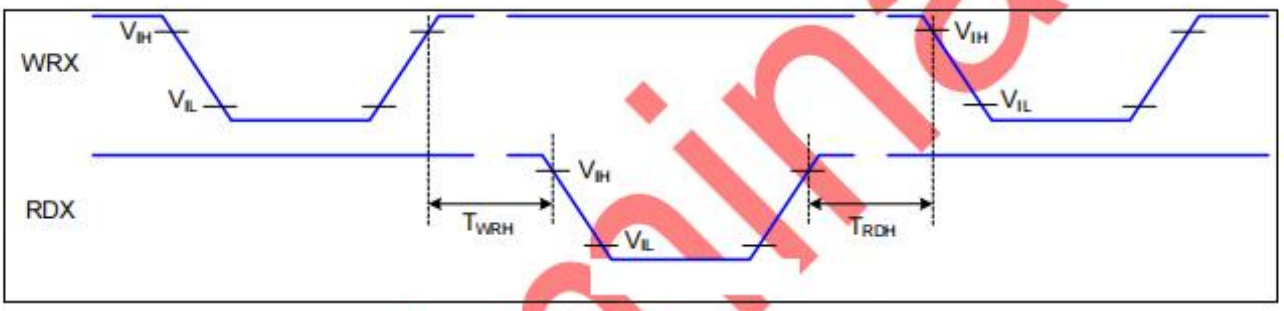


Figure 3 Write-to-Read and Read-to-Write Timing

Note: The rising time and falling time (Tr, Tf) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

7.4.2 Serial Interface Characteristics (3-line serial):

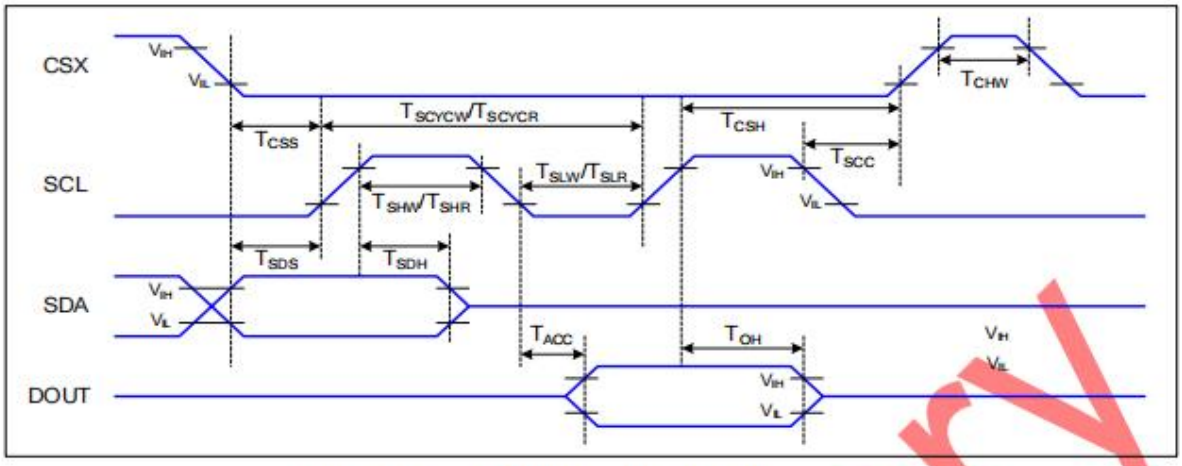


Figure 4 3-line serial Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	TBD	-	ns	
	T_{CSH}	Chip select hold time (write)	TBD	-	ns	
	T_{CSS}	Chip select setup time (read)	TBD	-	ns	
	T_{SCC}	Chip select hold time (read)	TBD	-	ns	
	T_{CHW}	Chip select "H" pulse width	TBD	-	ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	TBD	-	ns	
	T_{SHW}	SCL "H" pulse width (Write)	TBD	-	ns	
	T_{SLW}	SCL "L" pulse width (Write)	TBD	-	ns	
	T_{SCYCR}	Serial clock cycle (Read)	TBD	-	ns	
	T_{SHR}	SCL "H" pulse width (Read)	TBD	-	ns	
	T_{SLR}	SCL "L" pulse width (Read)	TBD	-	ns	
SDA (DIN)	T_{SDS}	Data setup time	TBD	-	ns	
	T_{SDH}	Data hold time	TBD	-	ns	
DOUT	T_{ACC}	Access time	TBD	TBD	ns	For maximum CL=30pF
	T_{OH}	Output disable time	TBD	TBD	ns	For minimum CL=8pF

Table 5 3-line serial Interface Characteristics

Note1 : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Note2 : In the read sequence of Serial interface, the 500nsec delay time is needed between read command and first read clock.

7.4.3 Serial Interface Characteristics (4-line serial):

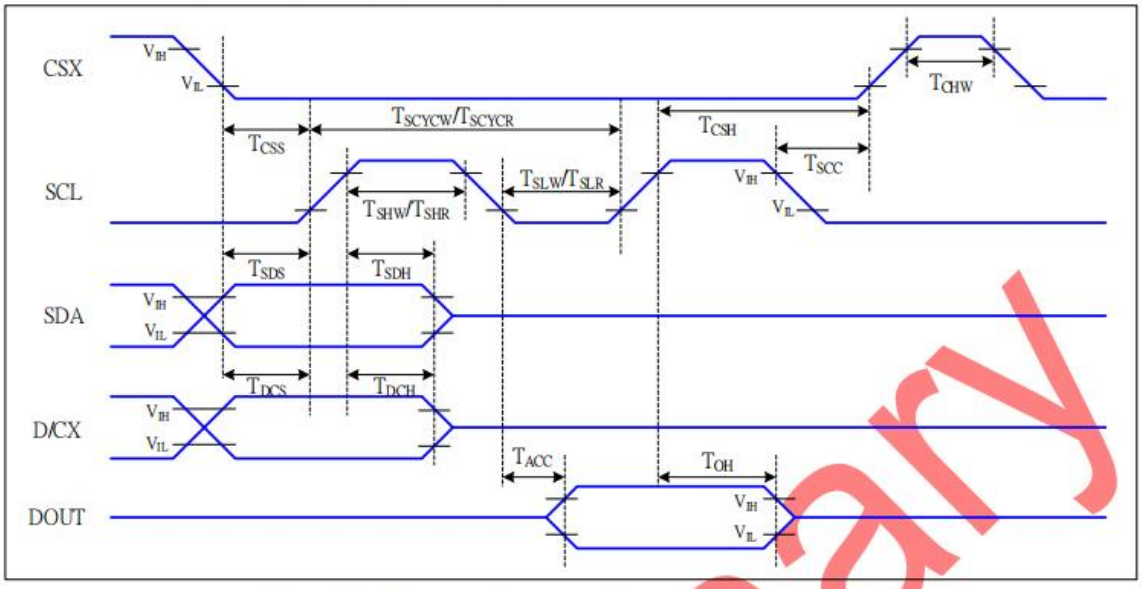


Figure 5 4-line serial Interface Timing Characteristics

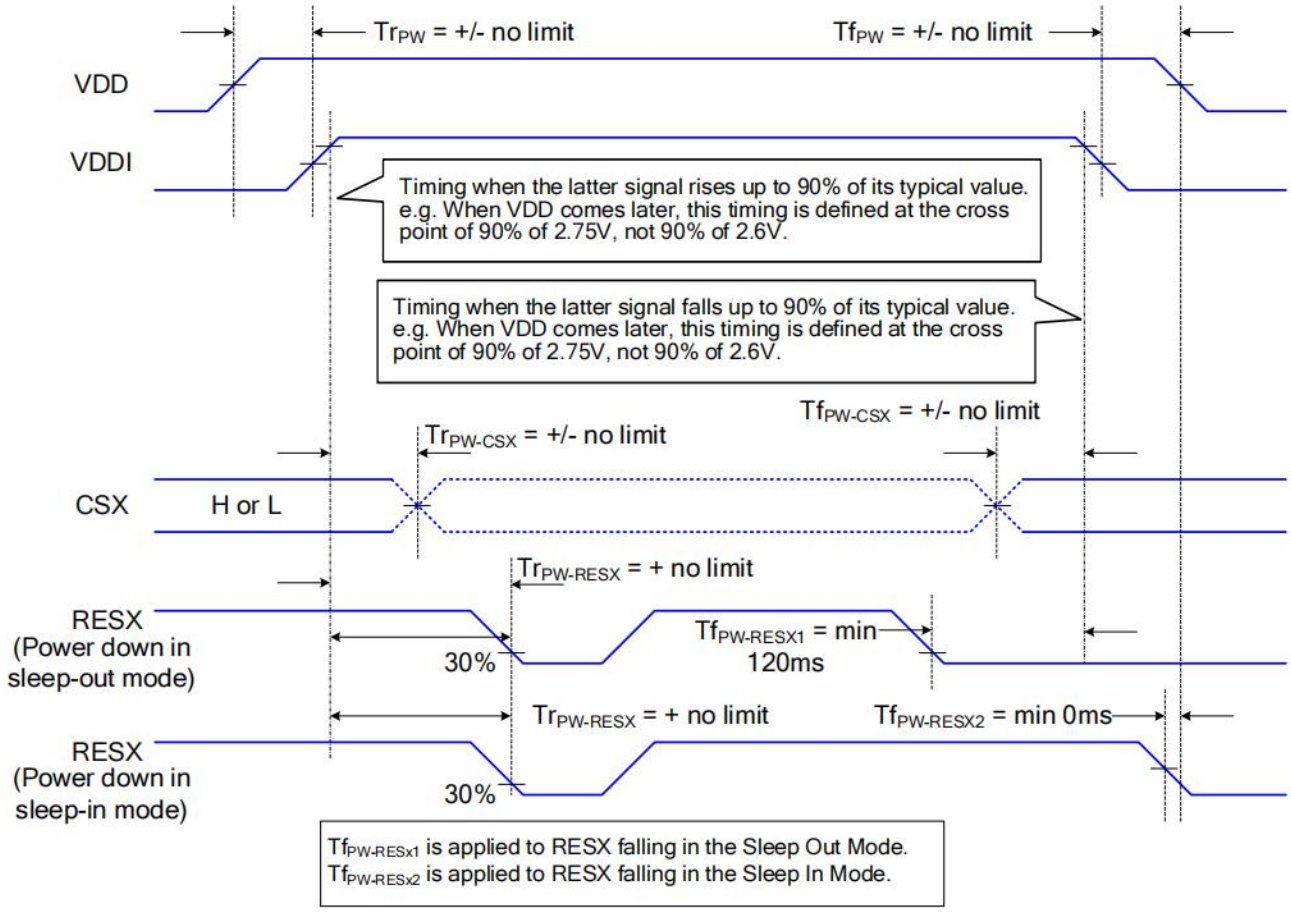
VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	TBD	-	ns	
	T_{CSH}	Chip select hold time (write)	TBD	-	ns	
	T_{CSS}	Chip select setup time (read)	TBD	-	ns	
	T_{SCC}	Chip select hold time (read)	TBD	-	ns	
	T_{CHW}	Chip select “H” pulse width	TBD	-	ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	TBD	-	ns	-write command & data ram
	T_{SHW}	SCL “H” pulse width (Write)	TBD	-	ns	
	T_{SLW}	SCL “L” pulse width (Write)	TBD	-	ns	
	T_{SCYCR}	Serial clock cycle (Read)	TBD	-	ns	-read command & data ram
	T_{SHR}	SCL “H” pulse width (Read)	TBD	-	ns	
	T_{SLR}	SCL “L” pulse width (Read)	TBD	-	ns	
D/CX	T_{DCS}	D/CX setup time	TBD	-	ns	
	T_{DCH}	D/CX hold time	TBD	-	ns	
SDA (DIN)	T_{SDS}	Data setup time	TBD	-	ns	
	T_{SDH}	Data hold time	TBD	-	ns	
DOUT	T_{ACC}	Access time	TBD	TBD	ns	For maximum CL=30pF
	T_{OH}	Output disable time	TBD	TBD	ns	For minimum CL=8pF

Table 6 4-line serial Interface Characteristics

Note1 : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

The power on/off sequence is illustrated below



8. Electro-Optical Characteristics

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time		Tr +Tf	θx = θy =0	---	30	---	ms	Note 1
Contrast Ratio		CR		---	250	---	---	Note 2
Transmittance		T%		4	4.7	---	%	
Color Chromaticity (CIE1931)	White	W x	θx = θy =0	---	0.308	---	---	
		W y		---	0.325	---	---	
Viewing angle	θ_T		CR > 10	---	45	---	Deg.	Note 3
	θ_B			---	20	---		
	θ_L			---	45	---		
	θ_R			---	45	---		

Note 1: Ambient temperature = 25°C.

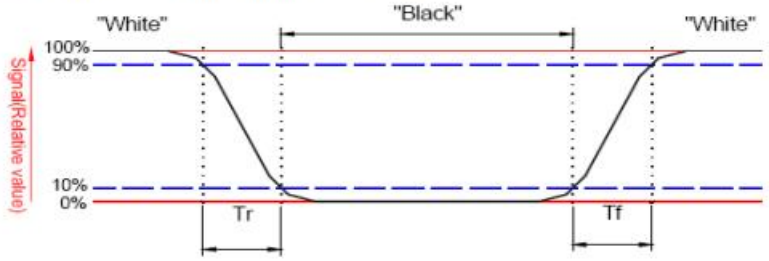
Note 2: To be measured with a viewing cone of 2°by Topcon luminance meter BM-5A.

Note 3: To be measured with Otsuta chromaticity meter LCF-2100M，CF only measure under C light simulation.

Note 4: CTC shipping status is cell without polarizer. Transmittance of Specification is cell with polarizer

Note 5: Definition of response time:

The output signals of TRD-100 are measured when the input signals are changed to "White" (falling time) and from "White" to "Black" (rising time), respectively. The interval is between the 10% and 90% of amplitudes. Refer to figure as below.

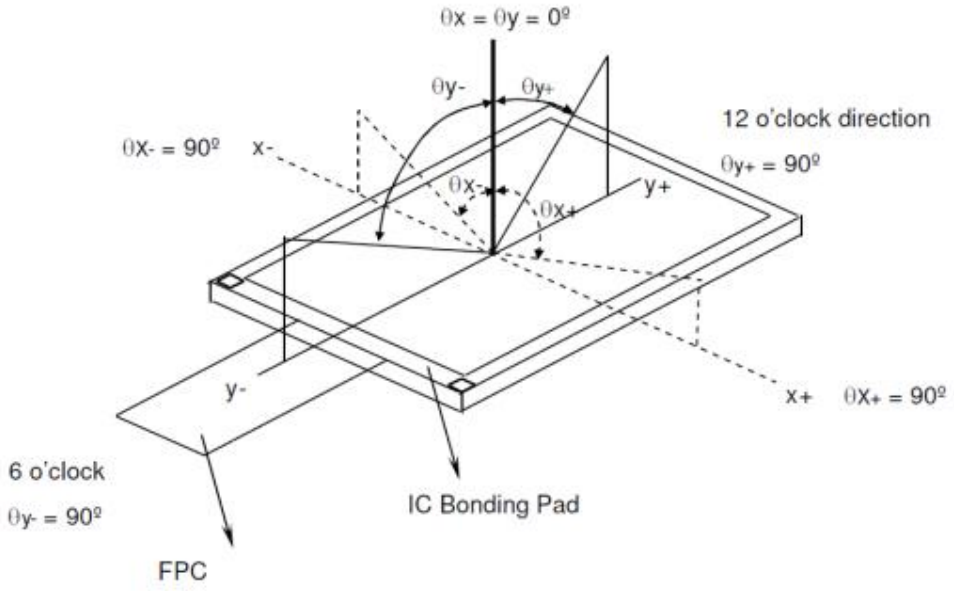


Note 6: Definition of contrast ratio:

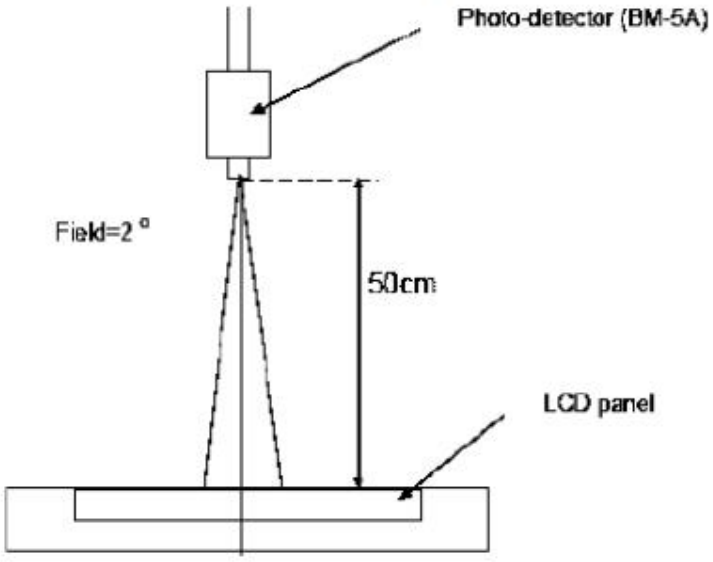
Contrast ratio is calculated by the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "white" state}}{\text{Brightness on the "black" state}}$$

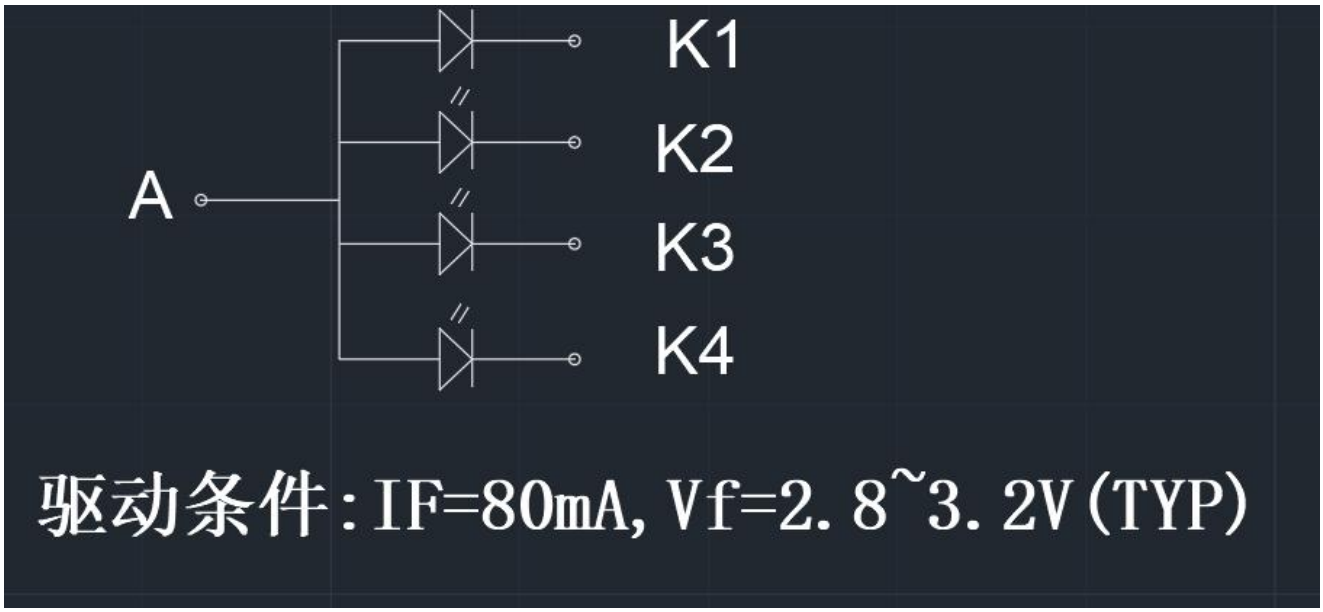
Note 7: Definition of viewing angle



Note 8: Optical characteristic measurement setup.



Note(4) Backlight circuit



9.Inspection Standards

1. AQL(Acceptable Quality Level)

AQL of major and minor defect

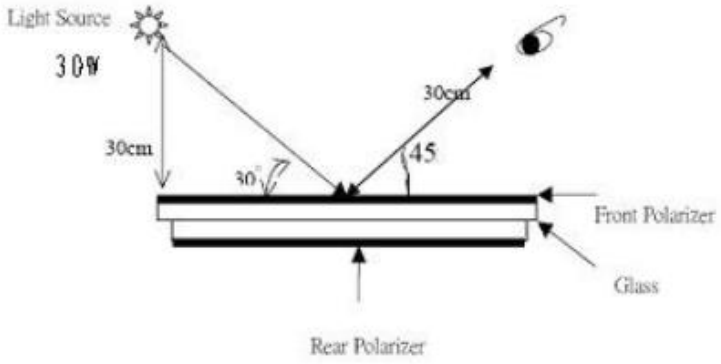
According to GB/T 2828-2003 ; , normal inspection, Class II

MAJOR DEFECT	MINORDEFECT
0.65	1.5

2. Basic conditions for inspection

The LCM face to us, in normal environment, About an angle of incidence 30, a distance of 30cm with normal eye,with an angle of 45 degree to check the products without uncovering the film!

(As shown below)

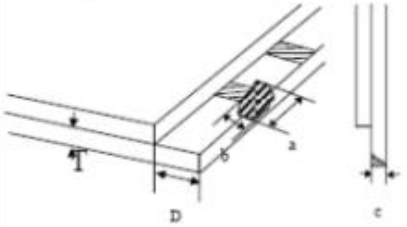
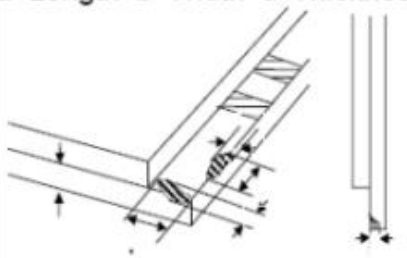


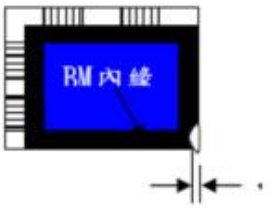
3. Inspection item and criteria

3.1 Visual inspection criterion in immobility

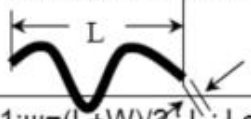
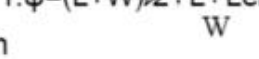
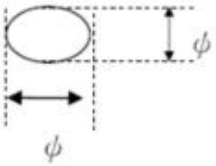
3.1.1 Glass defect

No	Defect item	Criteria	Remark
1	Dimension Unconformity (Major defect)	By Engineering Drawing	

No	Defect item	Criteria	Remark
2	Cracks (Major defect)	1.Linear cracks on panel 【Reject】 2. Nonlinear crack contrast by limited sample	
3	Glass extrude the conductive area (minor defect)	a: disregards and no influence assemblage 1) b≦1/3Pin width(non bonding area) 【Accept】 2) bonding area≦0.5mm 【Accept】	a:Length, b:Width
4	Pin-side，conductive area damaged (minor defect)	(a c：disregards) b≦ 1/3 of effective length for bonding electrode 【Accept】	a：Length，b：Width，c：Thickness 
5	Pin-side，non-conductive area damaged (minor defect)	1) Damage area don't touch the ITO (Inclueling contraposition mark,except scribing mark) 【Accept】 2) c<T b≦BM 1/3 of width 【Accept】 3) c=T b not touch the seal glue 【Accept】 4) a disregards	a：Length，b：Width，c：Thickness 

No	Defect item	Criteria	Remark
6	Non-pin-side damage (minor defect)	c<T 1) b exceeds 1/3 BM 【Reject】 c=T b not touch the seal glue 【Reject】	c : Thickness b: width of damage 

3.1.2 LCD appearance defect (View area)

No	Defect item	Criteria		Remark
1	Fiber、glass cratch、polarizer scratch/folded (minor defect)	Specification	Allowable	note1: L：Length、W：Width note2: disregard if out of AA 
		0.05mm<W≦0.1mm; L≦3.0mm	1	
		W>0.1mm ; L>3.0mm	0	
2	Polarizer bubble、concave and convex (minor defect)	ψ≦0.2mm	disregard	note 1:ψ=(L+W)/2；L：Length、W：Width note2: disregard if out of AA 
		0.2mm<ψ ≦ 0.3mm	2	
		0.3mm<ψ ≦ 0.5mm	1	
		0.5mm<ψ	0	
3	Black dots、dirty dots、impurities、eyewinker (Major defect)	ψ≦0.15mm	disregard	note2: disregard if out of AA 
		0.15mm<ψ ≦ 0.25mm	2	
		0.25mm<ψ ≦ 0.3mm	1	
		0.3mm<ψ	0	
4	Polarizer prick (Major defect)	ψ≦0.1mm	disregard	note1:ψ=(L+W)/2 ：L= Length、W=Width note2: the distance between two dots >5mm
		0.1mm<ψ≦0.25mm	3	
		ψ>0.25mm	0	

3.1.3 .FPC

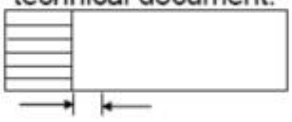
No	Defect item	Criteria		Remark
1	Copper screen peel (Major defect)	Copper screen peel 【Reject】		
2	No release tape or peel (Major defect)	No release tape or peel 【Reject】		
3	Dirty dot and impurity of FPC for customer using side (minor defect)	Specification	Allowable	note1: Cannot have stride ITO impurities
		ψ≤0.25mm	2	
		ψ>0.25	0	

3.1.4 Black tape & Mara tape

1	FPC or H/S black tape shift (minor defect)	1.shift spec: 1)glue to the polarize 【Reject】 2) IC bare 【Reject】 2. left-and-right spec: 1) exceed of FPC edge or H-S edge 【Reject】 2)IC bare 【Reject】	
2	No black tape (Major defect)	No black tape 【Reject】	
3	Tape position mistake (minor defect)	Not by engineering drawing 【Reject】	
4	Mara tape defect (minor defect)	Peel before pulling the protecting film. 【Reject】	

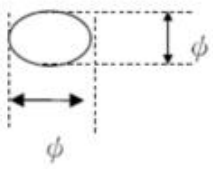
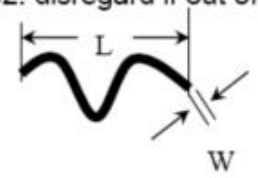
3.1.5 Silicon and Tuffy glue

No	Defect item	Criteria	Remark
1	Quantity of silicon (minor defect)	Uncover the ITO and circuit area. 【Reject】	note: compared by engineering drawing.

No	Defect item	Criteria	Remark
2	Tuffy glue (minor defect)	1. Uncover the reveal copper area 【Reject】 2. Cover layer 0.3mm(Min) ~ 3.0mm(Max) 【accept】	note:if customer has special requirement , refer to the technical document. 
3	Depth of glue covering (minor defect)	Depth of glue covering overtop front Polarizer 【Reject】	Except of the special requirement。

3.2 Electrical criteria

No	Defect item	Criteria	Remark
1	No display (Major defect)	No display 【Reject】	
2	Missing line (Major defect)	Missing line 【Reject】	
3	Seg-com light and dark (Major defect)	Seg-com light and dark 【Reject】	ND filter 2% test
4	No display in immobility (Major defect)	No display in immobility 【Reject】	
5	Flicker of Pattern (Major defect)	Flicker of Pattern 【Reject】	
6	Mura (Major defect)	ND filter 2% test	
7	Over current (Major defect)	Over current 【Reject】	
8	Voltage out of specification (Major defect)	Voltage out of specification 【Reject】	
9	Pattern blur ,error code (Major defect)	Pattern blur ,error code 【Reject】	
10	Dark light, Flicker (Major defect)	Dark light, Flicker 【Reject】	

No	Defect item	Criteria	Remark	
11	Black/White dots、Dirty dots、eyewinker (Major defect)	Specification	Allowable	Note1: disregard if out of AA 
		ψ≦0.15mm	disregard	
		0.15mm<ψ≦0.25mm	2	
		0.25mm<ψ≦0.3mm	1	
		0.3mm<ψ	0	
12	Fiber、glass cratch、polarizer scratch/folded (minor defect)	W≦0.03mm	disregard	note1: L : Length、W : Width note2: disregard if out of AA 
		0.03mm<W≦0.05mm ; L≦3.0mm	2	
		0.05mm<W≦0.1mm; L≦3.0mm	1	
		W>0.1mm ; L>3.0mm	0	

10.Records Of Version

Version	Revise Date	Page	Content
00	2024-3-30	ALL	New released