

PRODUCT SPECIFICATION **FOR LCD MODULE**

Revision: 1.0

Model No: LSC035I19-R-V1

Module Type: COG+FPC+B/L+CTP

APPROVED SIGNATURE

- ☒ Approved Product Specification only
- ☐ Approved Product Specification and Samples

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1. General Description

LSC035I19-R-V1 is a transmissive type a-Si TFT-LCD (amorphous silicon thin film transistor liquid crystal display) module, which is composed of a TFT-LCD panel, a driver circuit and a backlight unit. The panel size is 3.5 inch and the resolution is 320(RGB)*480, the panel can display up to 16.7 M colors.

2. Physical Features

Display Mode	TFT-LCD Module
	Active matrix TFT, Transmissive type
Display Format	Graphic 320(RGB)×480 Dot-matrix
Input Data	RGB
Viewing Direction (Grayscale Inversion)	Free (IPS)
Drive	ST7365P

3. Mechanical Specification

Item	Specification	Unit
Module size (H×V×D)	56.0 ×87.9×3.7	mm
Number of dots	320(RGB) ×480	pixel
Active area (H×V)	48.96×73.44	mm



5. Absolute Maximum Ratings

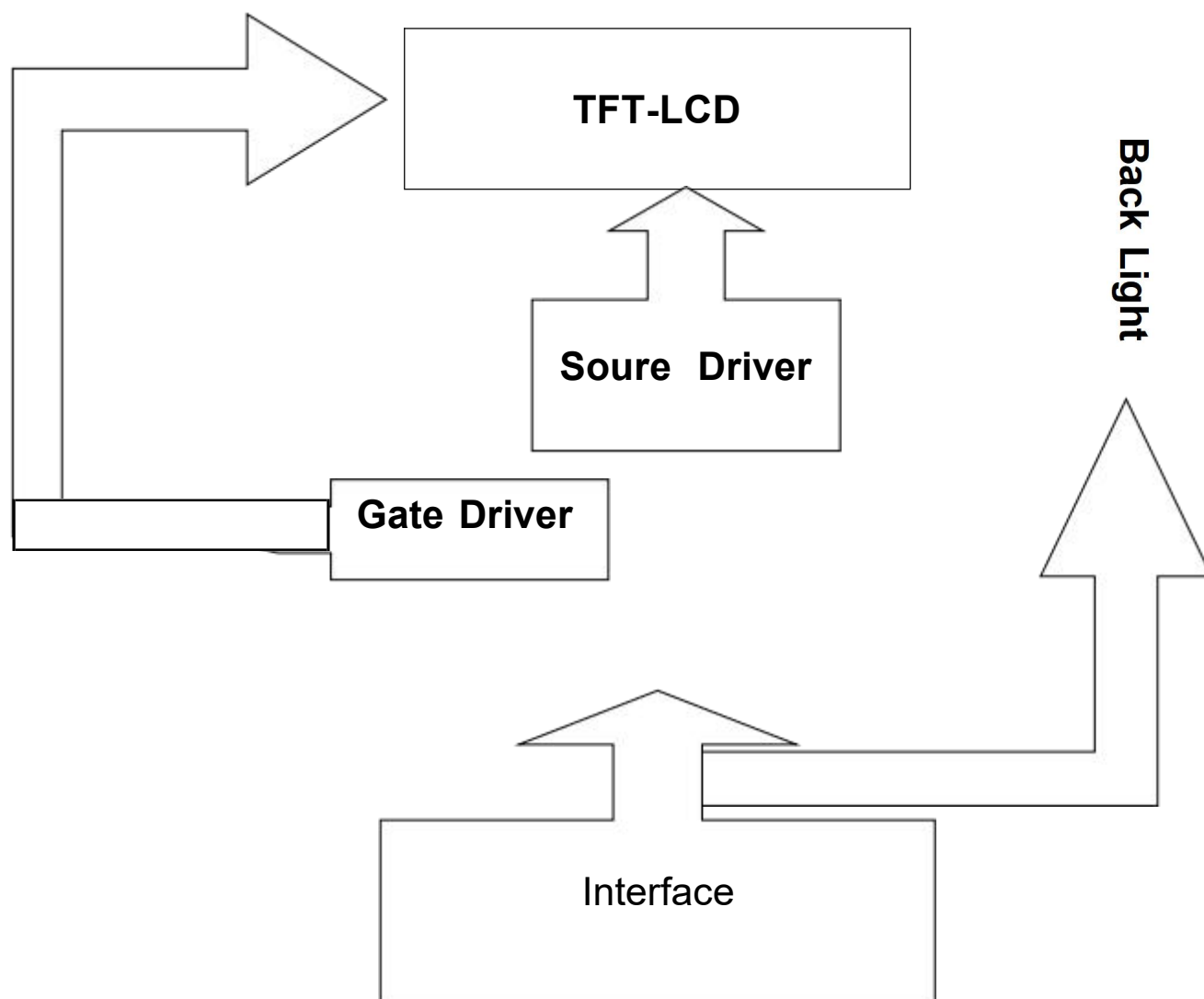
Item	Symbol	Min	Max	Unit	Remark
Supply voltage	VCC	-0.3	4.6	V	Note1 Note2
Supply voltage	IOVCC	-0.3	4.0	V	
Operating temperature	TOPR	-20	70	°C	
Storage temperature	TSTR	-30	80	°C	

6. Electrical Characteristics

Item		Symbol	Rating			Unit	Remark
			Min	Typ	Max		
Supply voltage		VCC	2.4	2.8	3.3	V	Note1
Supply voltage		IOVCC	1.65	1.8	3.3	V	
Input Voltage	L level	VIL	0	---	0.3*IOVCC	V	
	H level	VIH	0.7*VCC	---	IOVCC	V	

7. Module Function Description

7-1. Block Diagram Of LCM



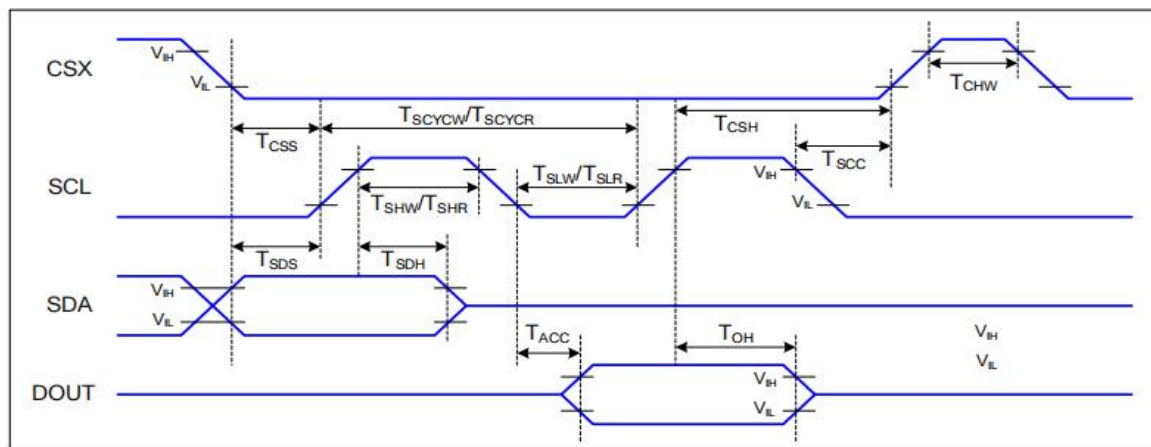
7-2. Pin Description

PIN NO.	Symbol	I/O	Description
1	GND	P	ground
2	TP_RESET	I	Touch circuit reset pin
3	TP_INT	I	Touch screen interrupt line
4	TP_SCL	I	Touch Serial interface clock input for I2C interface.
5	TP_SDA	I	Touch Serial interface address and data input/output for I2C interface
6	IOVCC	P	Power supply
7	VCC	P	Power supply
8	CS	I	Chip selection pin.
9	SCL	I	In SPI mode, this pin is used as SCL
10	SDA	I	SPI interface input/output pin.
11	RESET	I	This signal will reset the device and it must be applied to properly initialize the chip
12	DE	I	Data enable signal for RGB interface operation.
13	DCLK	I	Dot clock signal for RGB interface operation.
14	HS	I	Horizontal synchronizing input signal for RGB interface operation.
15	VS	I	Vertical synchronizing input signal for RGB interface operation.
16	B0	I	data bus
17	B1	I	data bus
18	B2	I	data bus
19	B3	I	data bus
20	B4	I	data bus
21	B5	I	data bus
22	G0	I	data bus
23	G1	I	data bus
24	G2	I	data bus
25	G3	I	data bus
26	G4	I	data bus

27	G5	I	data bus
28	R0	I	data bus
29	R1	I	data bus
30	R2	I	data bus
31	R3	I	data bus
32	R4	I	data bus
33	R5	I	data bus
34	NC	I	
35	LEDK	P	Power for LED backlight cathode
36	NC		
37	LEDA	P	Power for LED backlight anode
38	NC		
39	GND	P	ground
40	GND	P	ground

7-3 Timing Characteristics

7.4.2 3-SPI Serial Data Transfer Interface Characteristics:



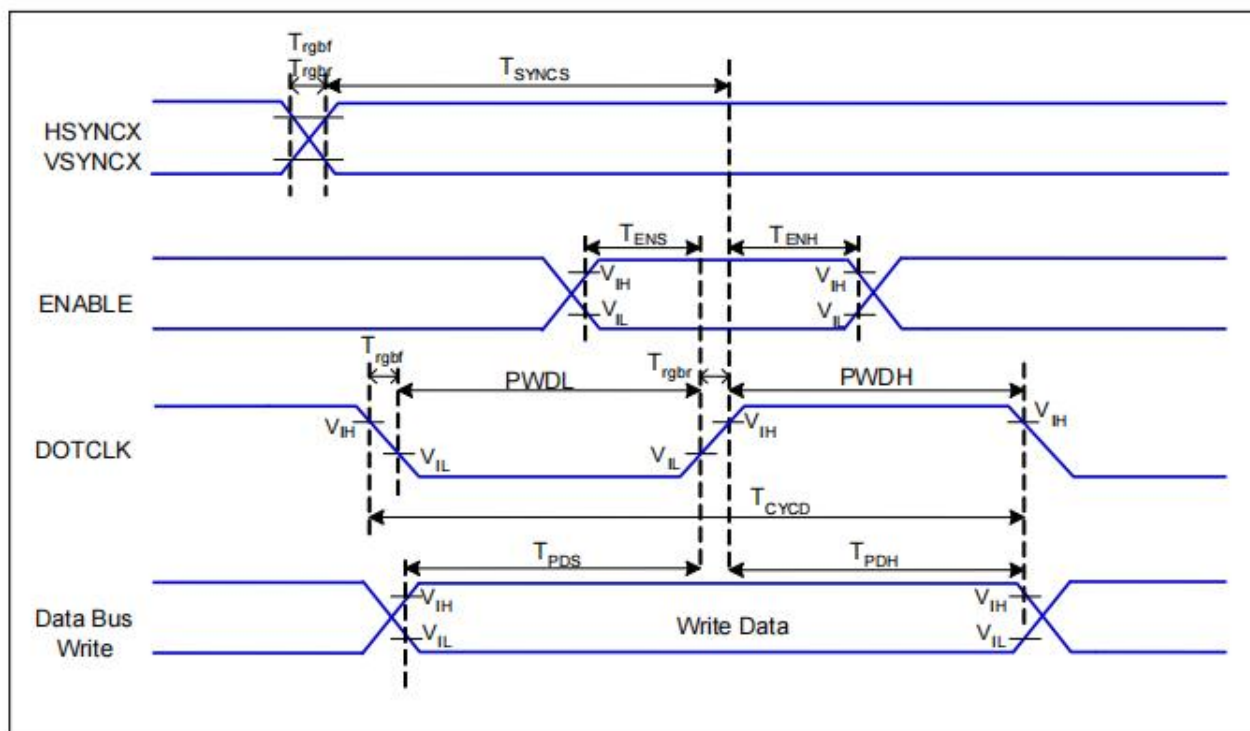
3-SPI Interface Timing Characteristics

$V_{DDI}=1.8V, V_{DDA}=2.8V, AGND=DGND=0V, T_a=25^{\circ}C$

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	
	T_{SLW}	SCL "L" pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum $CL=30pF$
	T_{OH}	Output disable time	15	50	ns	For minimum $CL=8pF$

3-SPI Interface Characteristics

7.4.4 RGB Interface Characteristics:

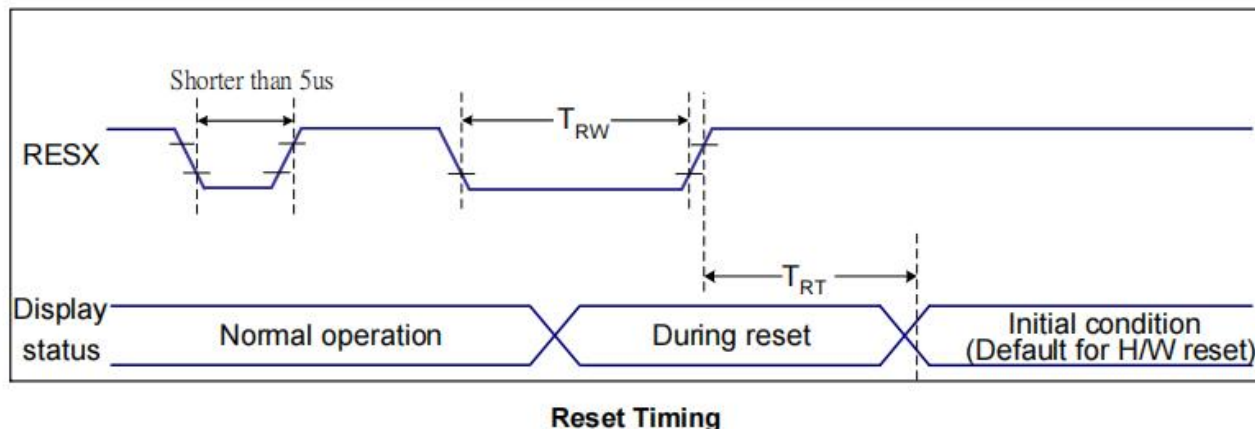


$V_{DDI}=1.8V, V_{DDA}=2.8V, AGND=DGND=0V, T_a=25^{\circ}C$

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	15	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	15	-	ns	
	T_{ENH}	Enable Hold Time	15	-	ns	
DOTCLK	$PWDH$	DOTCLK High-level Pulse Width	30	-	ns	
	$PWDL$	DOTCLK Low-level Pulse Width	30	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	66	-	ns	
	T_{rghr}, T_{rghf}	DOTCLK Rise/Fall time	-	15	ns	
DB	T_{PDS}	PD Data Setup Time	15	-	ns	
	T_{PDH}	PD Data Hold Time	15	-	ns	

RGB Interface Timing Characteristics

7.4.6 Reset Timing



VDDI=1.8V, VDDA=2.8V, AGND=DGND=0V, Ta=25℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120 (Note 1, 6, 7)	ms

Table 1 Reset Timing

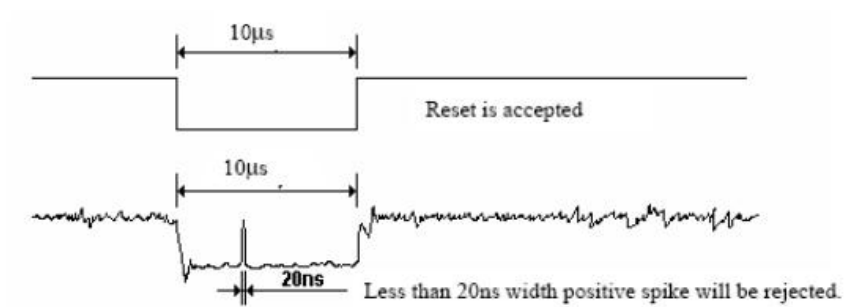
Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

8. Electro-Optical Characteristics

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time		Tr +Tf	$\theta_x = \theta_y = 0$	---	25	35	ms	Note 1
Contrast Ratio		CR		800	1000	---	---	Note 2
Transmittance		T%		3.45	4.05	---	%	
Color Chromaticity (CIE1931)	White	W x	$\theta_x = \theta_y = 0$	---	0.304	---	---	
		W y		---	0.332	---	---	
Viewing angle	θ_T		CR > 10	80	85	---	Deg.	Note 3
	θ_B			80	85	---		
	θ_L			80	85	---		
	θ_R			80	85	---		

1.Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o' clock direction and the vertical or 6, 12 o' clock direction with respect to the optical axis which is normal to the LCD surface (see FIGURE 1).

2.Contrast measurements shall be made at viewing angle of $\Theta = 0$ and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state . (see FIGUR 1)
Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3.Transmittance is the Value without APF and without CG.

4.The color chromaticity coordinates specified in the above table shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

5.The electro-optical response time measurements shall be made as FIGURE

2. The times needed for the luminance to change from 10% to 90% is Tr, and 90% to 10% is Tf.

Figure1 Measurement Set Up

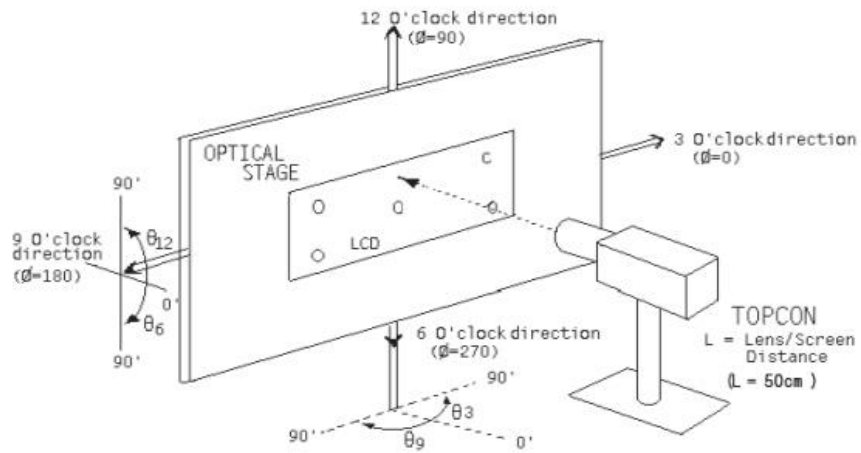
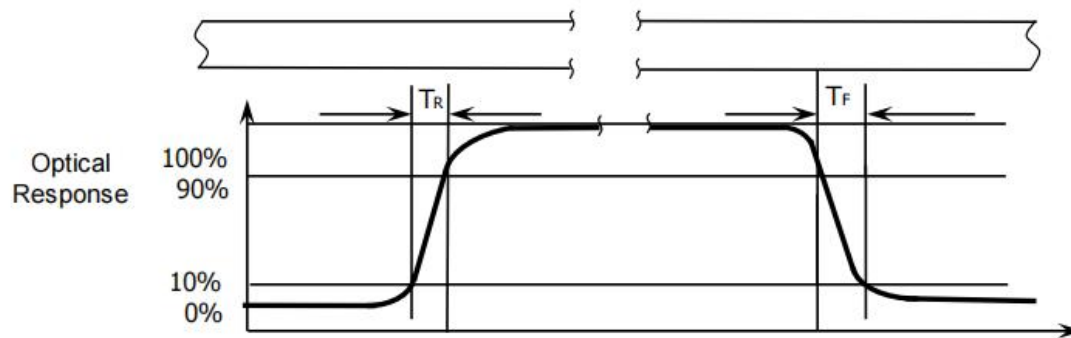
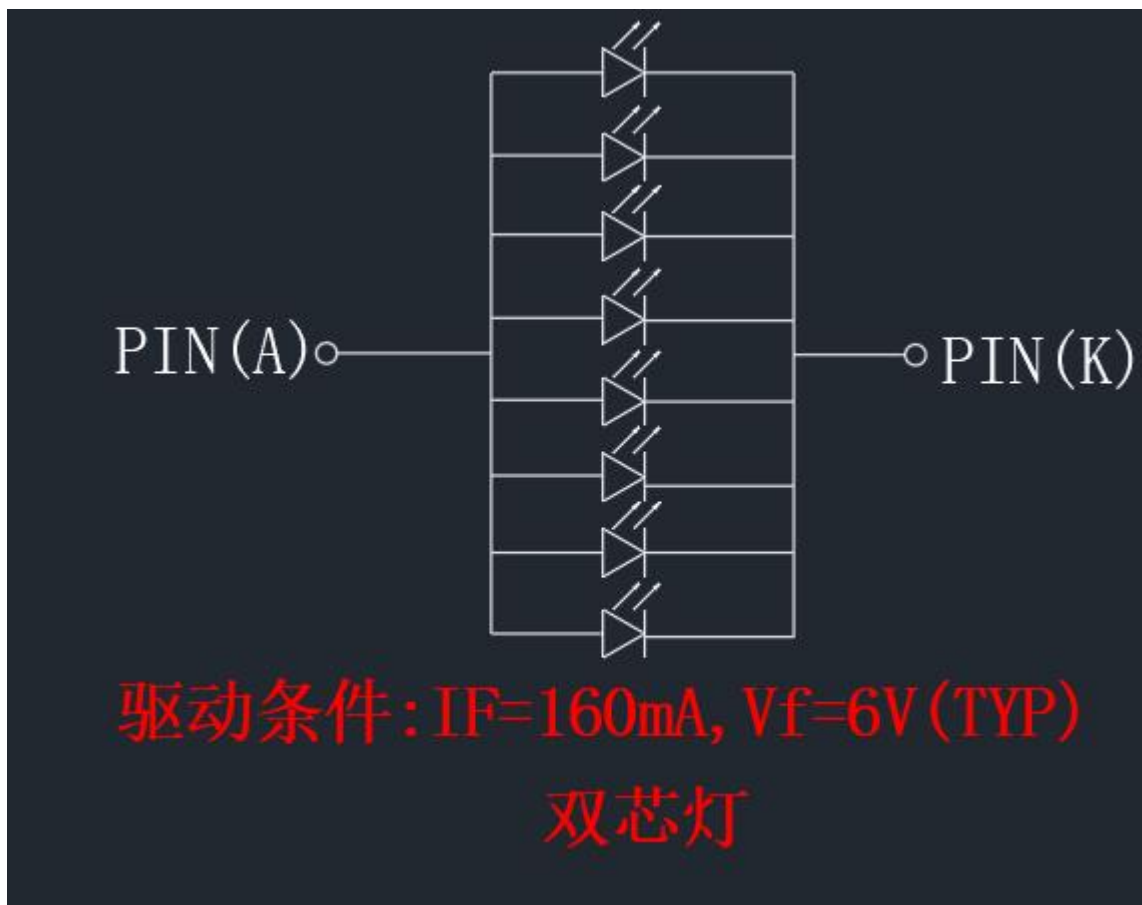


Figure2 Response Time Testing



Note(4) Backlight circuit



9.Records Of Version

Version	Revise Date	Page	Content
00	2026-9-2	ALL	New released