PRODUCT SPECIFICATION FOR LCD MODULE

Revision: 1.0

Model No: LSC101I33-MP-V2

Module Type: COG+FPC+B/L+LENS

APPROVED SIGNATURE

■ Approved Product Specification only

□ Approved Product Specification and Samples

Prepared By	Checked By	Approved By

Contents

目录

1. General Description

LSC101I33-MP-V2 is a transmissive type a-Si TFT-LCD (amorphous silicon thin film transistor liquid crystal display) module, which is composed of a TFT-LCD panel, a driver circuit and a backlight unit. The panel size is 10.1 inch and the resolution is 800(RGB)*1280, the panel can display up to 16.7M colors.

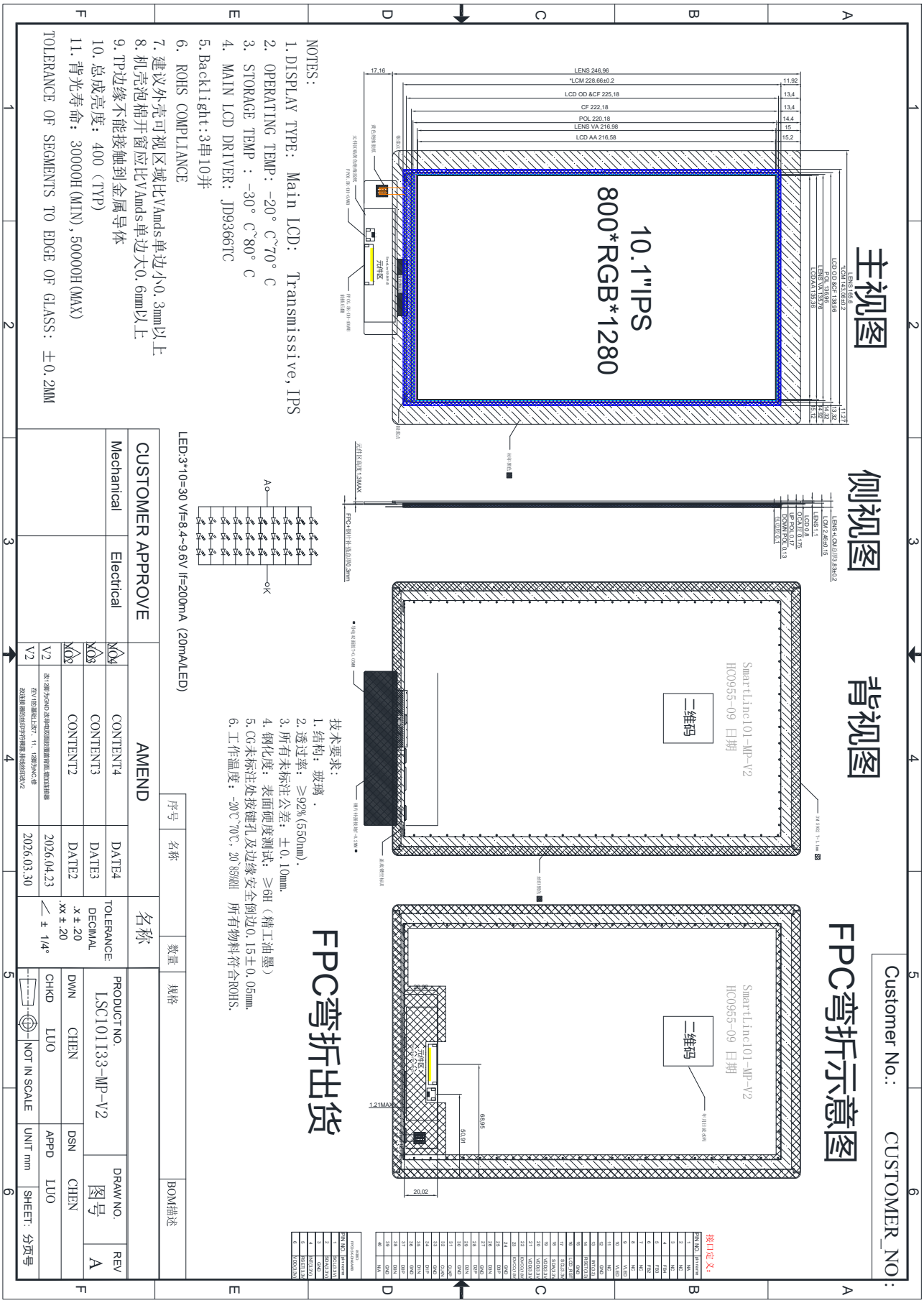
2. Physical Features

Display Mode	TFT-LCD Module
	Active matrix TFT, Transmissive type
Display Format	Graphic 800(RGB)×1280 Dot-matrix
Input Data	MIPI
Viewing Direction （Grayscale Inversion）	Free（IPS）
Drive	JD9366TC

3. Mechanical Specification

Item	Specification	Unit
Module size (H×V×D)	165.6 ×246.96×3.83	mm
Number of dots	800(RGB) ×1280	pixel
Active area (H×V)	135.36×216.58	mm

4. Outline Dimension



5. Absolute Maximum Ratings

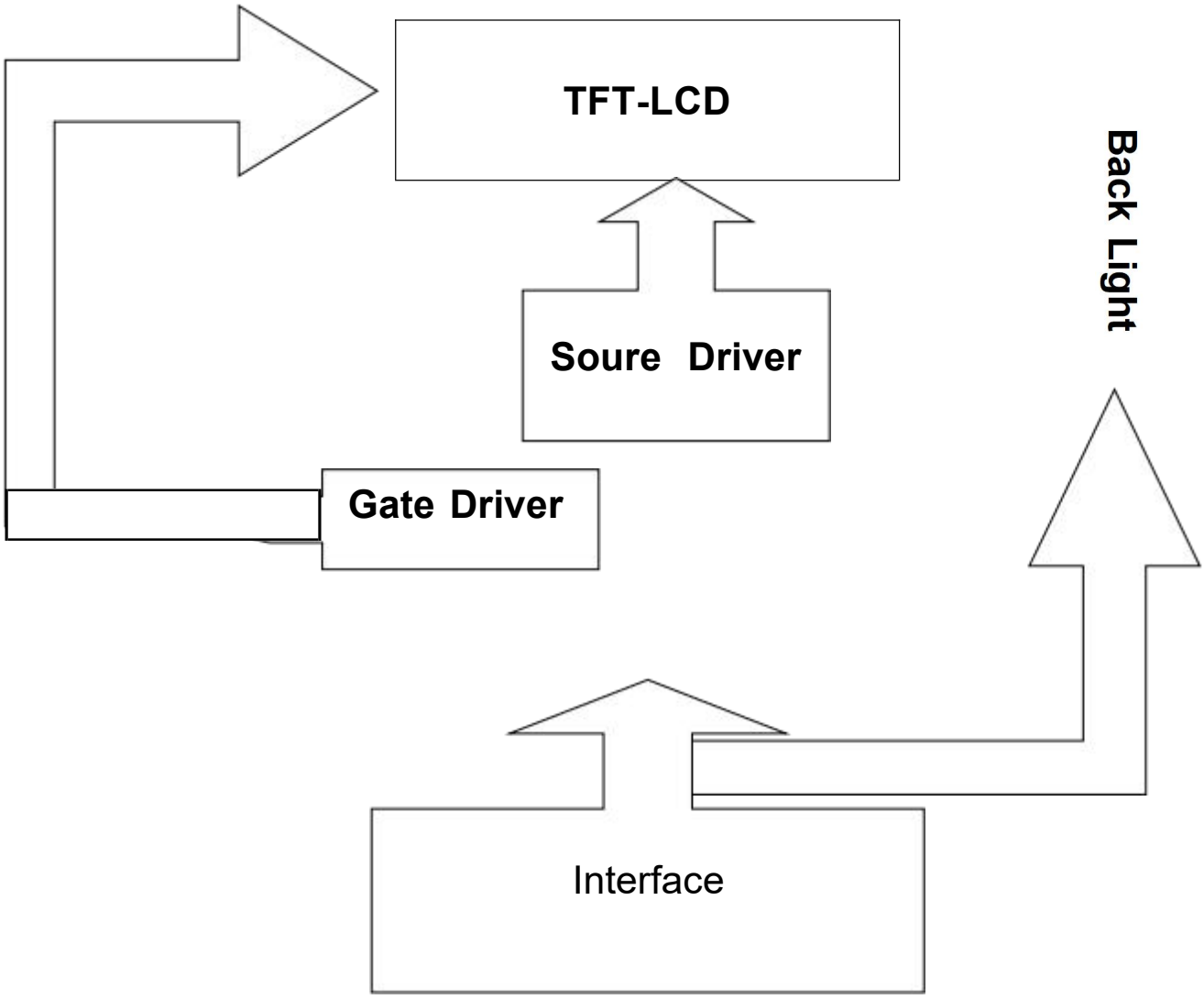
Item	Symbol	Min	Max	Unit	Remark
Supply voltage	VCC	-0.3	3.3	V	Note1 Note2
Supply voltage	IOVCC	-0.3	1.95	V	
Operating temperature	TOPR	-20	70	℃	
Storage temperature	TSTR	-30	80	℃	

6. Electrical Characteristics

Item		Symbol	Rating			Unit	Remark
			Min	Typ	Max		
Supply voltage		VCC	---	3.3	---	V	Note1
Supply voltage		IOVCC	1.65	1.8	1.95	V	
Input Voltage	L level	VIL	0	---	0.3*IOVCC	V	
	H level	VIH	0.7*VCC	---	IOVCC	V	

7. Module Function Description

7-1. Block Diagram Of LCM



7-2. Pin Description

PIN NO.	Symbol	I/O	Description
1	NC		
2	NC		
3	NC		
4	LEDK	P	Power for LED backlight cathode
5	LEDK	P	Power for LED backlight cathode
6	LEDK	P	Power for LED backlight cathode
7	LEDK	P	Power for LED backlight cathode
8	NC		
9	LEDA	P	Power for LED backlight anode
10	LEDA	P	Power for LED backlight anode
11	LEDA	P	Power for LED backlight anode
12	NC		
13	TP_INT(3.3V)	I	Touch screen interrupt line. Interrupt active when the line is low.
14	TP_RESET(3.3V)	I	Touch circuit reset pin
15	GND	P	ground.
16	LCD_RST(1.8V)	I	Global reset pin
17	TP_SDA(3.3V)	I/O	Touch Serial interface address and data input/output for I2C interface
18	TP_SCL(3.3V)	I	Touch Serial interface clock input for I2C interface.
19	VDD(3.3V)	P	Power supply 3.3V
20	VDD(3.3V)	P	Power supply 3.3V
21	VDD(3.3V)	P	Power supply 3.3V
22	IOVCC(1.8V)	P	Power supply VDDI=1.65V to 1.95V.
23	IOVCC(1.8V)	P	Power supply VDDI=1.65V to 1.95V.
24	GND	P	ground.
25	D3P	I	MIPI data input pin.

26	D3N	I	MIPI data input pin.
27	GND	P	ground.
28	D2P	I	MIPI data input pin.
29	D2N	I	MIPI data input pin.
30	GND	P	ground.
31	CLKP	I	MIPI clock input pin.
32	CLKN	I	MIPI clock input pin.
33	GND	P	ground.
34	D1P	I	MIPI data input pin.
35	D1N	I	MIPI data input pin.
36	GND	P	ground.
37	D0P	I/O	MIPI data input pin.
38	D0N	I/O	MIPI data input pin.
39	GND	P	ground.
40	NC		

7-3 Timing Characteristics

12.3.1.Reset input timings

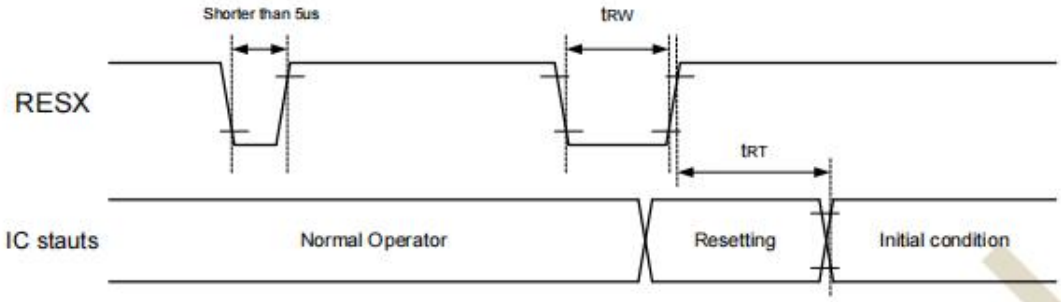


Figure 12.1: Reset input timings

Symbol	Parameter	Related pins	Min.	Max.	Unit
t_{RW}	Reset pulse width(2)	RESX	10	-	μs
t_{RT}	Reset complete time(3)	-	-	5 (Note 5)	ms
		-	-	120 (Note 6, 7)	ms

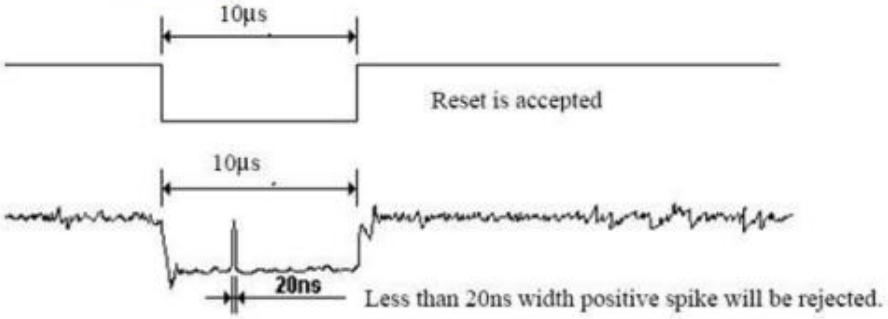
Note: (1) The reset complete time also required time for loading ID bytes from OTP to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

(2) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5 μs	Reset Rejected
Longer than 10 μs	Reset
Between 5 μs and 10 μs	Reset Start

(3) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then returns to Default condition for H/W reset.

(4) Spike Rejection also applies during a valid reset pulse as shown below:



(5) When Reset is applied during Sleep In Mode.

(6) When Reset is applied during Sleep Out Mode.

(7) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

(8) After Sleep Out Command, it is necessary to wait 120msec then send RESX.

Table 12.3: Reset timings

Burst Mode Data Transmission

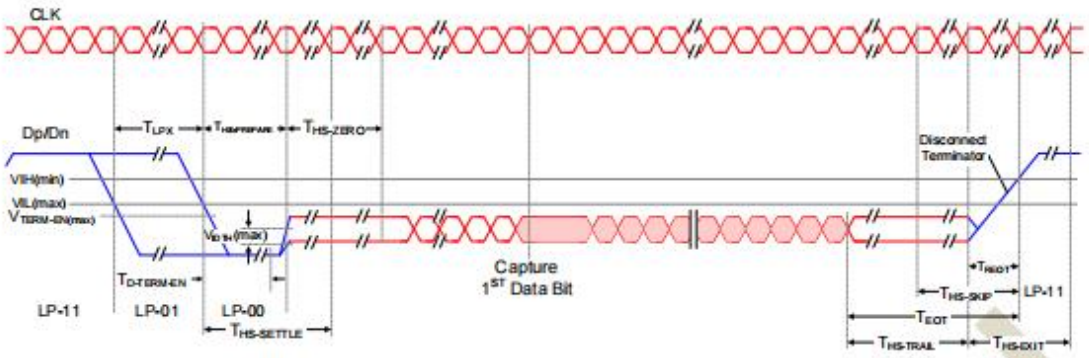


Figure 12.7: High-Speed Data Transmission in Bursts

Parameter	Description	Min	Typ	Max	UNIT
T_{LPX}	Transmitted length of any Low-Power state period	50	-	-	ns
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40 + 4*UI	-	85 + 6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145 + 10*UI	-	-	ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination.	-	-	35 + 4*UI	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions.	85 + 6*UI	-	145 + 10*UI	ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	max(n*8*UI, 60 + n*4*UI)	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns

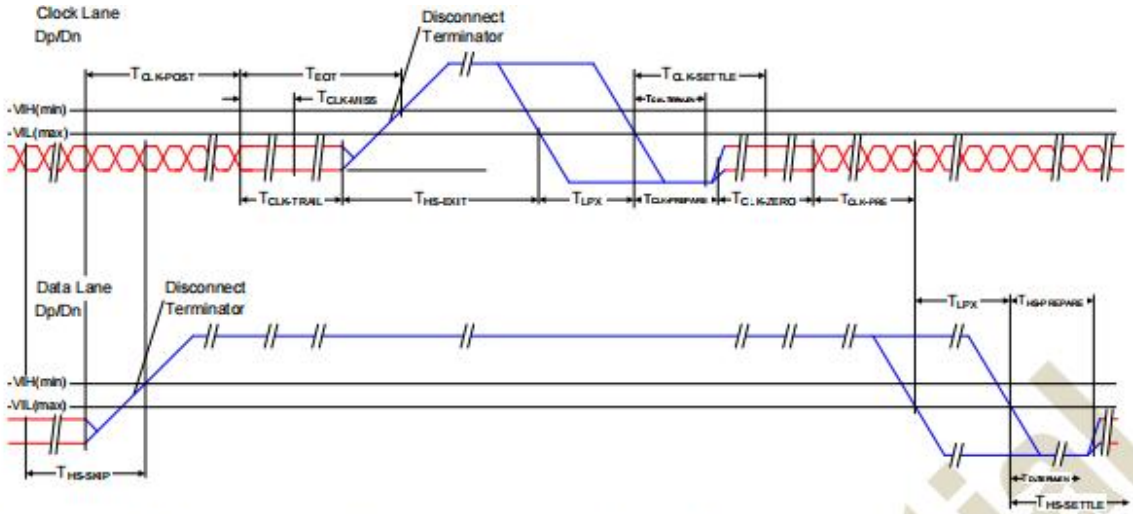


Figure 12.8: Switching the Clock Lane between Clock Transmission and Low-Power Mode

Parameter	Description	Min	Typ	Max	UNIT
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode.	60 + 52*UI	-	-	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8*UI	-	-	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38	-	95	ns
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300	-	-	ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination.	-	-	38	ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns

12.3.3. Timings for DSI Video mode

Vertical Timings

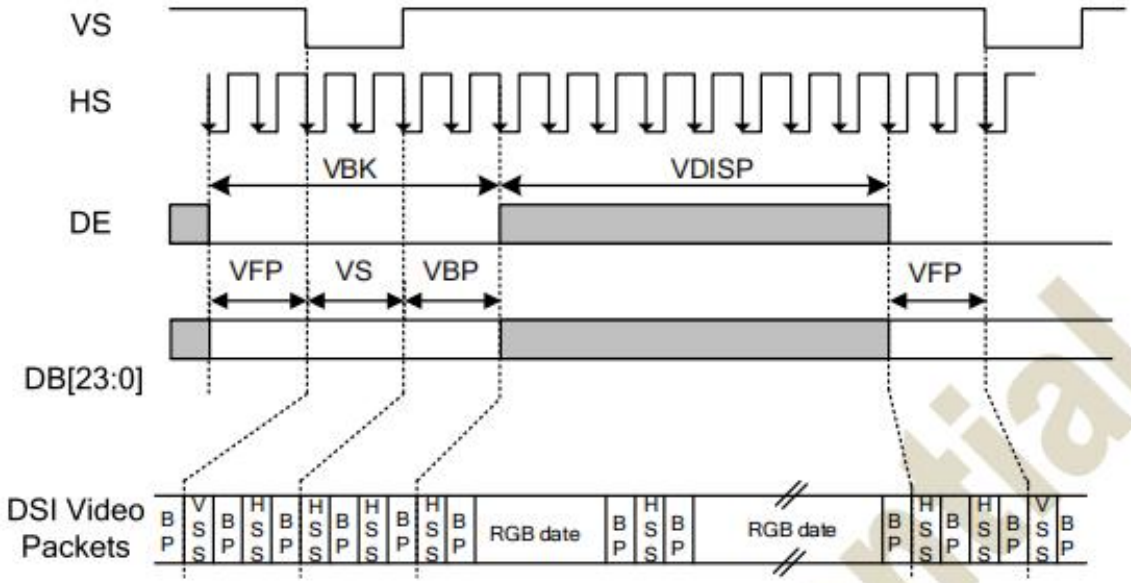


Figure 12.9: Vertical Timings for DPI I/F

Resolution=800x1280(T_A=25°C, IOVCC=1.8V, VCIP=2.8V, VCI=2.8V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical low pulse width	VS	-	2	4	200 Note(1)	Line
Vertical front porch	VFP	-	4	20	200	Line
Vertical back porch	VBP	-	2	10	200 Note(1)	Line
Vertical blanking period	VBK	VS+VBP+VFP	8	34	250	Line
Vertical active area	-	VDISP	-	1280	-	Line
Vertical Refresh rate	VRR	-	-	60	-	Hz

Note: (1) The VS and VBP pulse width are related to GIP start pulse and GIP clock pulse timing. The GIP start pulse and GIP clock pulse must be set at corresponding position for LCD normal display.

Table 12.13: Vertical Timings for RGB I/F

Horizontal Timings

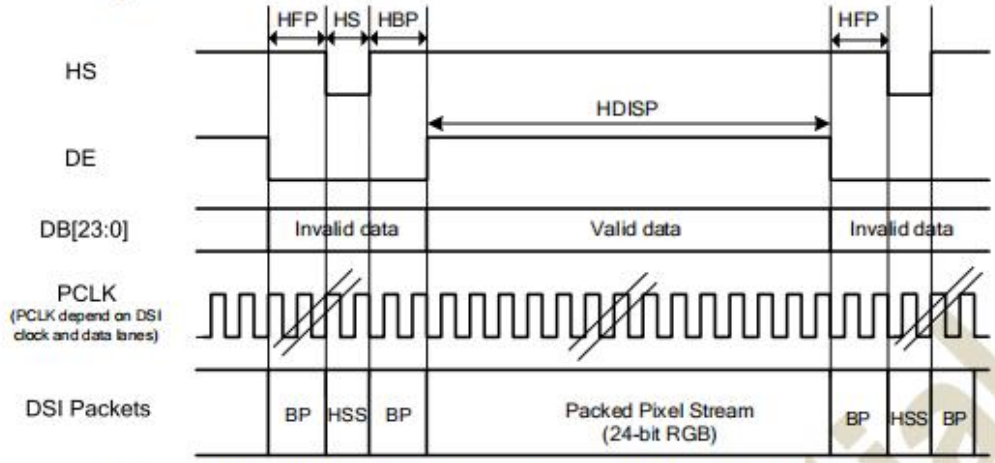


Figure 12.10: Horizontal Timing for DSI Video mode I/F

Resolution=800x1280 (T_A=25°C, IOVCC=1.8V, VCIP=VCI=VCCH=2.8V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HS low pulse width	HS	-	6	18	-	DCK
Horizontal back porch	HBP	-	5	18	-	DCK
Horizontal front porch	HFP	-	5	18	-	DCK
Horizontal blanking period	HBLK	HS+HBP+HFP	16	54 (Note1)	-	DCK
Horizontal active area	HDISP	-	-	800	-	DCK
Pixel Clock	PCLK	-	63.06 (Note2)	67.33 (Note2)	-	MHz

Note 1: HS+HBP > 0.5us.
Note 2: Pixel Clock = (HBLK+HDISP) * (VBK+VDISP) * Frame rate, Frame rate=60Hz.

Table 12.14: Horizontal Timings for DSI Video mode I/F

8. Electro-Optical Characteristics

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time		Tr +Tf	θx = θy =0	---	30	35	ms	Note 1
Contrast Ratio		CR		1000	1500	---	---	Note 2
Transmittance		T%		5.35	6.04	---	%	
Color Chromaticity (CIE1931)	White	W x	θx = θy =0	---	0.303	---	---	
		W y		---	0.319	---	---	
Viewing angle	θ_T		CR > 10	80	85	---	Deg.	Note 3
	θ_B			80	85	---		
	θ_L			80	85	---		
	θ_R			80	85	---		

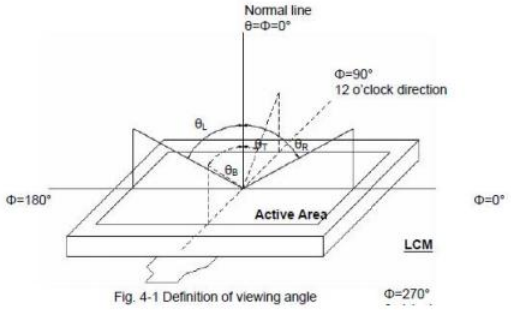


Fig. 4-1 Definition of viewing angle

Note 2: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 30 minutes operation, the optical properties are measured at the center point of the LCD screen.

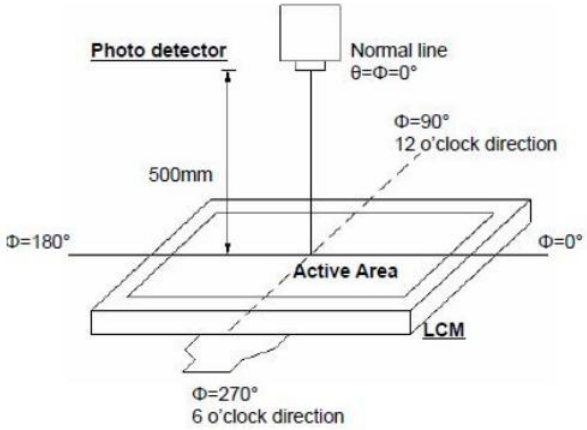
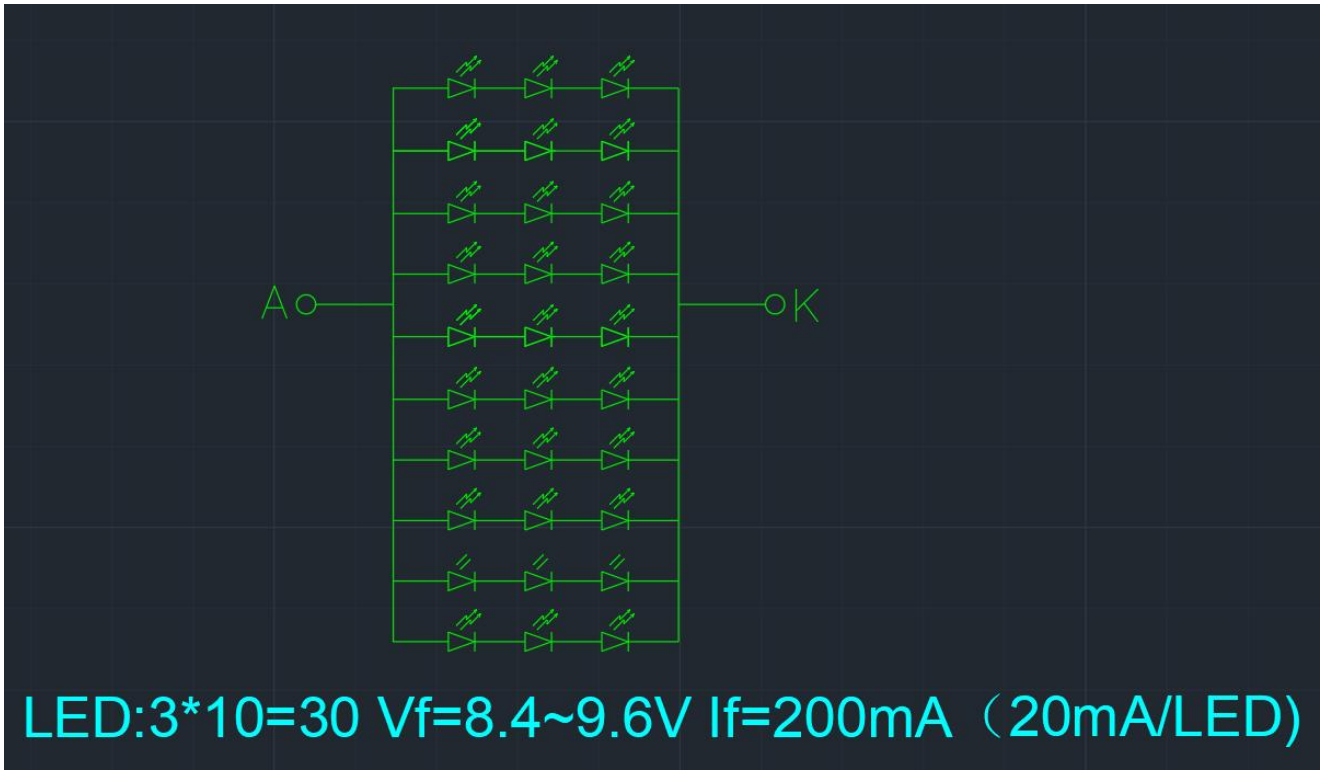


Fig. 4-2 Optical measurement system setup

Note 3: Definition of response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rising time (Tr) is the time between photo detector output intensity changed from 10% to 90%. And falling time (Tf) is the time between photo detector output intensity changed from 90% to 10%.

Backlight circuit



9.Records Of Version

Version	Revise Date	Page	Content
00	2025-12-9	ALL	New released