

PRODUCT SPECIFICATION **FOR LCD MODULE**

Revision: 1.0

Model No: LS050I07-MP-V1

Module Type: COG+FPC+B/L

APPROVED SIGNATURE

- ☒ Approved Product Specification only
- ☐ Approved Product Specification and Samples

<u>Prepared By</u>	<u>Checked By</u>	<u>Approved By</u>

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1. General Description

LS050I07-MP-V1 is a transmissive type a-Si TFT-LCD (amorphous silicon thin film transistor liquid crystal display) module, which is composed of a TFT-LCD panel, a driver circuit and a backlight unit. The panel size is 4.94 inch and the resolution is 720(RGB)*1280, the panel can display up to 16.7M colors.

2. Physical Features

Display Mode	TFT-LCD Module
	Active matrix TFT, Transmissive type
Display Format	Graphic 720(RGB)×1280 Dot-matrix
Input Data	MIPI
Viewing Direction (Grayscale Inversion)	Free (IPS)
Drive	NV3051F

3. Mechanical Specification

Item	Specification	Unit
Module size (H×V×D)	64.55 ×117.35 ×1.57	mm
Number of dots	720(RGB) ×1280	pixel
Active area (H×V)	61.56×109.44	mm

4. Outline Dimension

[illegible]

5. Absolute Maximum Ratings

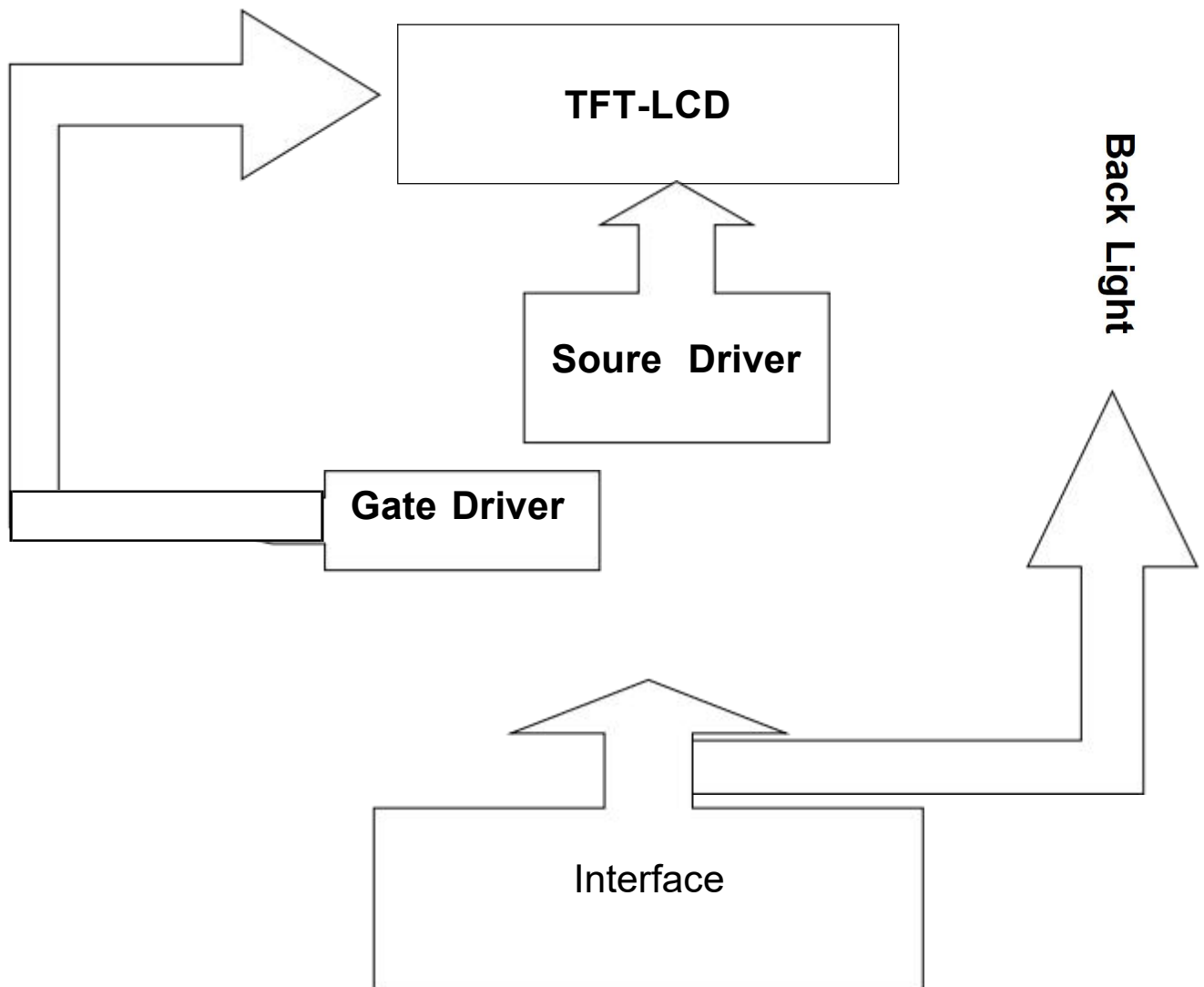
Item	Symbol	Min	Max	Unit	Remark
Supply voltage	VCC	-0.3	6.6	V	Note1 Note2
Supply voltage	IOVCC	-0.3	4.5	V	
Operating temperature	TOPR	-20	70	°C	
Storage temperature	TSTR	-30	80	°C	

6. Electrical Characteristics

Item		Symbol	Rating			Unit	Remark
			Min	Typ	Max		
Supply voltage		VCC	2.5	2.8	6.0	V	Note1
Supply voltage		IOVCC	1.65	1.8	3.6	V	
Input Voltage	L level	VIL	0	---	0.3*IOVCC	V	
	H level	VIH	0.7*IOVCC	---	IOVCC	V	

7. Module Function Description

7- 1. Block Diagram Of LCM

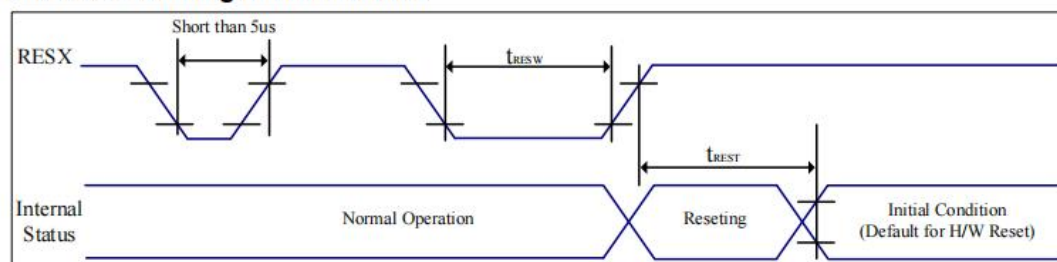


7-2. Pin Description

PIN NO.	Symbol	I/O	Description
1-2	GND	P	ground
3	NC		
4	GND	P	ground
5	NC		
6	NC		
7	NC		
8	NC		
9-10	GND	P	ground
11-13	LEDA	P	LED anode
14	NC		
15-18	LEDK	P	LED cathode
19-20	GND	P	ground
21	MIPI_2P	I	Negative MIPI differential data inputs
22	MIPI_2N	I	Negative MIPI differential data inputs
23	GND	P	ground
24	MIPI_1P	I	Negative MIPI differential data inputs
25	MIPI_1N	I	Negative MIPI differential data inputs
26	GND	P	ground
27	MIPI_CKP	I	Negative MIPI differential clock inputs
28	MIPI_CKN	I	Negative MIPI differential clock inputs
29	GND	P	ground
30	MIPI_0P	I	Negative MIPI differential data inputs
31	MIPI_0N	I	Negative MIPI differential data inputs
32	GND	P	ground
33	MIPI_3P	I	Negative MIPI differential data inputs
34	MIPI_3N	I	Negative MIPI differential data inputs
35	GND	P	ground
36	NC		
37	RESET	I	Reset signal
38	NC		
39	IOVCC	P	Power voltage
40	VDD	P	Power voltage

7-3 Timing Characteristics

7.3.1. Reset timing characteristics



VSS=0V, IOVCC=1.65V to 3.6V, VCI=2.5V to 6.0V, Ta = -30°C to 85°C

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
T_{resw}	*1) Reset low pulse width	RESX	10	-	-	-	us
T_{rest}	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-	-	-	120	When reset applied during Sleep out mode	ms

Table: Reset input timing

Note 1: Due to an electrostatic discharge on RESX line, spike does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts (It depends on voltage and temperature condition.)

Note 2: During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120ms, when Reset Starts in Sleep Out mode. The display remains the blank state in Sleep In mode), then return to default condition for H/W reset.

Note 3: During Reset Complete Time, ID1/ID2/ID3 and VCOM value in OTP will be latched to internal register. After a rising edge of RESX, there is a H/W reset complete time (T_{rest}) which lasted 5ms. The loading operation will be done every time during this reset.

7.3.3.1. High speed mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed Mode						
DSI-CLK+/-	2Xui _{inst}	Double UI instantaneous	2.22	-	25	ns
DSI-CLK+/-	UI _{INSTA} , UI _{INSTB}	UI instantaneous Halfs	1.11	-	12.5	ns
DSI-Dn+/-	T _{ds}	Data to clock setup time	0.15	-	-	UI
DSI-Dn+/-	T _{dh}	Data to clock hold time	0.15	-	-	UI
DSI-CLK+/-	T _{drtclk}	Differential rise time for clock	150	-	0.3UI	ps
DSI-Dn+/-	T _{drtdata}	Differential rise time for data	150	-	0.3UI	ps
DSI-CLK+/-	T _{dfclk}	Differential fall time for clock	150	-	0.3UI	ps
DSI-Dn+/-	T _{dfdata}	Differential fall time for data	150	-	0.3UI	ps

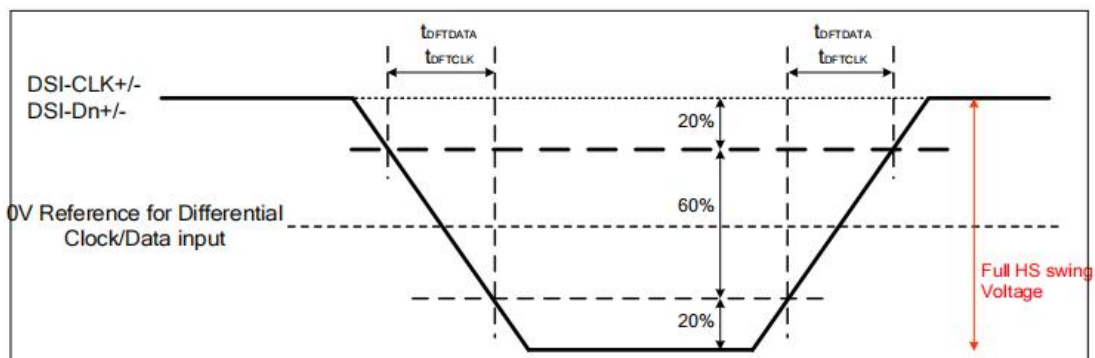
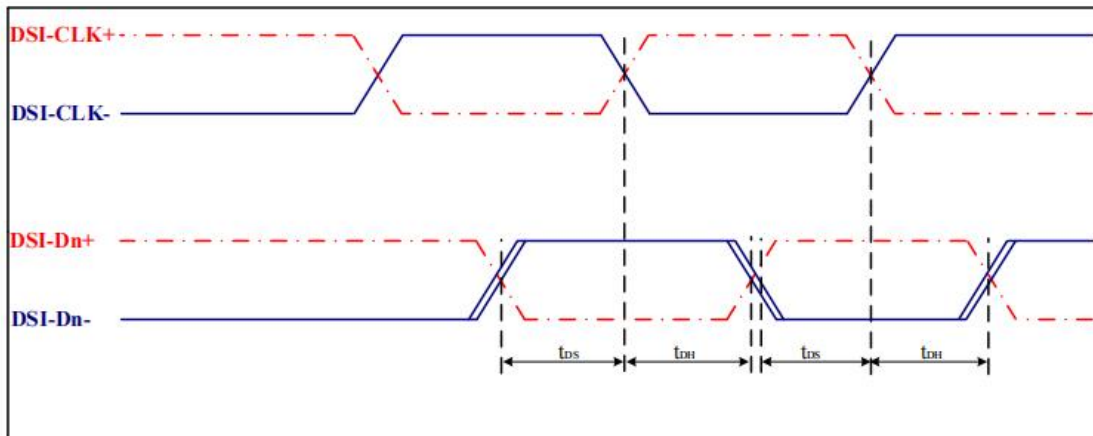
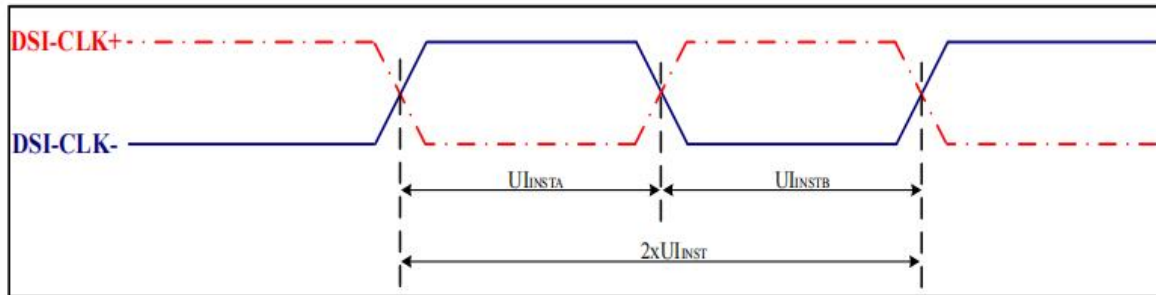


Figure: AC characteristics for MIPI-DSI High speed mode

7.3.3.2. Low power mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Low Power Mode						
DSI-D0+/-	TLPXM	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU Display Module	50	-	-	ns
DSI- D0+/-	TLPXD	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Modulen MPU	58	-	-	ns
DSI- D0+/-	TTA-SURED	Time-out before the MPU start driving	TLPXD	-	2XTLPXD	ns
DSI- D0+/-	TTA-GETD	Time to drive LP-00 by display module	5XTLPXD	-	-	ns
DSI- D0+/-	TTA-GOD	Time to drive LP-00 after turnaround request – MPU	4XTLPXD	-	-	ns
DSI- D0+/-	Ratio TLPX	Ratio of TLPXM / TLPXD between MCU and display module	2/3	-	3/2	

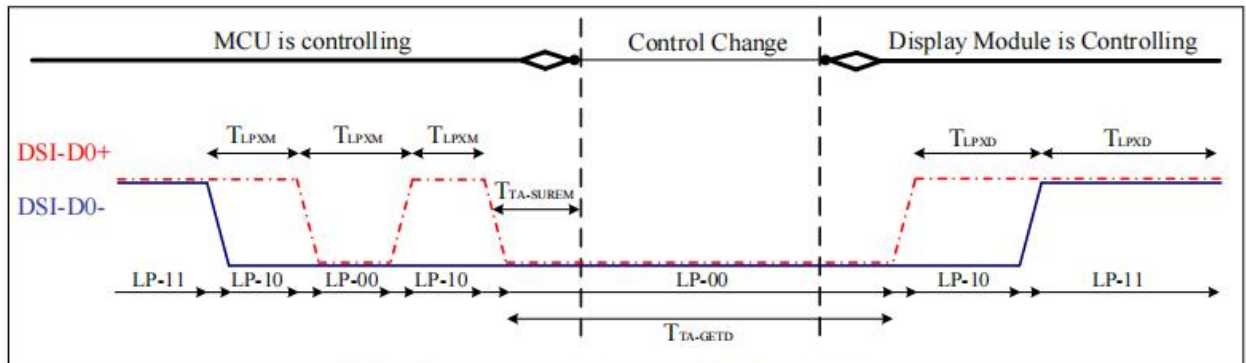


Figure: BTA from the MCU to the Display Module

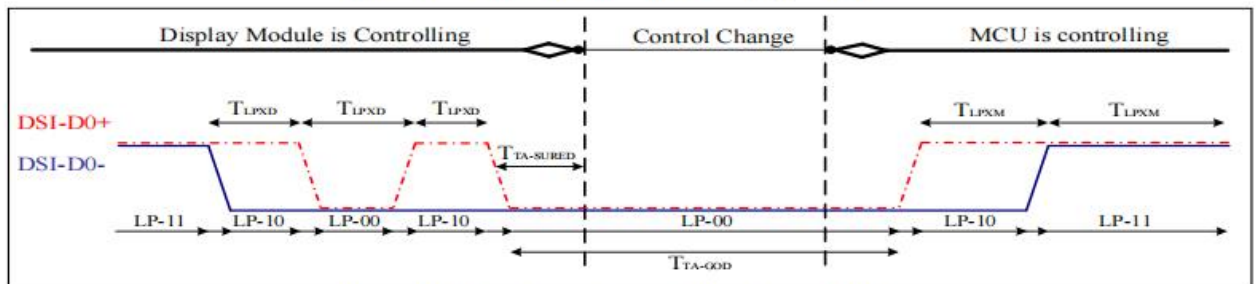


Figure: BTA from the Display Module to the MCU

7.3.3.3. Bursts

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed Data Transmission Bursts						
DSI-Dn+/-	TLPX	Length of any low-power state period	50	-	-	ns
DSI- Dn+/-	THS- PREPARE	Time to drive LP-00 to prepare for HS transmission	40ns+4UI	-	85ns+6UI	ns
DSI- Dn+/-	THS- PREPARE+THS- ZERO	THS-PREPARE+time to drive HS-0 before the sync sequence	145ns+10UI	-	-	ns
DSI- Dn+/-	TD-TERM- EN	Time to enable Data Lane receiver line termination measured from when Dn crosses VIL(max)	Time for Dn to reach VTERM-EN	-	35ns+4UI	ns
DSI- Dn+/-	THS-SKIP	Time-out at RX to ignore transition period of EoT	40	-	55ns+4UI	ns
DSI- Dn+/-	THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	max (8UI, 60ns+4UI)	-	-	ns
DSI- Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	-	ns
DSI- Dn+/-	TeoT	Time from start of THS-TRAIL period to start of LP-11 state	-	-	105ns+12UI	ns

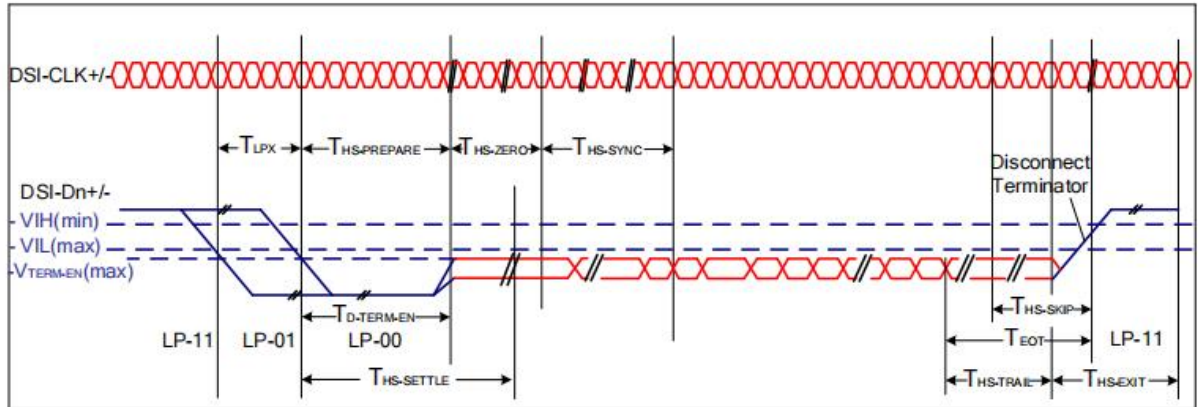


Figure: High Speed Data Transmission Bursts

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Switching the clock Lane between clock Transmission and Low Power Mode						
DSI-CLK+/-	TCLK-POST	Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	60ns+52UI	-	-	ns
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8	-	-	UI
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS clock transmission	38	-	95	ns
DSI-CLK+/-	TCLK-TERM- EN	Time to enable Clock Lane receiver line termination measured from when Dn crosses V _{IL(max)}	Time for Dn to reach V _{TERM-EN}	-	38	ns
DSI- CLK+/-	TCLK-PREPARE +TCLK-ZERO	TCLK-PREPARE + time for lead HS-0 drive period before starting Clock	300	-	-	ns
DSI- CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns
DSI-CLK+/-	TeoT	Time from start of TCLK-TRAIL period to start of LP-11 state	-	-	105ns+12UI	ns

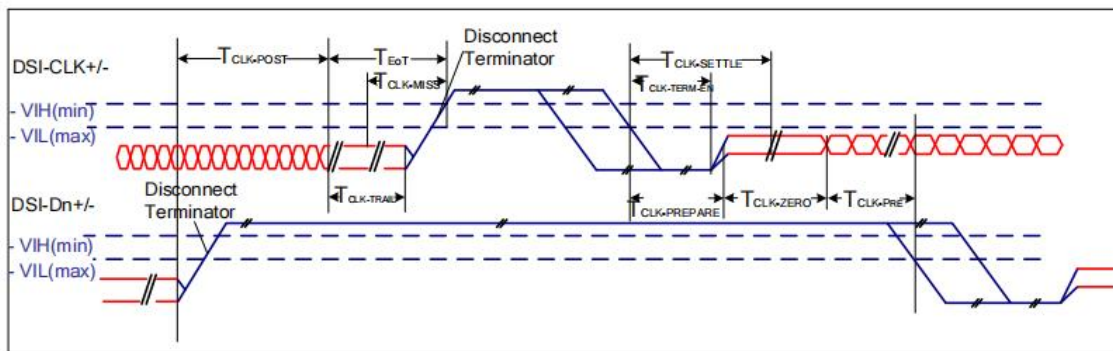


Figure: Switching the clock Lane between clock Transmission and Low Power Mode

8. Electro-Optical Characteristics

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time		Tr +Tf	$\theta_x = \theta_y = 0$	---	50	--	ms	Note 1
Contrast Ratio		CR		---	800	---	---	Note 2
Transmittance		T%		2.87	3.19	---	%	
Color Chromaticity (CIE1931)	White	W x	$\theta_x = \theta_y = 0$	---	0.321	---	---	
		W y		---	0.346	---	---	
Viewing angle	θ_T		CR > 10	---	80	---	Deg.	Note 3
	θ_B			---	80	---		
	θ_L			---	80	---		
	θ_R			---	80	---		
Luminance ($I_F = 40mA$)		L		--	300	---	cd/m2	Note4

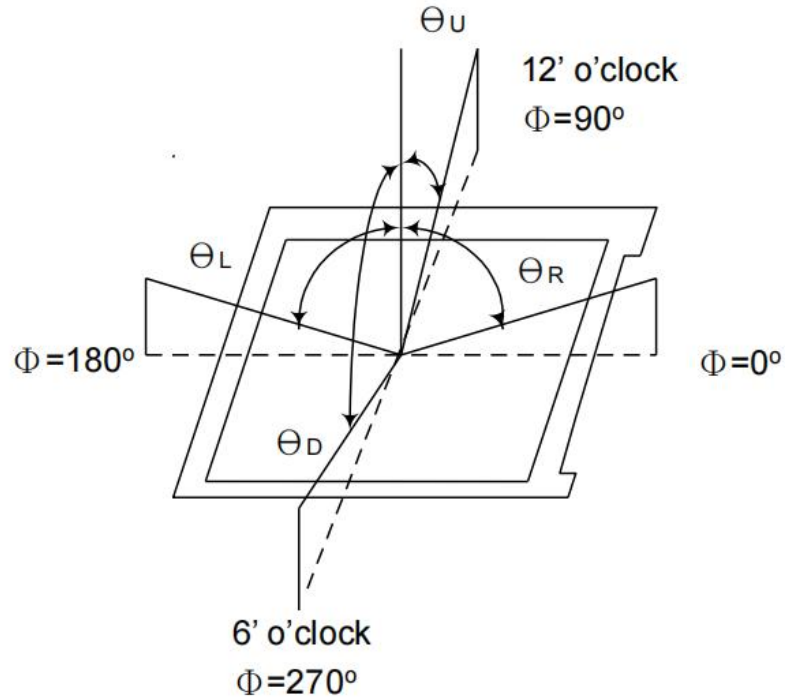
4.2 Measuring Condition

- Measuring surrounding: dark room
- Ambient temperature: 25±2°C
- 30min. warm-up time.

4.3 Measuring Equipment

- FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.
- Measuring spot size : 20 ~ 21 mm

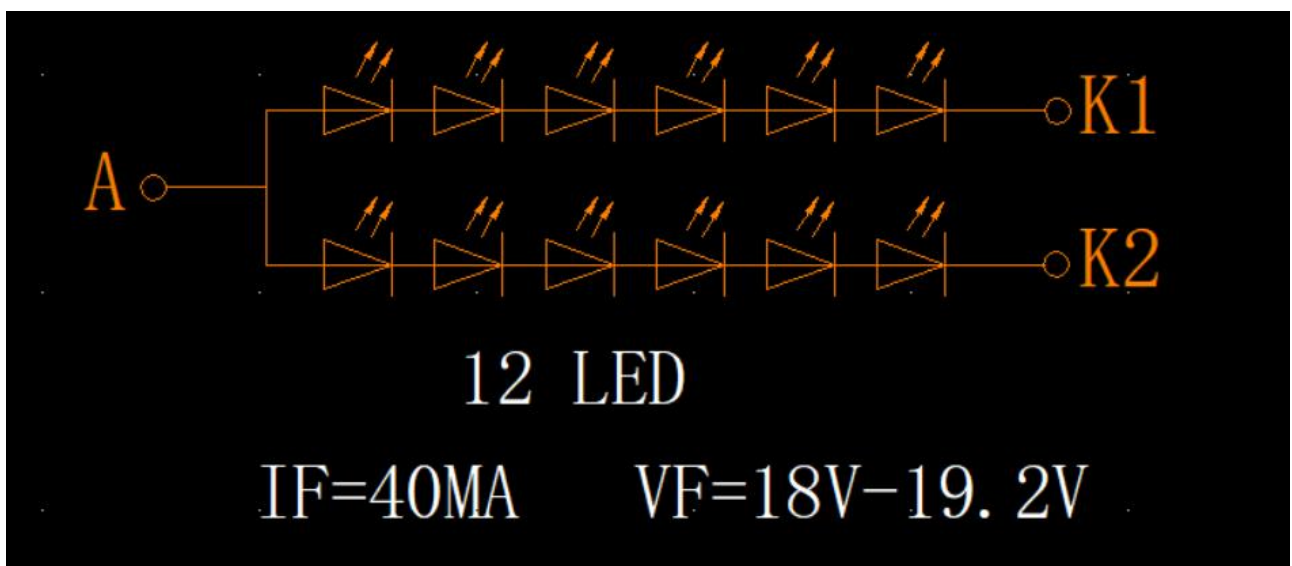
Note (1) Definition of Viewing Angle:



Note (2) Definition of Contrast Ratio(CR) :
measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note(4) Backlight circuit



9. Records Of Version

Version	Revise Date	Page	Content
00		ALL	New released