PRODUCT SPECIFICATION FOR LCD MODULE

Revision: 1.0

Model No: LS043I16-L-V1

Module Type: COG+FPC+B/L

APPROVED SIGNATURE

■ Approved Product Specification only

□ Approved Product Specification and Samples

Prepared By	Checked By	Approved By

Contents

目录

1. General Description

LS043I16-L-V1 is a transmissive type a-Si TFT-LCD (amorphous silicon thin film transistor liquid crystal display) module, which is composed of a TFT-LCD panel, a driver circuit and a backlight unit. The panel size is 4.3 inch and the resolution is 800(RGB)*480, the panel can display up to 16.7M colors.

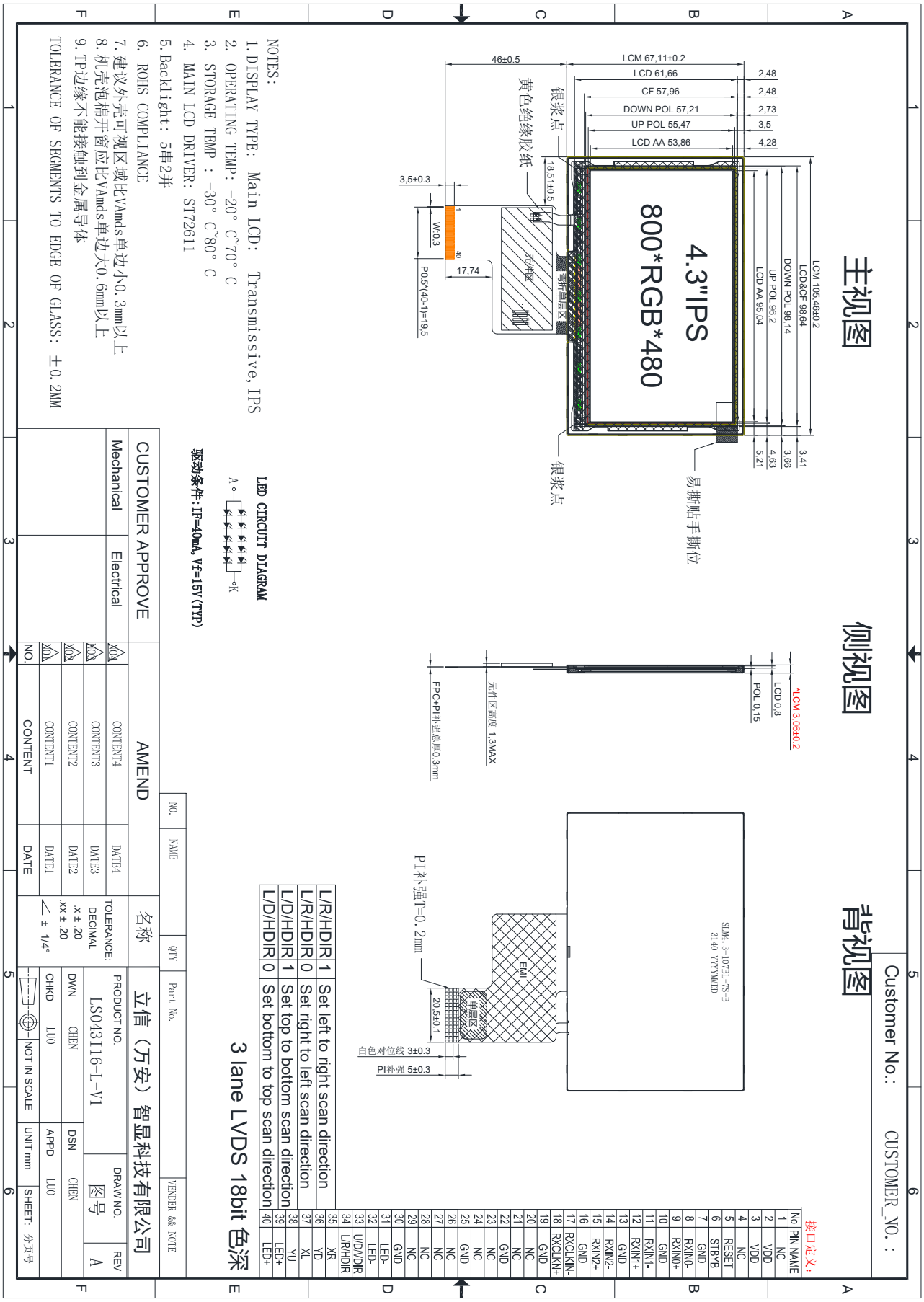
2. Physical Features

Display Mode	TFT-LCD Module
	Active matrix TFT, Transmissive type
Display Format	Graphic 800(RGB)×480 Dot-matrix
Input Data	LVDS
Viewing Direction （Grayscale Inversion）	Free（IPS）
Drive	ST72611

3. Mechanical Specification

Item	Specification	Unit
Module size (H×V×D)	105.46×67.11×3.06	mm
Number of dots	800(RGB)×480	pixel
Active area (H×V)	95.04×53.86	mm

4. Outline Dimension



No	PIN NAME
1	NC
2	VDD
3	VDD
4	NC
5	RESET
6	STBYB
7	GND
8	RXIN0-
9	RXIN0+
10	GND
11	RXIN1-
12	RXIN1+
13	GND
14	RXIN2-
15	RXIN2+
16	GND
17	RXCLKIN-
18	RXCLKIN+
19	GND
20	NC
21	NC
22	GND
23	NC
24	NC
25	GND
26	NC
27	NC
28	NC
29	NC
30	GND
31	LED-
32	LED-
33	UD/VDIR
34	LR/HDIR
35	XR
36	YD
37	XL
38	YU
39	LED+
40	LED+

接口定义：

L/R/HDIR 1	Set left to right scan direction
L/R/HDIR 0	Set right to left scan direction
L/D/HDIR 1	Set top to bottom scan direction
L/D/HDIR 0	Set bottom to top scan direction

3 lane LVDS 18bit 色深

NOTES:
1. DISPLAY TYPE: Main LCD: Transmissive, IPS
2. OPERATING TEMP: -20° C~70° C
3. STORAGE TEMP : -30° C~80° C
4. MAIN LCD DRIVER: ST72611
5. Backlight: 5串2并
6. ROHS COMPLIANCE
7. 建议外壳可视区域比VAmds单边小0.3mm以上
8. 机壳泡棉开窗应比VAmds单边大0.6mm以上
9. TP边缘不能接触到金属导体
TOLERANCE OF SEGMENTS TO EDGE OF GLASS: ±0.2MM

LED CIRCUIT DIAGRAM

驱动条件: IF=40mA, Vf=15V (TYP)

NO.	NAME	QTY	Part No.	VENDER && NOTE

CUSTOMER APPROVE		AMEND		名称	立信（万安）智显科技有限公司		
Mechanical	Electrical			TOLERANCE:	PRODUCT NO.	DRAW NO.	REV
		CONTENT4	DATE4	DECIMAL	LS043I16-L-V1	图号	A
		CONTENT3	DATE3	.x ± 20			
		CONTENT2	DATE2	.xx ± 20	DWN CHEN	DSN CHEN	
		CONTENT1	DATE1	∠ ± 1/4°	CHKD LUO	APPD LUO	
NO.		CONTENT	DATE	NOT IN SCALE	UNIT mm	SHEET: 分页号	

5. Absolute Maximum Ratings

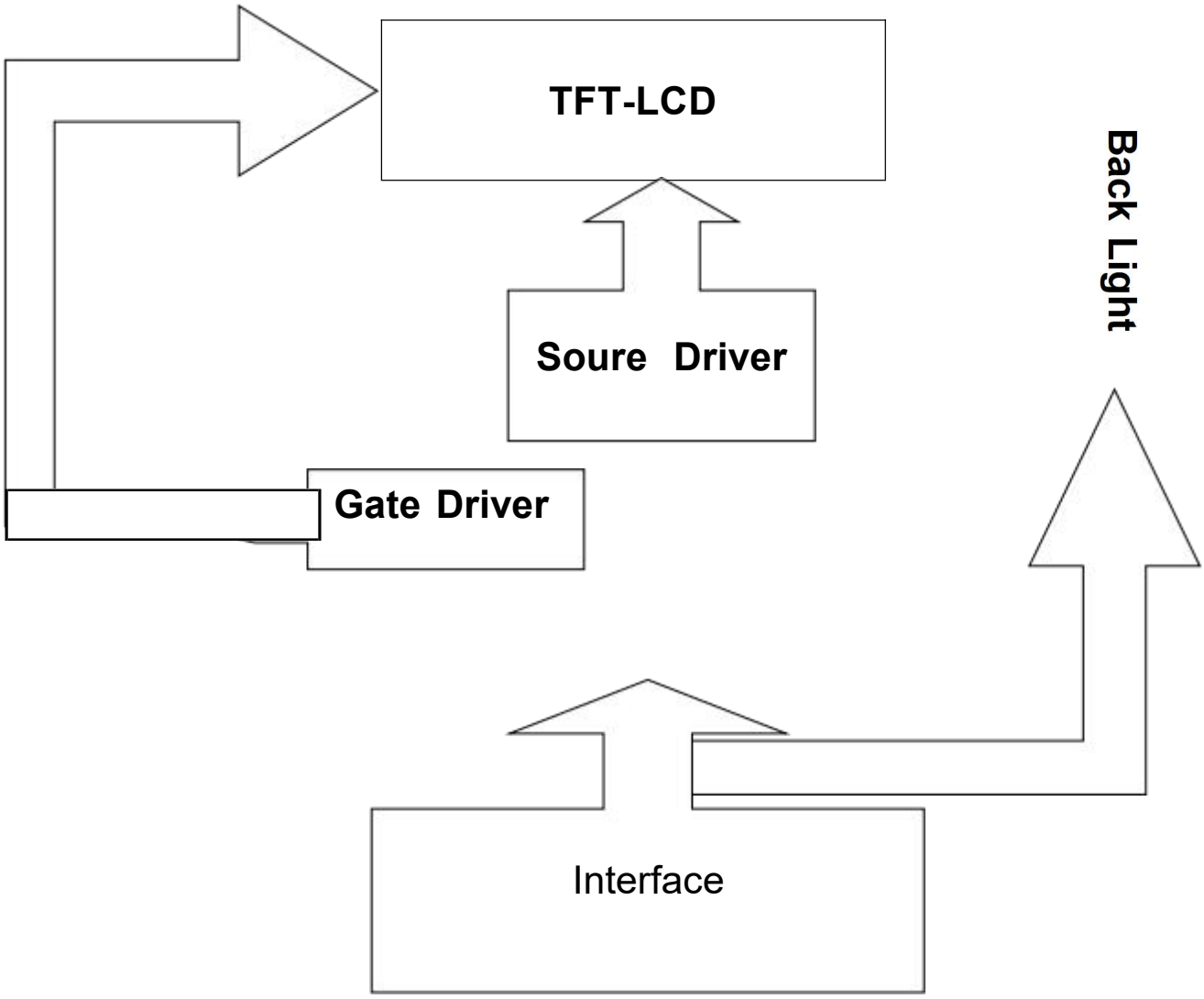
Item	Symbol	Min	Max	Unit	Remark
Supply voltage	VCC	-0.3	3.6	V	Note1 Note2
Supply voltage	IOVCC	-0.3	3.6	V	
Operating temperature	TOPR	-20	70	℃	
Storage temperature	TSTR	-30	80	℃	

6. Electrical Characteristics

Item		Symbol	Rating			Unit	Remark
			Min	Typ	Max		
Supply voltage		VCC	2.5	2.8	3.3	V	Note1
Supply voltage		IOVCC	1.65	1.8	3.3	V	
Input Voltage	L level	VIL	0	---	0.3*IOVCC	V	
	H level	VIH	0.7*IOVCC	---	IOVCC	V	

7. Module Function Description

7-1. Block Diagram Of LCM



7-2. Pin Description

PIN NO.	Symbol	I/O	Description
1	NC		
2	VDD	P	power supply
3	VDD	P	power supply
4	NC		
5	RESET	I	Global reset pin. When GRB is “L”, internal initialization procedure is executed.
6	STBYB	I	L:Standby mode(Default) H:Normal display mode
7	GND	P	
8	RXIN0-	I	LVDS input lane: RX0N
9	RXIN0+	I	LVDS input lane: RX0P
10	GND	P	
11	RXIN1-	I	LVDS input lane: RX1N
12	RXIN1+	I	LVDS input lane: RX1P
13	GND	P	
14	RXIN2-	I	LVDS input lane: RX2N
15	RXIN2+	I	LVDS input lane: RX2P
16	GND	P	
17	RXCLKIN-	I	LVDS clock lane: CLKN
18	RXCLKIN+	I	LVDS clock lane: CLKP
19	GND	P	Ground
20	NC		
21	NC		
22	GND	P	Ground
23	NC		
24	NC		
25	GND	P	Ground
26	NC		
27	NC		
28	NC		
29	NC		
30	GND	P	Ground
31	LEDK	P	Power for LED backlight cathode
32	LEDK	P	Power for LED backlight cathode
33	U/D	I	L:From right to left H:From left to right(Default)
34	L/R	I	L:From down to up H:From up to down(Default)
35	XR	I	TP X+
36	YD	I	TP YU+
37	XL	I	TP X-

38	YU	I	TP YU-
39	LEDA	P	Power for LED backlight anode
40	LEDA	P	Power for LED backlight anode

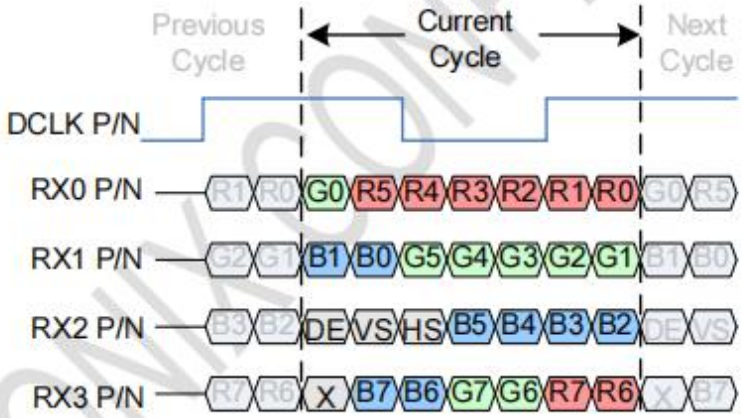
7-3 Timing Characteristic

7.3.1 LVDS Input Pin Mapping Table

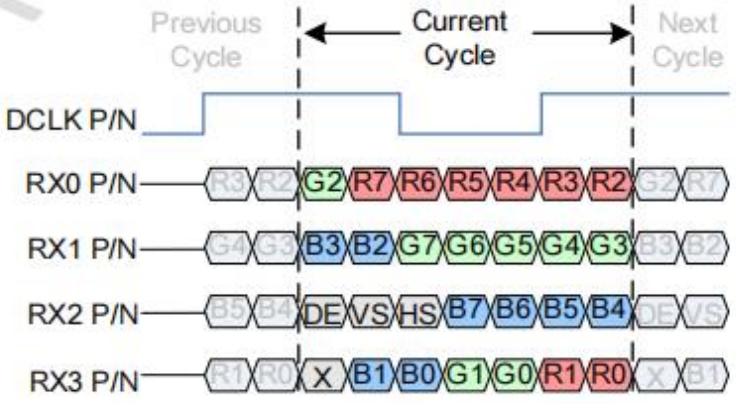
Pin Name RGB (LVDS)	LVDS 3 lane	LVDS 4 Lane
DCLKN	RXCLKN	RXCLKN
DCLKP	RXCLKP	RXCLKP
DB0	RX0P	RX0P
DB1	RX0N	RX0N
DB2	RX1P	RX1P
DB3	RX1N	RX1N
DB4	RX2P	RX2P
DB5	RX2N	RX2N
DB6	-	RX3P
DB7	-	RX3N

Note: Symbol "-" means reserve pin and should fix to "L" by DGND.

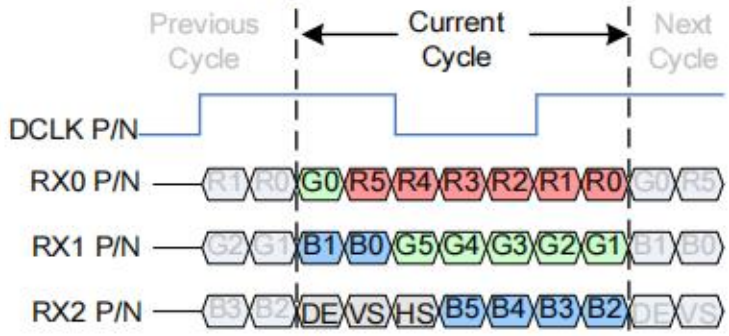
7.3.2 4 Lane VESA Data Format Color Bit Map



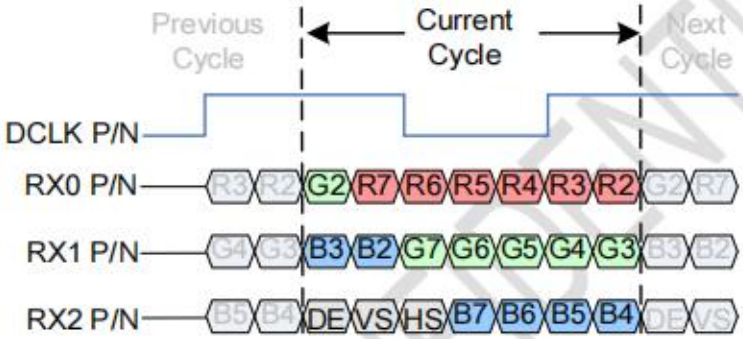
7.3.3 4 Lane JEIDA Data Format Color Bit Map



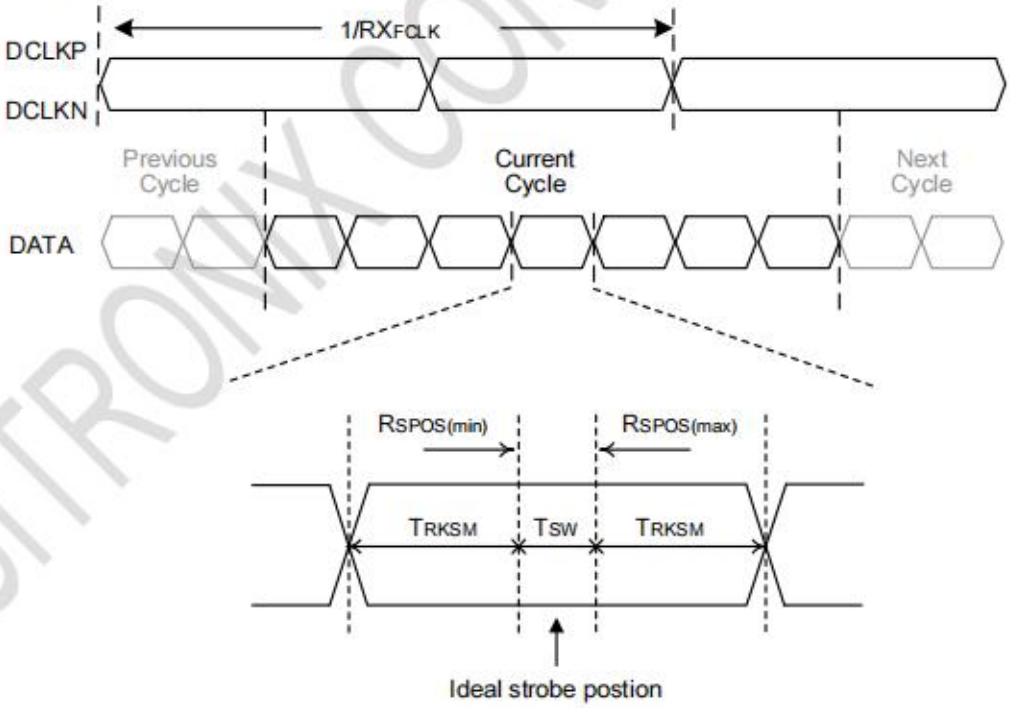
7.3.4 3 Lane VESA Mode Color Bit Map



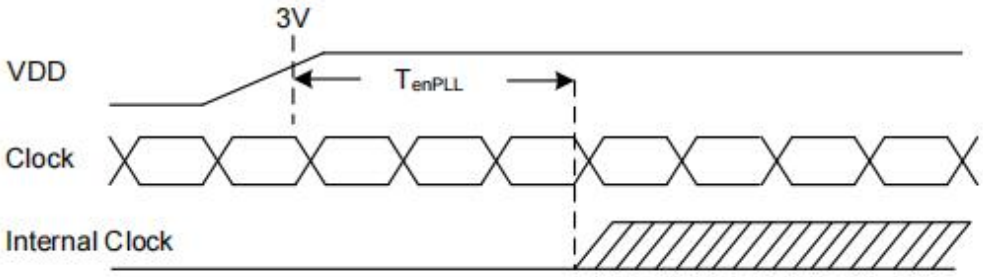
7.3.5 3 Lane JEIDA Mode Color Bit Map



7.3.6 LVDS Input Timing Table



RRKSM : Receiver strobe margin
RSPOS : Receiver strobe position
TSW : Strobe width (internal DATA sampling window)



LVDS Input Timing (PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C).

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Clock Frequency	RX_{FCLK}	23	25	27	MHz	
Input Data Skew Margin	T_{RSKM}	400	-	-	ps	
Clock High Time	T_{LVCH}	4/(7 x RX_{FCLK})			ns	
Clock Low Time	T_{LVCL}	3/(7 x RX_{FCLK})			ns	
PLL Wake-up Time	T_{enPLL}	-	-	150	us	
LVDS Spread Spectrum Clocking (SSC) Tolerance of LVDS Receiver						
Modulation Frequency	SSC_{MF}	-	-	100	KHz	
Modulation Rate	SSC_{MR}	-	-	+/-3	%	

Note. The maximum RXFCLK Frequency is 27MHz. If the case needs faster RXFCLK, please contact Sitronix.

8. Electro-Optical Characteristics

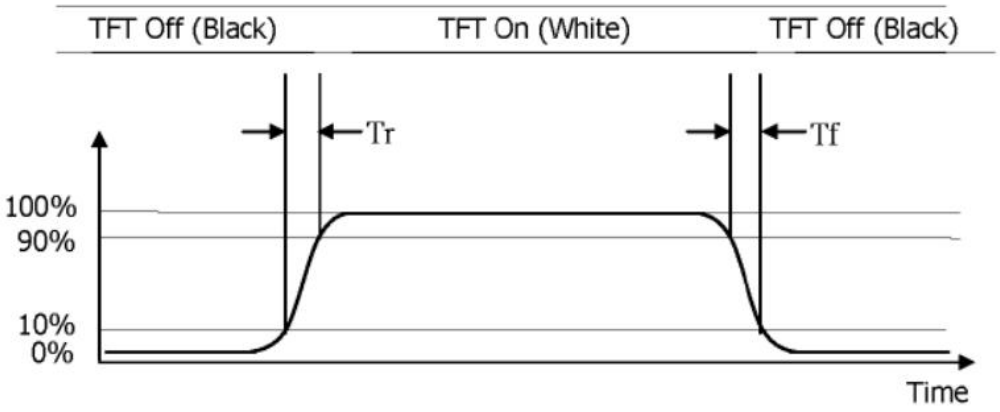
Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle range	Horizontal	Θ_3	CR > 10	-	80	-	Deg.	Note 1
		Θ_9		-	80	-	Deg.	
	Vertical	Θ_{12}		-	80	-	Deg.	
		Θ_6		-	80	-	Deg.	
Luminance Contrast ratio		CR	Θ = 0°	-	1200	-		Note 2
Color Gamut	NTSC	CIE1931	Θ = 0°	-	50	-	%	Note 5 @C Light
Reproduction of color	White	Wx	Θ = 0°	Typ -0.03	0.311	Typ +0.03		
		Wy			0.338			
Response Time		Tr+Td	Ta= 25° C Θ = 0°	-	30	-	ms	Note 6

Note :

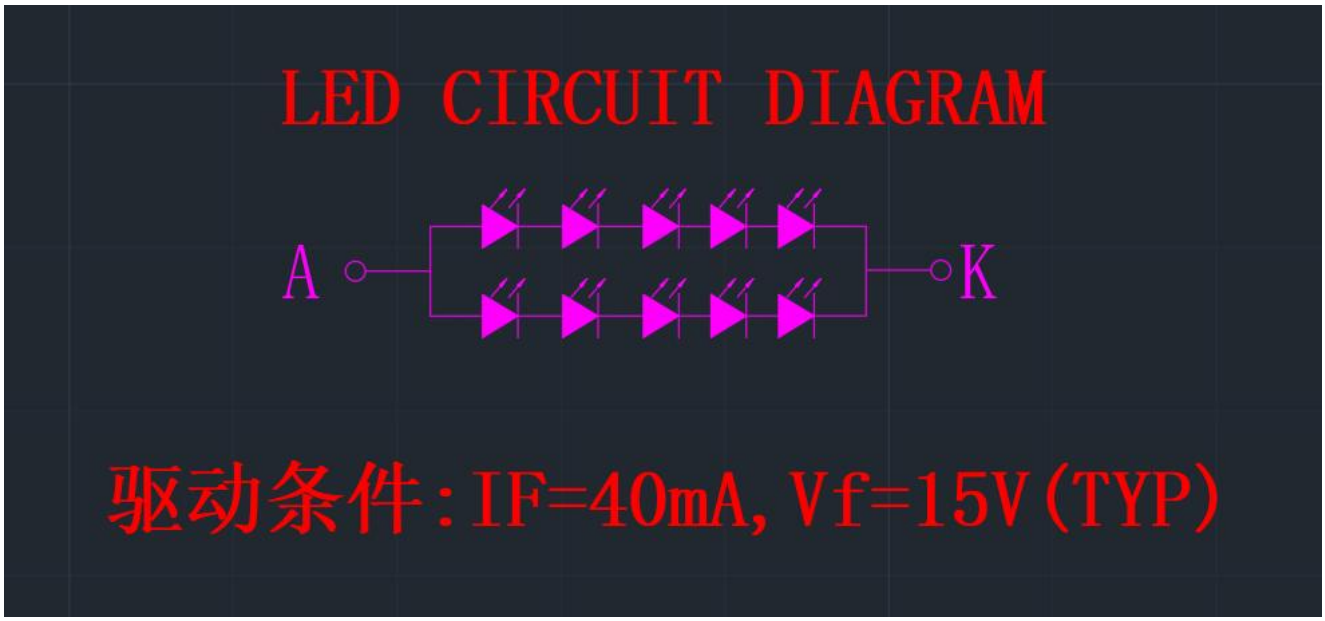
1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface.
2. Contrast measurements shall be made at viewing angle of θ= 0° and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (See FIGURE 1 shown in Appendix) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Center Luminance of white is defined as the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in FIGURE 4 for a total of the measurements per display.
4. The White luminance uniformity on LCD surface is then expressed as : ΔY = Minimum Luminance of 9 Points or 5 points / Maximum Luminance of 9 Points or 5 points(See FIGURE 2).
5. The color chromaticity coordinates specified in Table 5. shall be calculated from the spectral data measured with C light. Measurements shall be made at the center of the panel.
6. The electro-optical response time measurements shall be made as FIGURE 5 shown in Appendix by switching the “data” input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Td, and 90% to 10% is Tr.



Note(4) Backlight circuit



9.Records Of Version

Version	Revise Date	Page	Content
1.0	2026-3-22	ALL	New released