

PRODUCT SPECIFICATION **FOR LCD MODULE**

Revision: 1.0

Model No: LSL070I27-MP-V1

Module Type: COG+FPC+B/L+LENS

APPROVED SIGNATURE

- ☒ Approved Product Specification only
- ☐ Approved Product Specification and Samples

<u>Prepared By</u>	<u>Checked By</u>	<u>Approved By</u>

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1. General Description

LSL070I27-MP-V1 is a transmissive type a-Si TFT-LCD (amorphous silicon thin film transistor liquid crystal display) module, which is composed of a TFT-LCD panel, a driver circuit and a backlight unit. The panel size is 7.0 inch and the resolution is 1024(RGB)*600, the panel can display up to 16.7 M colors.

2. Physical Features

Display Mode	TFT-LCD Module
	Active matrix TFT, Transmissive type
Display Format	Graphic 1024(RGB)×600 Dot-matrix
Input Data	MIPI input
Viewing Direction (Grayscale Inversion)	Free (IPS)
Drive	JD9165BA

3. Mechanical Specification

Item	Specification	Unit
Module size (H×V×D)	178.2 ×111.9 ×4.35	mm
Number of dots	1024(RGB) × 600	pixel
Active area (H×V)	154.21×85.92	mm



5. Absolute Maximum Ratings

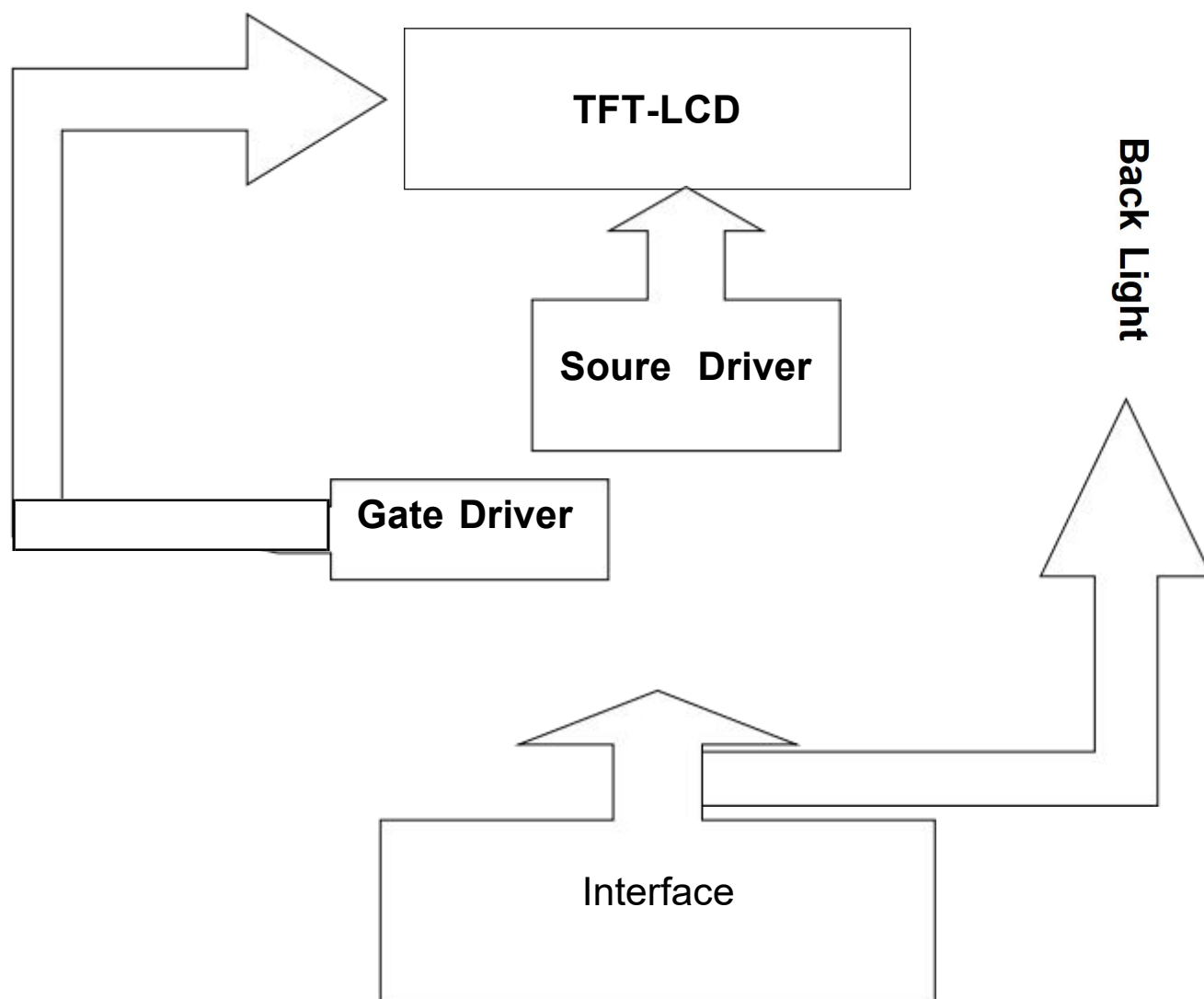
Item	Symbol	Min	Max	Unit	Remark
Supply voltage	VCC	-0.3	3.6	V	Note1 Note2
Operating temperature	TOPR	-20	70	°C	
Storage temperature	TSTR	-30	80	°C	

6. Electrical Characteristics

Item		Symbol	Rating			Unit	Remark
			Min	Typ	Max		
Supply voltage		VCC	2.8	3.3	3.6	V	Note1
Input Voltage	L level	VIL	VSS	---	0.3*VCC	V	
	H level	VIH	0.7*VCC	---	VCC	V	

7. Module Function Description

7- 1. Block Diagram Of LCM



7-2. Pin Description

PIN NO.	Symbol	I/O	Description
1	D0P	I/O	MIPI data input pin
2	D0N	I/O	MIPI data input pin
3	GND	P	ground.
4	D1P	I	MIPI data input pin
5	D1N	I	MIPI data input pin
6	GND	P	ground.
7	CLKP	I	MIPI clock input pin
8	CLKN	I	MIPI clock input pin
9	GND	P	ground.
10	D2P	I	MIPI data input pin
11	D2N	I	MIPI data input pin
12	GND	P	ground.
13	D3P	I	MIPI data input pin
14	D3N	I	MIPI data input pin
15	GND	P	ground.
16	LCD_EN_H	I	High-level for LCD startup, low-level for standby
17	BL_EN	I	BackLight ENable
18	LCD_RST	I	Global reset pin, active low
19	PWM	I	Backlight PWM signal, brightness control
20	VCC	P	power supply 3.3V
21	VCC	P	power supply 3.3V
22	NC		
23	NC		
24	NC		
25	NC		
26	VCC	P	power supply 3.3V
27	VCC	P	power supply 3.3V
28	BL_VIN	P	Backlight power supply 3.3V-5V
29	BL_VIN	P	Backlight power supply 3.3V-5V
30	BL_VIN	P	Backlight power supply 3.3V-5V

7-3 Timing Characteristics

Video Mode

Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the display image. Video information should only be transmitted using High Speed Mode.

Some Video Mode architectures may include a simple timing controller and partial line buffer, used to maintain a partial-screen or lower-resolution image in standby or Low Power Mode. This permits the interface to be shut down to reduce power consumption. To reduce complexity and cost, systems that only operate in Video Mode may use a unidirectional data path.

Virtual Channel Capability

While this specification only addresses the connection of a host processor to a single peripheral, DSI incorporates a virtual channel capability for communication between a host processor and multiple, physical display modules. Since interface bandwidth is shared between peripherals, there are constraints that limit the physical extent and performance of multiple-peripheral systems. The DSI protocol permits up to four virtual channels, enabling traffic for multiple peripherals to share a common DSI Link. The DSI specification makes no requirements on the specific value assigned to each virtual channel used to designate interlaced fields. For clarity, the first interlaced video field may be assigned as DI[7:6]=2'b00 and the second interlaced video field may be assigned DI[7:6]=2'b01.

8.3 DSI Format

Information is transferred between host processor and peripheral using one or more serial data signals and accompanying serial clock. The action of sending high-speed serial data across the bus is called a HS transmission or burst. Between transmissions, the differential data signal or Lane goes to a low-power state (LPS). Interfaces should be in LPS when they are not actively transmitting or receiving high-speed data. Figure 8.3 shows the basic structure of a HS transmission. N is the total number of bytes sent in the transmission.

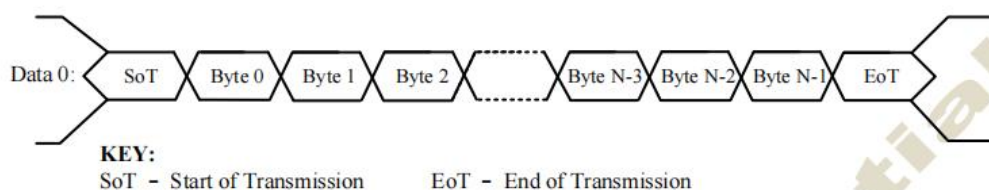


Figure 8.3: Basic HS Transmission Structure

Multi Lane Distribution and Merging

DSI is a Lane-scalable interface. Applications requiring more bandwidth than that provided by one Data Lane may expand the data path to two, three, or four Lanes wide and obtain approximately linear increases in peak bus bandwidth.

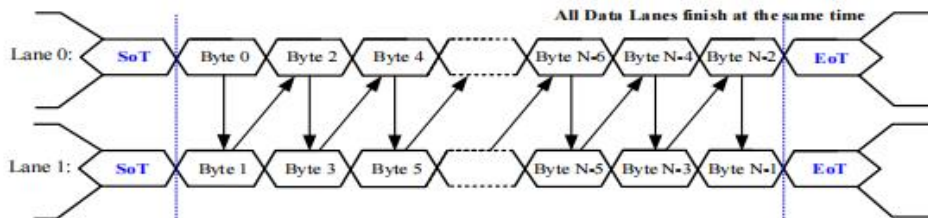
Multi-Lane implementations shall use a single common clock signal, shared by all Data Lanes. Conceptually, between the PHY and higher functional blocks is a layer that enables multi-Lane operation.

Since a HS transmission is composed of an arbitrary number of bytes that may not be an integer multiple of the number of Lanes, some Lanes may run out of data before others. Therefore, the Lane Management layer, as it buffers up the final set of less-than-N bytes, de-asserts its "valid data" signal into all Lanes for which there is no further data.

Although all Lanes start simultaneously with parallel Sots, each Lane operates independently and may complete the HS transmission before the other Lanes, sending an EoT one cycle (byte) earlier.

The N PHYs on the receiving end of the Link collect bytes in parallel and feed them into the Lane Management layer. The Lane Management layer reconstructs the original sequence of bytes in the transmission. Figure 8.4 & 8.5 illustrate a variety of ways a HS transmission can terminate for different number of Lanes and packet lengths.

Number of Bytes, N transmitted is an integer multiple of the number of lanes



Number of Bytes, N transmitted is NOT an integer multiple of the number of lanes

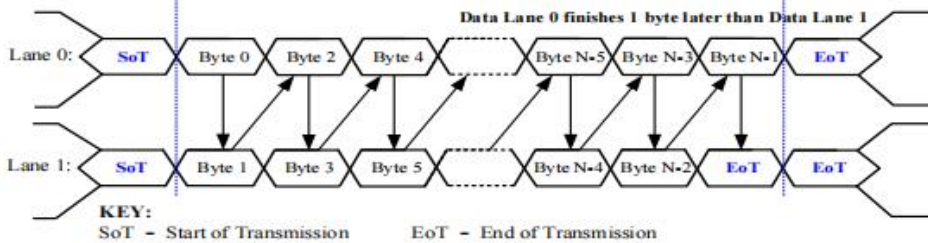
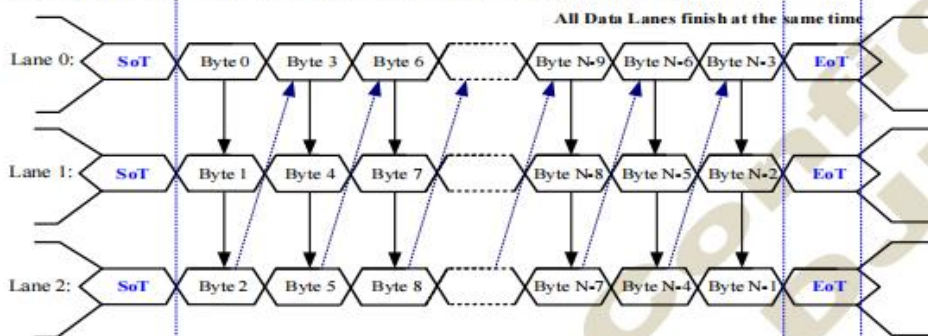
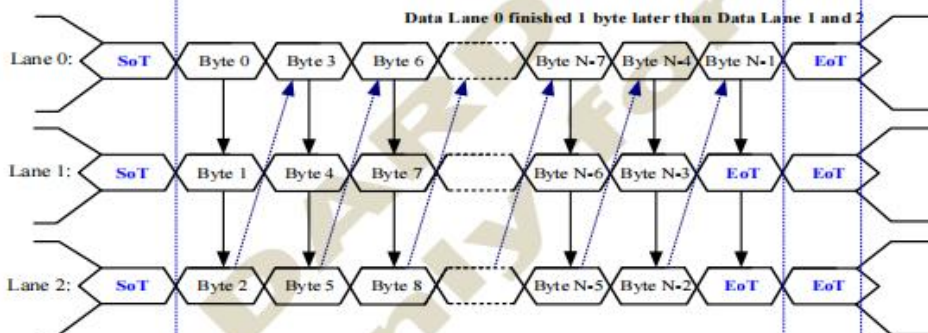


Figure 8.4: Two Lane HS Transmission Example

Number of Bytes, N transmitted is an integer multiple of the number of lanes



Number of Bytes, N transmitted is NOT an integer multiple of the number of lanes (Example 1):



Number of Bytes, N transmitted is NOT an integer multiple of the number of lanes (Example 2):

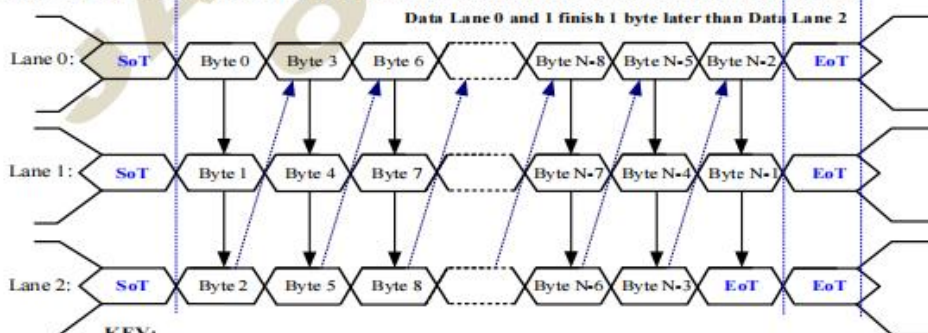


Figure 8.5: Three Lane HS Transmission Example

8. Electro-Optical Characteristics

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle range	Horizontal	Θ_3	CR > 10	-	85	-	Deg.	WV-Pol Note 1
		Θ_9		-	85	-	Deg.	
	Vertical	Θ_{12}		-	85	-	Deg.	
		Θ_6		-	85	-	Deg.	
Luminance Contrast ratio		CR	$\Theta = 0^\circ$	-	800	-		Note 2
Cell Transmittance		Tr		4.9%	5.45%	-	%	Base on 客户BLU Note 3
White Chromaticity		x_w		TYP. - 0.03	0.298	TYP. + 0.03		Note 4 Base on C Light
		y_w			0.337			
Reproduction of color (C light)	Red	R_x			0.633			
		R_y			0.341			
	Green	G_x			0.276			
		G_y			0.547			
	Blue	B_x			0.144			
		B_y			0.166			
Color Gamut (C light)					-	50	-	%
Response Time (Rising + Falling)		T_{RT}	Ta= 25° C $\Theta = 0^\circ$	-	30	40	ms	Note 5

Note :

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see FIGURE 5).
2. Contrast measurements shall be made at viewing angle of $\Theta = 0$ and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state . (see FIGURE 5) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Transmittance is the Value with Polarizer.
4. The color chromaticity coordinates specified in Table 6 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.
5. The electro-optical response time measurements shall be made as FIGURE 6 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is T_r , and 90% to 10% is T_d .

9. Inspection Standards

1. AQL(Acceptable Quality Level)

AQL of major and minor defect

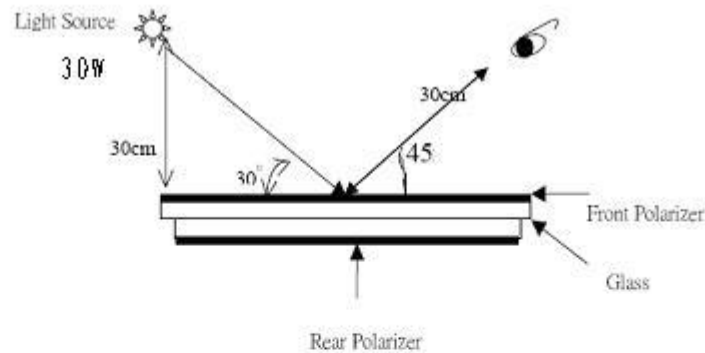
According to GB/T 2828-2003 ; , normal inspection, Class II

MAJOR DEFECT	MINOR DEFECT
0.65	1.5

2. Basic conditions for inspection

The LCM face to us, in normal environment, About an angle of incidence 30°, a distance of 30cm with normal eye, with an angle of 45° degree to check the products without uncovering the film!

(As shown below)

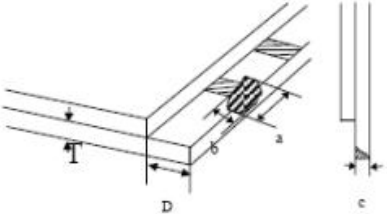
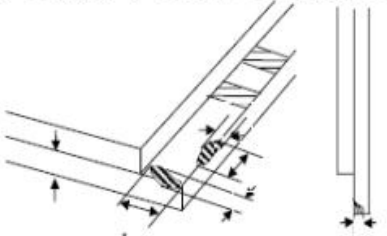


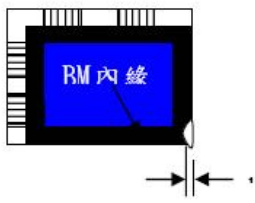
3. Inspection item and criteria

3.1 Visual inspection criterion in immobility

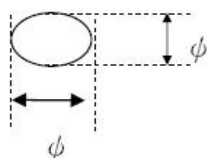
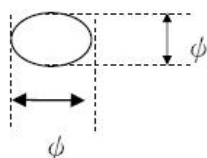
3.1.1 Glass defect

No	Defect item	Criteria	Remark
1	Dimension Unconformity (Major defect)	By Engineering Drawing	

No	Defect item	Criteria	Remark
2	Cracks (Major defect)	1.Linear cracks on panel 【Reject】 2. Nonlinear crack contrast by limited sample	
3	Glass extrude the conductive area (minor defect)	a: disregards and no influence assemblage 1) $b \leq 1/3$ Pin width(non bonding area) 【Accept】 2) bonding area $\leq 0.5\text{mm}$ 【Accept】	a:Length, b:Width
4	Pin-side , conductive area damaged (minor defect)	(a c : disregards) $b \leq 1/3$ of effective length for bonding electrode 【Accept】	a:Length, b: Width, c: Thickness  The diagram shows a cross-section of a glass substrate with a conductive layer. A rectangular area of the conductive layer is damaged, with dimensions a (length), b (width), and c (thickness) indicated. A vertical dimension T is also shown.
5	Pin-side , non-conductive area damaged (minor defect)	1) Damage area don't touch the ITO (Inclueing contraposition mark,except scribing mark) 【Accept】 2) $c < T$ $b \leq BM 1/3$ of width 【Accept】 3) $c = T$ b not touch the seal glue 【Accept】 4) a disregards	a:Length, b: Width, c: Thickness  The diagram shows a cross-section of a glass substrate with a conductive layer. A rectangular area of the non-conductive layer is damaged, with dimensions a (length), b (width), and c (thickness) indicated. A vertical dimension T is also shown.

No	Defect item	Criteria	Remark
6	Non-pin-side damage (minor defect)	$c < T$ 1) b exceeds 1/3 BM $c = T$ b not touch the seal glue 【Reject】 【Reject】	c : Thickness b: width of damage 

3.1.2 LCD appearance defect (View area)

No	Defect item	Criteria		Remark
1	Fiber 、 glass cratch 、 polarizer scratch/folded (minor defect)	Specification	Allowable	note1: L : Length , W : Width note2: disregard if out of AA 
		$0.05\text{mm} < W \leq 0.1\text{mm};$ $L \leq 3.0\text{mm}$	1	
		$W > 0.1\text{mm}; L > 3.0\text{mm}$	0	
2	Polarizer bubble 、 concave and convex (minor defect)	$\psi \leq 0.2\text{mm}$	disregard	note 1: $\psi = (L+W)/2$; L : Length , W : Width note2: disregard if out of AA 
		$0.2\text{mm} < \psi \leq 0.3\text{mm}$	2	
		$0.3\text{mm} < \psi \leq 0.5\text{mm}$	1	
		$0.5\text{mm} < \psi$	0	
3	Black dots 、 dirty dots 、 impurities 、 eyewinker (Major defect)	$\psi \leq 0.15\text{mm}$	disregard	note2: disregard if out of AA 
		$0.15\text{mm} < \psi \leq 0.25\text{mm}$	2	
		$0.25\text{mm} < \psi \leq 0.3\text{mm}$	1	
		$0.3\text{mm} < \psi$	0	
4	Polarizer prick (Major defect)	$\psi \leq 0.1\text{mm}$	disregard	note1: $\psi = (L+W)/2$; L= Length , W=Width note2: the distance between two dots > 5mm
		$0.1\text{mm} < \psi \leq 0.25\text{mm}$	3	
		$\psi > 0.25\text{mm}$	0	

3.1.3 .FPC

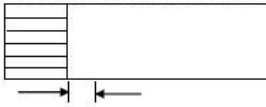
No	Defect item	Criteria		Remark
1	Copper screen peel (Major defect)	Copper screen peel 【 Reject】		
2	No release tape or peel (Major defect)	No release tape or peel 【 Reject】		
3	Dirty dot and impurity of FPC for customer using side (minor defect)	Specification	Allowable	note1: Cannot have stride ITO impurities
		$\psi \leq 0.25\text{mm}$	2	
		$\psi > 0.25$	0	

3.1.4 Black tape & Mara tape

1	FPC or H/S black tape shift (minor defect)	1.shift spec: 1)glue to the polarize 【 Reject】 2) IC bare 【 Reject】 2. left-and-right spec: 1) exceed of FPC edge or H-S edge 【 Reject】 2)IC bare 【 Reject】	
2	No black tape (Major defect)	No black tape 【 Reject】	
3	Tape position mistake (minor defect)	Not by engineering drawing 【 Reject】	
4	Mara tape defect (minor defect)	Peel before pulling the protecting film. 【 Reject】	

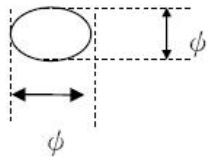
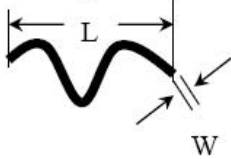
3.1.5 Silicon and Tuffy glue

No	Defect item	Criteria	Remark
1	Quantity of silicon (minor defect)	Uncover the ITO and circuit area. 【 Reject】	note: compared by engineering drawing.

No	Defect item	Criteria	Remark
2	Tuffy glue (minor defect)	1. Uncover the reveal copper area 【 Reject】 2. Cover layer 0.3mm(Min) ~ 3.0mm(Max) 【 accept】	note:if customer has special requirement , refer to the technical document. 
3	Depth of glue covering (minor defect)	Depth of glue covering overtop front Polarizer 【 Reject】	Except of the special requirement °

3.2 Electrical criteria

No	Defect item	Criteria	Remark
1	No display (Major defect)	No display 【 Reject】	
2	Missing line (Major defect)	Missing line 【 Reject】	
3	Seg-com light and dark (Major defect)	Seg-com light and dark 【 Reject】	ND filter 2% test
4	No display in immobility (Major defect)	No display in immobility 【 Reject】	
5	Flicker of Pattern (Major defect)	Flicker of Pattern 【 Reject】	
6	Mura (Major defect)	ND filter 2% test	
7	Over current (Major defect)	Over current 【 Reject】	
8	Voltage out of specification (Major defect)	Voltage out of specification 【 Reject】	
9	Pattern blur ,error code (Major defect)	Pattern blur ,error code 【 Reject】	
10	Dark light, Flicker (Major defect)	Dark light, Flicker 【 Reject】	

No	Defect item	Criteria	Remark	
11	Black/White dots 、 Dirty dots 、 eyewinker (Major defect)	Specification	Allowable	Note1: disregard if out of AA 
		$\psi \leq 0.15\text{mm}$	disregard	
		$0.15\text{mm} < \psi \leq 0.25\text{mm}$	2	
		$0.25\text{mm} < \psi \leq 0.3\text{mm}$	1	
		$0.3\text{mm} < \psi$	0	
12	Fiber 、 glass cratch 、 polarizer scratch/folded (minor defect)	$W \leq 0.03\text{mm}$	disregard	note1: L : Length 、 W : Width note2: disregard if out of AA 
		$0.03\text{mm} < W \leq 0.05\text{mm} ;$ $L \leq 3.0\text{mm}$	2	
		$0.05\text{mm} < W \leq 0.1\text{mm} ;$ $L \leq 3.0\text{mm}$	1	
		$W > 0.1\text{mm} ; L > 3.0\text{mm}$	0	

10.Records Of Version

Version	Revise Date	Page	Content
00	2026-7-22	all	New released