

PRODUCT SPECIFICATION **FOR LCD MODULE**

Revision: 1.0`

Model No: LS028T12-M-V1

Module Type: COG+FPC+B/L

APPROVED SIGNATURE

- Approved Product Specification only
- Approved Product Specification and Samples

<u>Prepared By</u>	<u>Checked By</u>	<u>Approved By</u>

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1. General Description

LS028T12-M-V1 is a transmissive type a-Si TFT-LCD (amorphous silicon thin film transistor liquid crystal display) module, which is composed of a TFT-LCD panel, a driver circuit and a backlight unit. The panel size is 2.8 inch and the resolution is 240(RGB)*320, the panel can display up to 262k colors.

2. Physical Features

Display Mode	TFT-LCD Module
	Active matrix TFT, Transmissive type
Display Format	Graphic 240(RGB)×320 Dot-matrix
Input Data	8bit 8080 /SPI
Viewing Direction (Grayscale Inversion)	TN
Drive	ST7789P3

3. Mechanical Specification

Item	Specification	Unit
Module size (H×V×D)	50.0 ×69.1 ×2.3	mm
Number of dots	240(RGB) ×320	pixel
Active area (H×V)	43.2×57.6	mm



5. Absolute Maximum Ratings

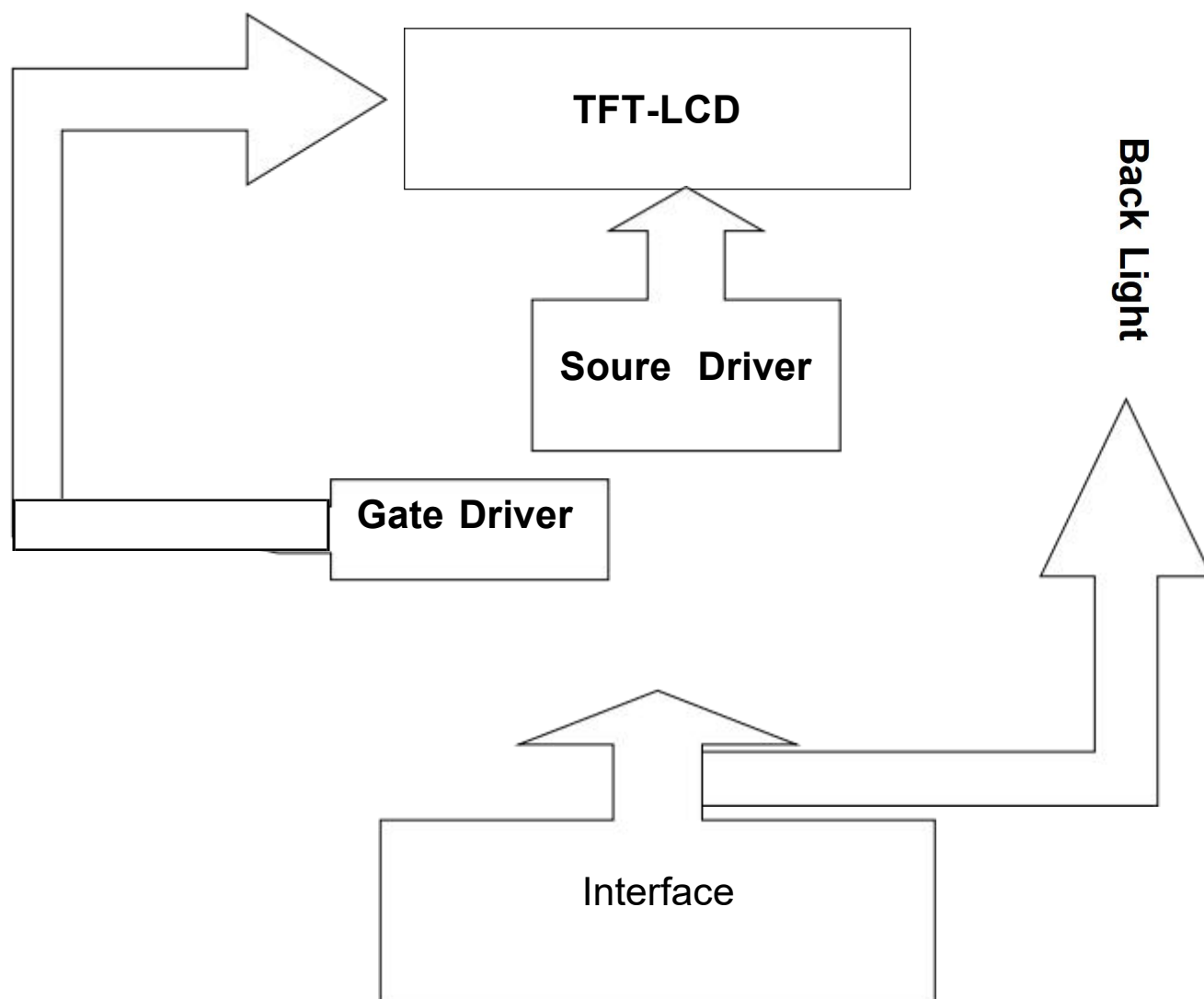
Item	Symbol	Min	Max	Unit	Remark
Supply voltage	VCC	-0.3	4.6	V	Note1 Note2
Supply voltage	IOVCC	-0.3	4.6	V	
Operating temperature	TOPR	-20	70	°C	
Storage temperature	TSTR	-30	80	°C	

6. Electrical Characteristics

Item		Symbol	Rating			Unit	Remark
			Min	Typ	Max		
Supply voltage		VCC	2.4	2.75	3.3	V	Note1
Supply voltage		IOVCC	1.65	1.8	3.3	V	
Input Voltage	L level	VIL	0	---	0.3*IOVCC	V	
	H level	VIH	0.7*IOVCC	---	IOVCC	V	

7. Module Function Description

7- 1. Block Diagram Of LCM



7-2. Pin Description

PIN NO.	Symbol	I/O	Description
1	GND		Ground
2	LEDK		Power for LED backlight cathode
3	LEDA		Power for LED backlight anode
4	GND		Ground
5	VDD2.8V		Power Supply
6	WR		Write enable in MCU parallel interface. - Display data/command selection pin in 4-line serial interface. - Second Data lane in 2 data lane serial interface. -If not used, please fix this pin at VDDI or DGND.
7	RD		Read enable in 8080 MCU parallel interface. -If not used, please fix this pin at VDDI or DGND.
8	CS		Chip selection pin . Low enable. High disable
9	RS		-Display data/command selection pin in parallel interface. -This pin is used to be serial interface clock.(SCL) DCX='1': display data or parameter. DCX='0': command data. -If not used, please fix this pin at VDDI or DGND.
10	SDA		-When IM3: Low, SPI interface input/output pin. -When IM3: High, SPI interface input pin. -The data is latched on the rising edge of the SCL signal. -If not used, please fix this pin at VDDI or DGND level.
11	DB0		parallel interface data bus
12	DB1		parallel interface data bus
13	DB2		parallel interface data bus
14	DB3		parallel interface data bus
15	DB4		parallel interface data bus
16	DB5		parallel interface data bus
17	DB6		parallel interface data bus
18	DB7		parallel interface data bus
19	RESET		This signal will reset the device and it must be applied to properly initialize the chip.

20	VDD2.8V		Power Supply																																																																																				
21	IM0		<table><tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>MPU Interface Mode</th><th>Data pin</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>80-8bit parallel I/F</td><td>DB[7:0]</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td>22</td><td>IM1</td><td></td><td><table><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>3-line 9bit serial I/F</td><td>SDA: in/out</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td></tr></table></td></tr><tr><td>23</td><td>IM2</td><td></td><td><table><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>2 data lane serial I/F</td><td>SDA: in/out WRX: in</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td></tr></table></td></tr><tr><td>24</td><td>GND</td><td></td><td>Ground</td></tr></table>	IM3	IM2	IM1	IM0	MPU Interface Mode	Data pin	0	0	0	0	80-8bit parallel I/F	DB[7:0]													22	IM1		<table><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>3-line 9bit serial I/F</td><td>SDA: in/out</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td></tr></table>	0	1	0	1	3-line 9bit serial I/F	SDA: in/out																			23	IM2		<table><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>2 data lane serial I/F</td><td>SDA: in/out WRX: in</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td></tr></table>	0	1	0	1	2 data lane serial I/F	SDA: in/out WRX: in																			24	GND		Ground
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	T_{DHT}	Data hold time	TBD	-	ns
	T_{RAT}	Read access time (ID)	-	TB-D	ns
	T_{RATFM}	Read access time (FM)	-	TBD	ns
	T_{ODH}	Output disable time	TBD	TBD	ns

Table 4 8080 Parallel Interface Characteristics

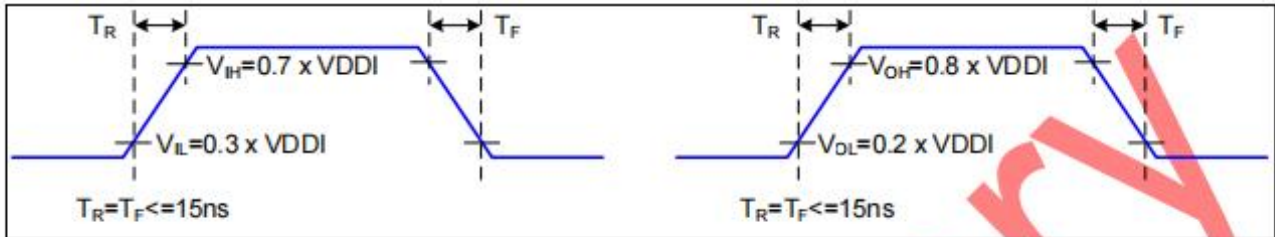


Figure 2 Rising and Falling Timing for I/O Signal

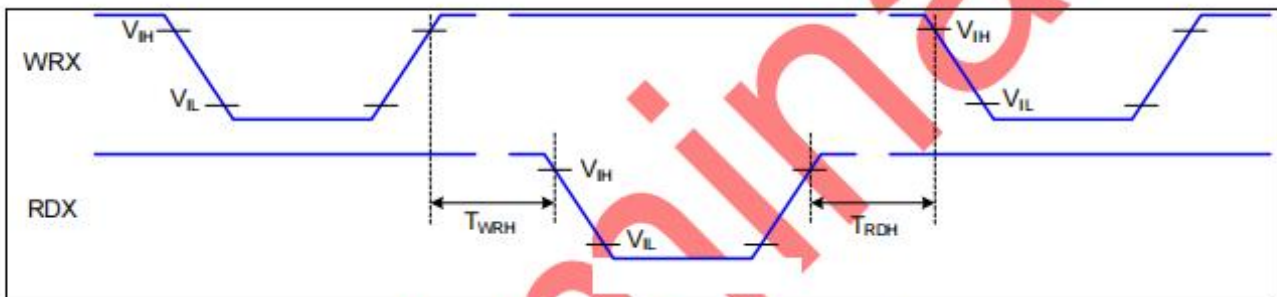


Figure 3 Write-to-Read and Read-to-Write Timing

Note: The rising time and falling time (T_r , T_f) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

7.4.2 Serial Interface Characteristics (3-line serial):

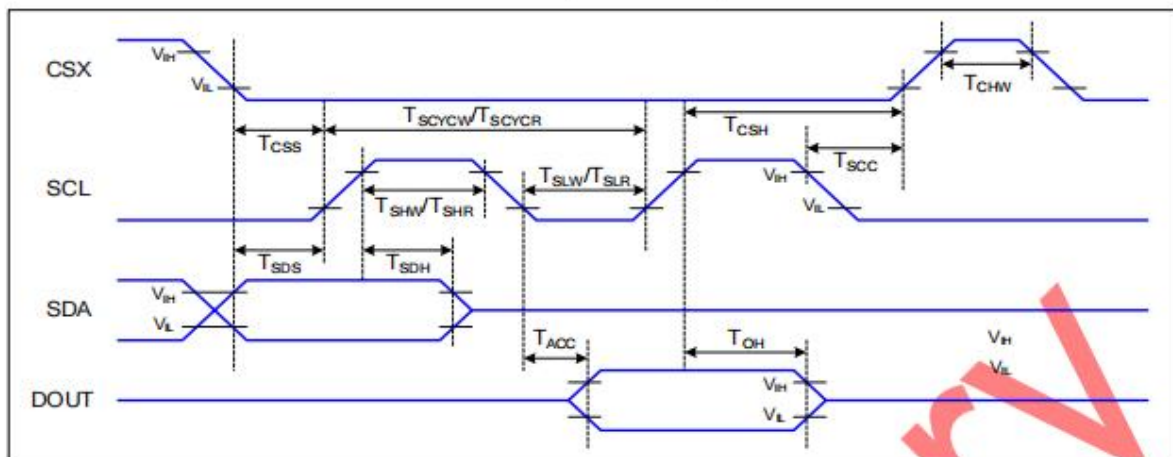


Figure 4 3-line serial Interface Timing Characteristics

$V_{DDI}=1.65$ to $3.3V$, $V_{DD}=2.4$ to $3.3V$, $AGND=DGND=0V$, $T_a=25^{\circ}C$

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	TBD	-	ns	
	T_{CSH}	Chip select hold time (write)	TBD	-	ns	
	T_{CSS}	Chip select setup time (read)	TBD	-	ns	
	T_{SCC}	Chip select hold time (read)	TBD	-	ns	
	T_{CHW}	Chip select "H" pulse width	TBD	-	ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	TBD	-	ns	
	T_{SHW}	SCL "H" pulse width (Write)	TBD	-	ns	
	T_{SLW}	SCL "L" pulse width (Write)	TBD	-	ns	
	T_{SCYCR}	Serial clock cycle (Read)	TBD	-	ns	
	T_{SHR}	SCL "H" pulse width (Read)	TBD	-	ns	
	T_{SLR}	SCL "L" pulse width (Read)	TBD	-	ns	
SDA (DIN)	T_{SDS}	Data setup time	TBD	-	ns	
	T_{SDH}	Data hold time	TBD	-	ns	
DOUT	T_{ACC}	Access time	TBD	TBD	ns	For maximum CL=30pF
	T_{OH}	Output disable time	TBD	TBD	ns	For minimum CL=8pF

Table 5 3-line serial Interface Characteristics

Note1 : The rising time and falling time (T_r , T_f) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of V_{DDI} for Input signals.

Note2 : In the read sequence of Serial interface, the 500nsec delay time is needed between read command and first read clock.

7.4.3 Serial Interface Characteristics (4-line serial):

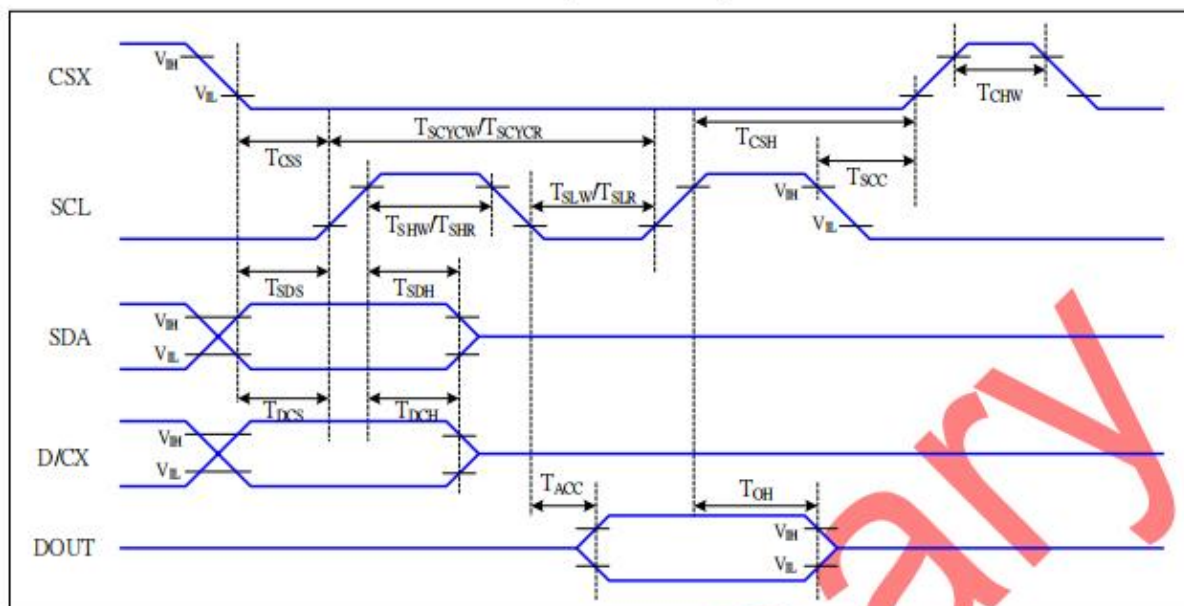


Figure 5 4-line serial Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25°C

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T _{CSS}	Chip select setup time (write)	TBD	-	ns	
	T _{CSH}	Chip select hold time (write)	TBD	-	ns	
	T _{CSS}	Chip select setup time (read)	TBD	-	ns	
	T _{SCC}	Chip select hold time (read)	TBD	-	ns	
	T _{CHW}	Chip select "H" pulse width	TBD	-	ns	
SCL	T _{SCYCW}	Serial clock cycle (Write)	TBD	-	ns	-write command & data ram
	T _{SHW}	SCL "H" pulse width (Write)	TBD	-	ns	
	T _{SLW}	SCL "L" pulse width (Write)	TBD	-	ns	
	T _{SCYCR}	Serial clock cycle (Read)	TBD	-	ns	-read command & data ram
	T _{SHR}	SCL "H" pulse width (Read)	TBD	-	ns	
	T _{SLR}	SCL "L" pulse width (Read)	TBD	-	ns	
D/CX	T _{DCS}	D/CX setup time	TBD	-	ns	
	T _{DCH}	D/CX hold time	TBD	-	ns	
SDA (DIN)	T _{SDS}	Data setup time	TBD	-	ns	
	T _{SDH}	Data hold time	TBD	-	ns	
DOUT	T _{ACC}	Access time	TBD	TBD	ns	For maximum CL=30pF
	T _{OH}	Output disable time	TBD	TBD	ns	For minimum CL=8pF

Table 6 4-line serial Interface Characteristics

Note1 : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

7.4.5 Reset Timing:

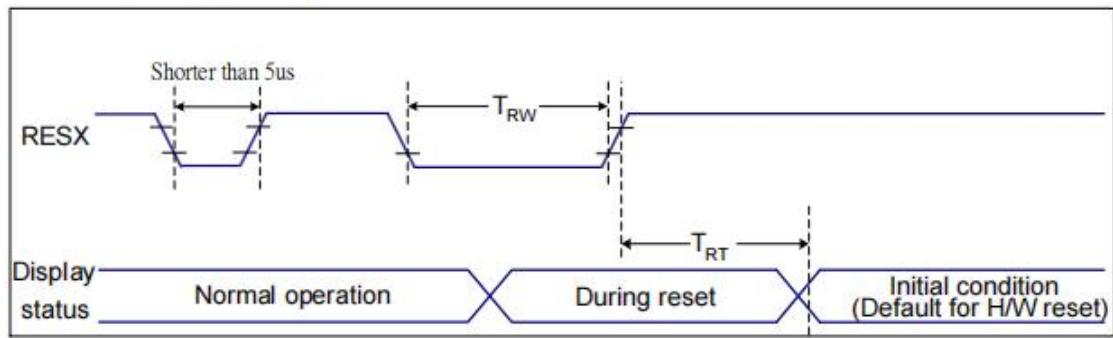


Figure 7 Reset Timing

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25 °C

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5) 120 (Note 1, 6, 7)	ms

Table 9 Reset Timing

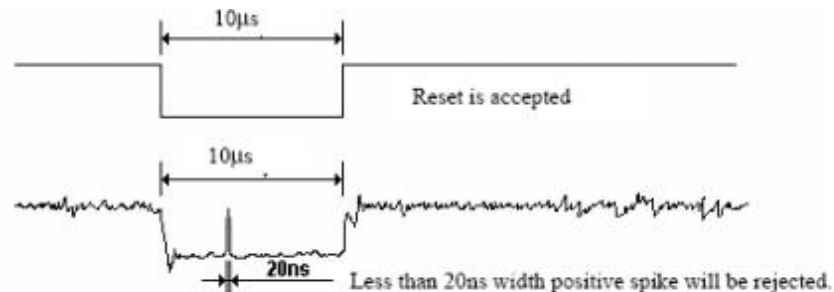
Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

8. Electro-Optical Characteristics

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time		Tr +Tf	$\theta_x = \theta_y = 0$	---	16	--	ms	Note 1
Contrast Ratio		CR		--	500	---	---	Note 2
Transmittance		T%		--	6.4	---	%	
Color Chromaticity (CIE1931)	White	W x	$\theta_x = \theta_y = 0$	---	0.301	---	---	
		W y		---	0.337	---	---	
Viewing angle	θ_T		CR > 10	35	45	---	Deg.	Note 3
	θ_B			35	45	---		
	θ_L			35	50	---		
	θ_R			20	20	---		
Luminance ($I_F = 80mA$)		L		---	350	---	cd/m2	Note4

Note 1: Ambient temperature = 25°C.

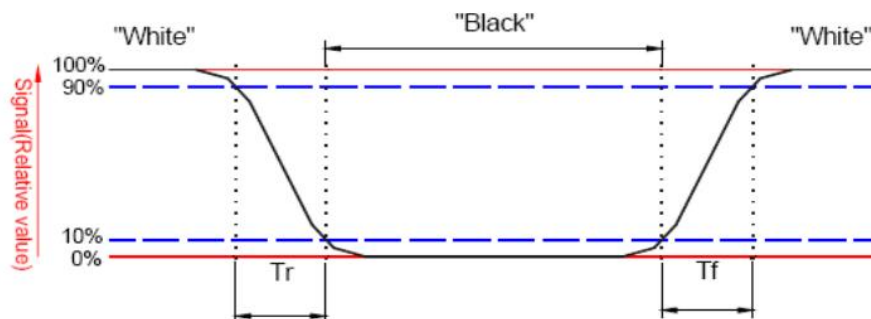
Note 2: To be measured with a viewing cone of 2° by Topcon luminance meter BM-5A.

Note 3: To be measured with Otsuta chromaticity meter LCF-2100M, CF only measure under C light simulation.

Note 4: CTC shipping status is cell without polarizer. Transmittance of Specification is cell with polarizer.
The tolerance of Transmittance is $\pm 10\%$.

Note 5: Definition of response time:

The output signals of TRD-100 are measured when the input signals are changed to "White" (falling time) and from "White" to "Black" (rising time), respectively. The interval is between the 10% and 90% of amplitudes. Refer to figure as below.

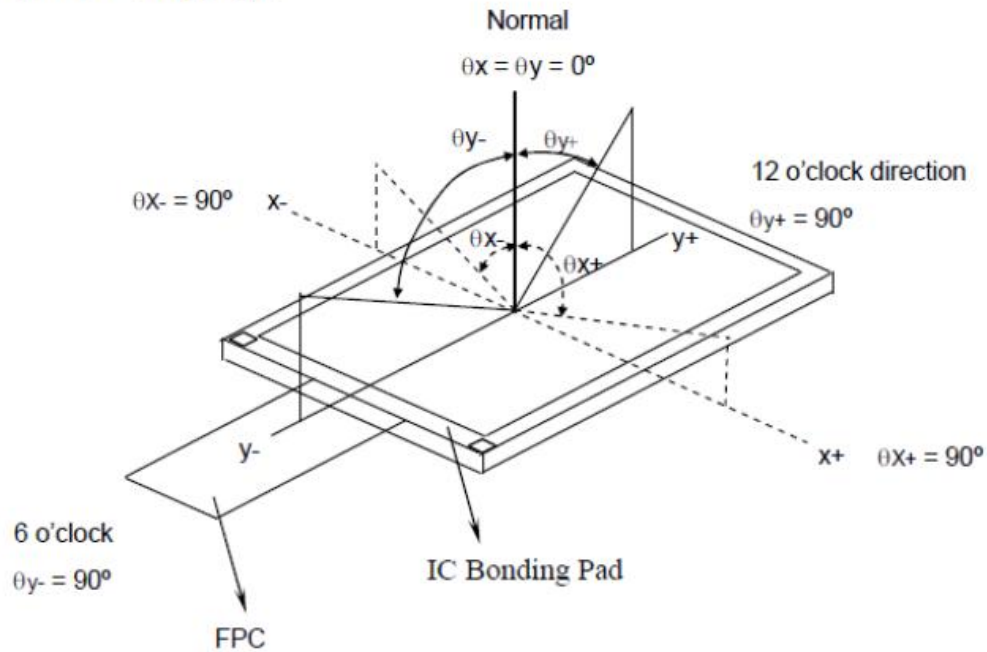


Note 6: Definition of contrast ratio:

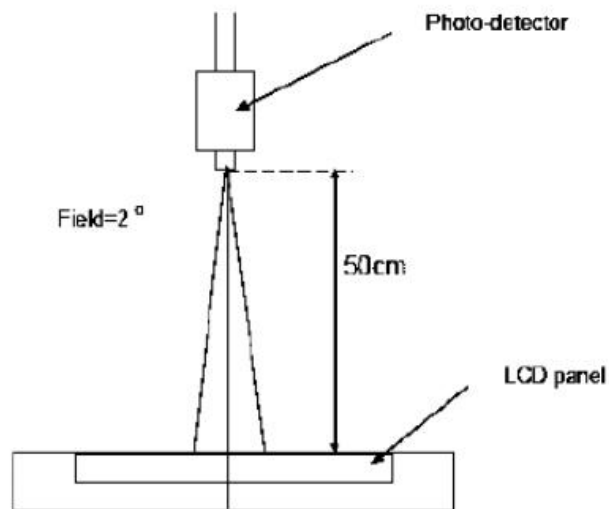
Contrast ratio is calculated by the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "white" state}}{\text{Brightness on the "black" state}}$$

Note 7: Definition of viewing angle

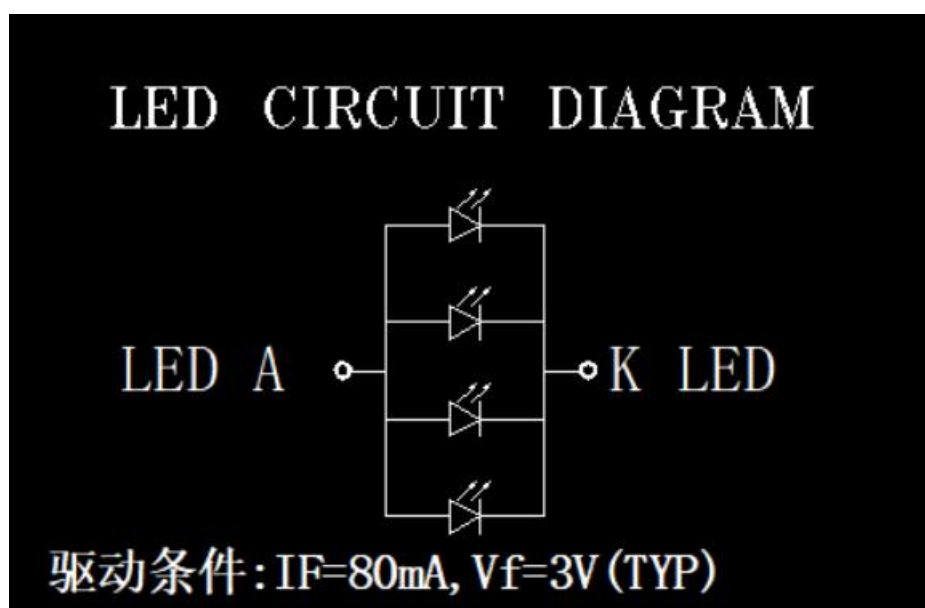


Note 8: Optical characteristic measurement setup.



Note 9:

Note(4) Backlight circuit



9.Records Of Version

Version	Revise Date	Page	Content
00	2025-8-12	ALL	New released