

PRODUCT SPECIFICATION **FOR LCD MODULE**

Revision: 1.0

Model No: LS028T38-M-V1

Module Type: COG+FPC+B/L

APPROVED SIGNATURE

- ☒ Approved Product Specification only
- ☐ Approved Product Specification and Samples

<u>Prepared By</u>	<u>Checked By</u>	<u>Approved By</u>

Contents

目录

1. General Description	3
2. Physical Features	3
3. Mechanical Specification	3
4. Outline Dimension	4
5. Absolute Maximum Ratings	5
6. Electrical Characteristics	5
7. Module Function Description	6
8. Electro-Optical Characteristics	12
9. Records Of Version	15

1. General Description

LS028T38-M-V1 is a transmissive type a-Si TFT-LCD (amorphous silicon thin film transistor liquid crystal display) module, which is composed of a TFT-LCD panel, a driver circuit and a backlight unit. The panel size is 2.8 inch and the resolution is 240(RGB)*320, the panel can display up to 262k colors.

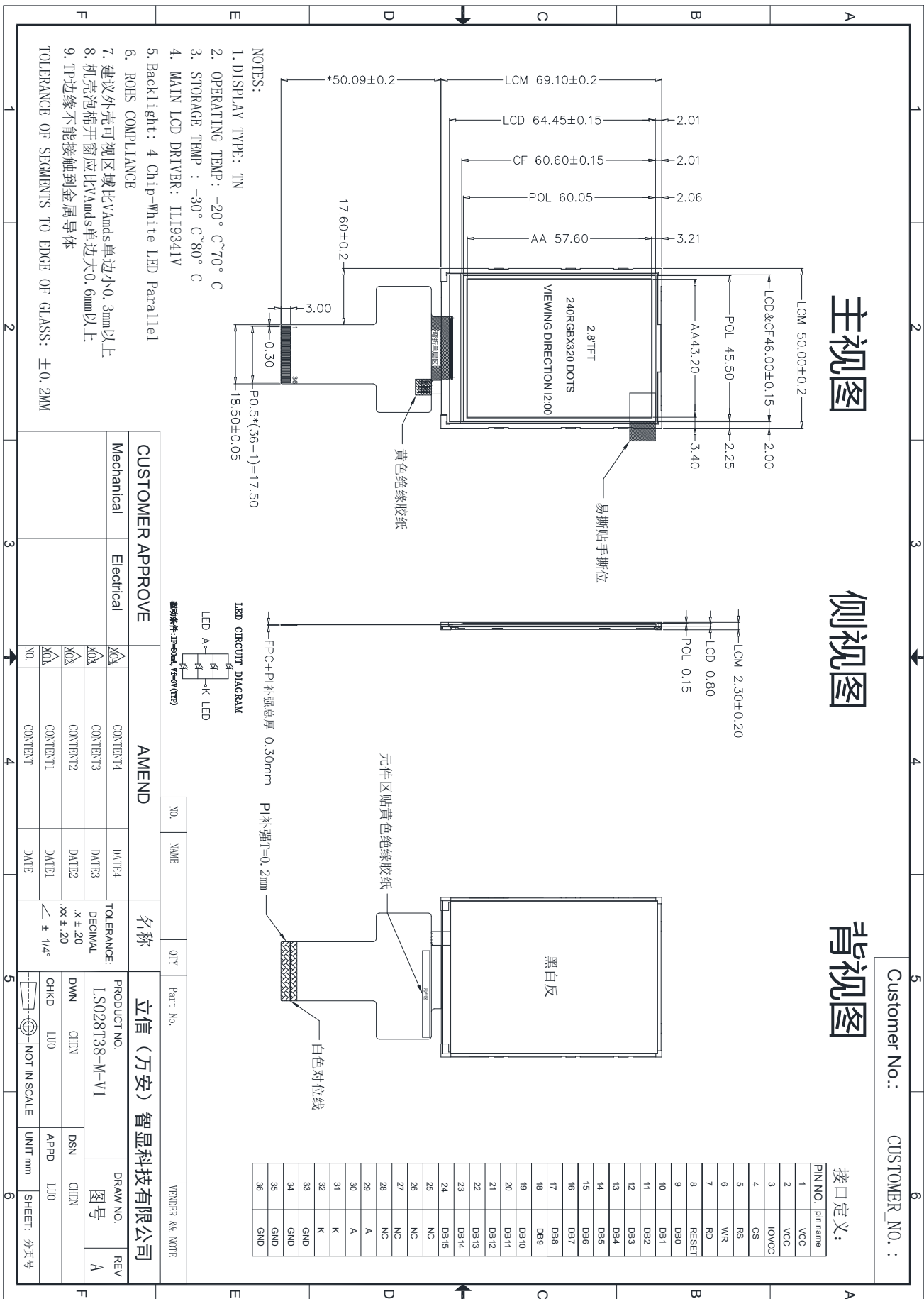
2. Physical Features

Display Mode	TFT-LCD Module
	Active matrix TFT, Transmissive type
Display Format	Graphic 240(RGB)×320 Dot-matrix
Input Data	16bit 8080
Viewing Direction (Grayscale Inversion)	TN
Drive	ILI9341V

3. Mechanical Specification

Item	Specification	Unit
Module size (H×V×D)	50.0×69.1×2.3	mm
Number of dots	240(RGB) × 320	pixel
Active area (H×V)	43.2×57.6	mm

4. Outline Dimension



5. Absolute Maximum Ratings

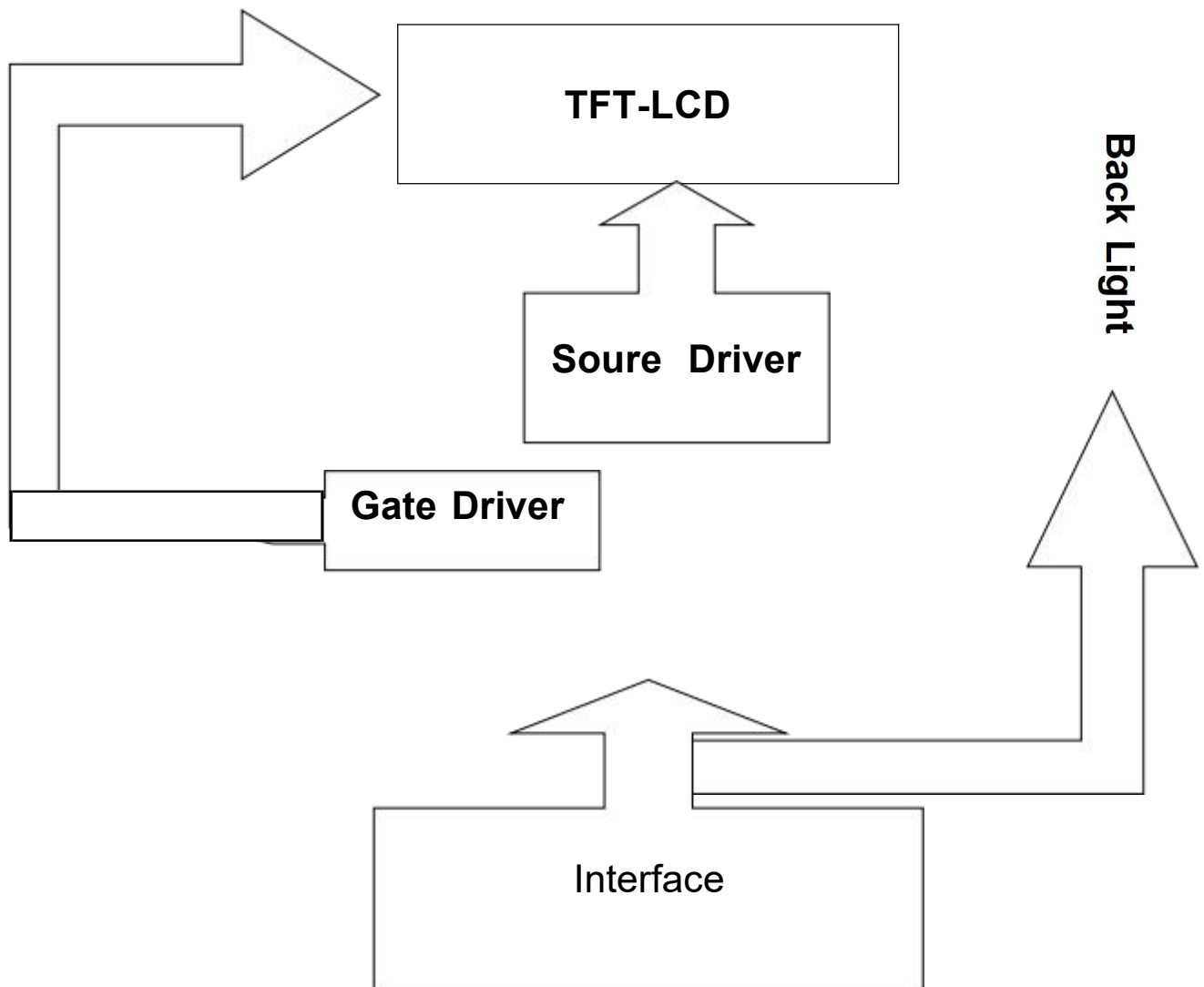
Item	Symbol	Min	Max	Unit	Remark
Supply voltage	VCC	-0.3	4.6	V	Note1 Note2
Supply voltage	IOVCC	-0.3	4.6	V	
Operating temperature	TOPR	-20	70	°C	
Storage temperature	TSTR	-30	80	°C	

6. Electrical Characteristics

Item		Symbol	Rating			Unit	Remark
			Min	Typ	Max		
Supply voltage		VCC	2.5	2.8	3.3	V	Note1
Supply voltage		IOVCC	1.65	2.8	3.3	V	
Input Voltage	L level	VIL	0	---	0.3*IOVCC	V	
	H level	VIH	0.7*IOVCC	---	IOVCC	V	

7. Module Function Description

7- 1. Block Diagram Of LCM



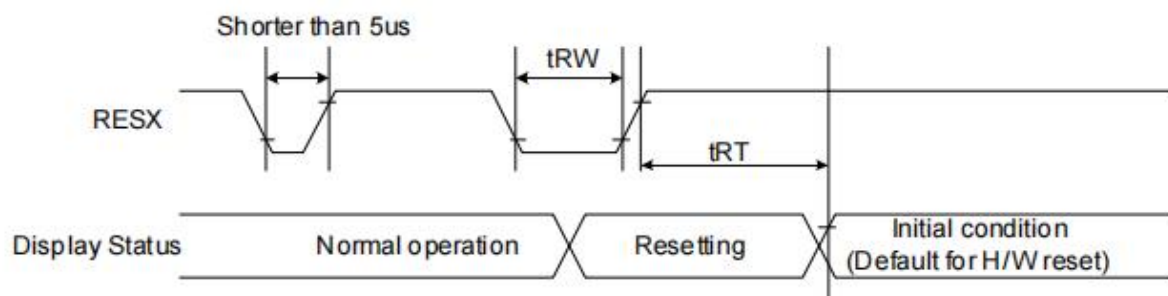
7-2. Pin Description

PIN NO.	Symbol	I/O	Description
1	VCC	P	power supply
2	VCC	P	power supply
3	IOVCC	P	power supply
4	CS	I	Chip select input pin
5	RS	I	This pin is used to select “Data or Command” in the parallel interface. When DCX = 1, data is selected. When DCX = 0, command is selected.
6	WR	I	8080- /8080 I - II system: Serves as a write signal and writes data at the rising edge.
7	RD	I	8080- /8080 I - II system (RDX): Serves as a read signal and MCU read data at the rising edge.
8	RESET	I	This signal will reset the device and must be applied to properly initialize the chip.
9	D0	I	data bus
10	D1	I	data bus
11	D2	I	data bus
12	D3	I	data bus
13	D4	I	data bus
14	D5	I	data bus
15	D6	I	data bus
16	D7	I	data bus
17	D8	I	data bus
18	D9	I	data bus
19	D10	I	data bus
20	D11	I	data bus
21	D12	I	data bus
22	D13	I	data bus
23	D14	I	data bus
24	D15	I	data bus
25	NC		

26	NC		
27	NC		
28	NC		
29	A	P	Power for LED backlight anode
30	A	P	Power for LED backlight anode
31	K	P	Power for LED backlight cathode
32	K	P	Power for LED backlight cathode
33	GND	P	Ground
34	GND	P	Ground
35	GND	P	Ground
36	GND	P	Ground

7-3 Timing Characteristics

15.4. Reset Timing



Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

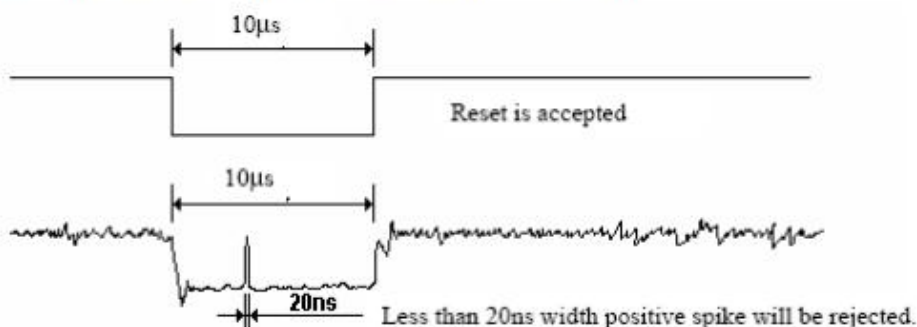
Note 1: The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NV memory to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

Note 2: Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below: -

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

Note 3: During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In -mode.) And then return to Default condition for Hardware Reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:



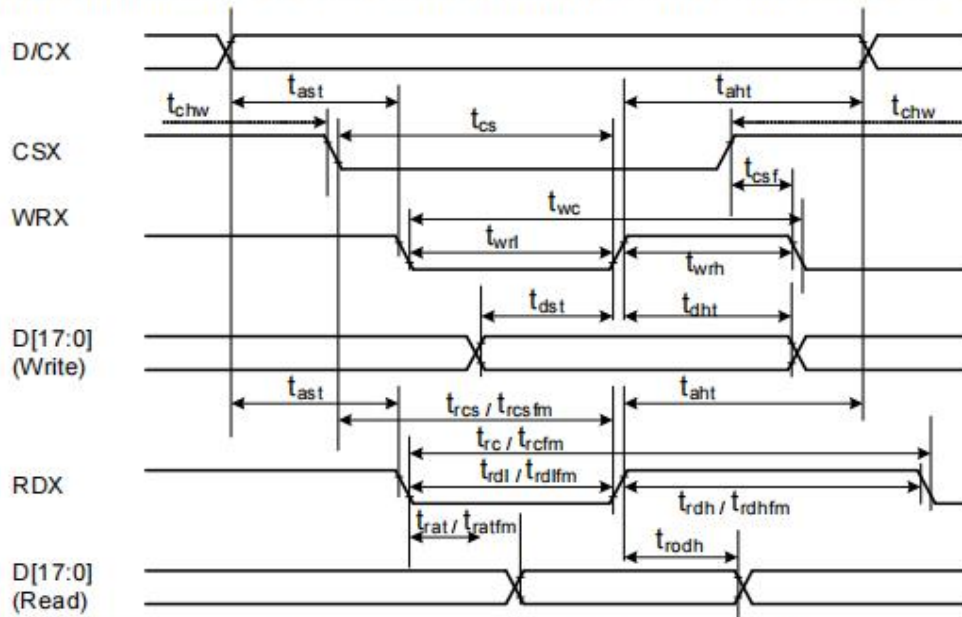
Note 5: When Reset applied during Sleep In Mode.

Note 6: When Reset applied during Sleep Out Mode.

Note 7: It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

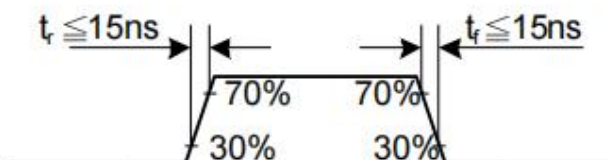
18.3 AC Characteristics

18.3.1 Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080- I system)

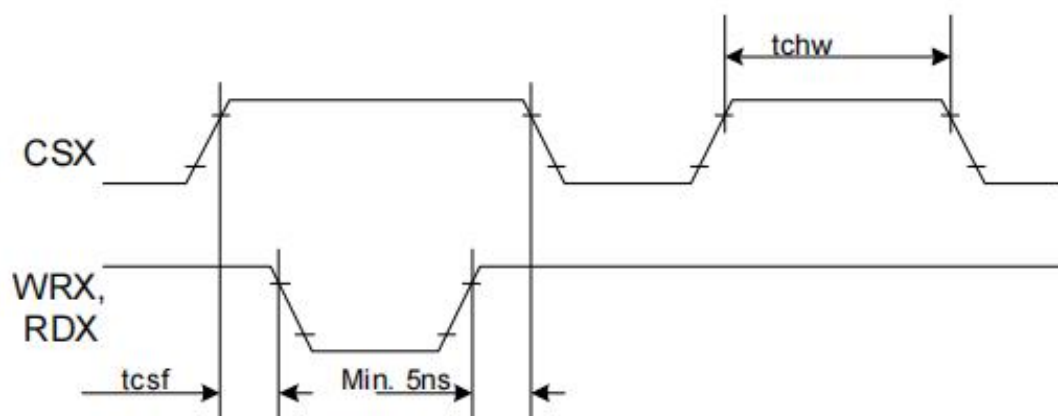


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0], D[15:0], D[8:0], D[7:0]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note: $T_a = -30$ to $70\text{ }^{\circ}\text{C}$, $V_{DDI}=1.65\text{V}$ to 3.3V , $V_{CI}=2.5\text{V}$ to 3.3V , $V_{SS}=0\text{V}$

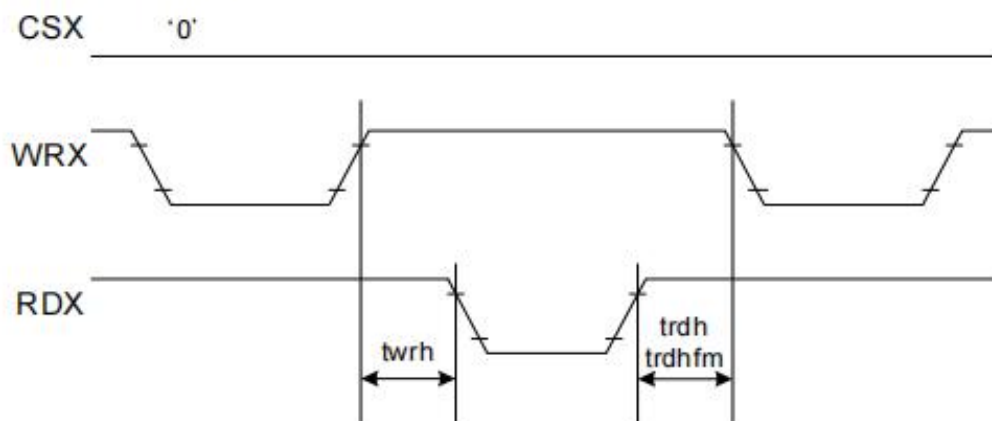


CSX timings :



Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:



Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

8. Electro-Optical Characteristics

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time		Tr +Tf	$\theta_x = \theta_y = 0$	---	16	--	ms	Note 1
Contrast Ratio		CR		---	500	---	---	Note 2
Transmittance		T%		---	6.4	---	%	
Color Chromaticity (CIE1931)	White	W x	$\theta_x = \theta_y = 0$	---	0.301	---	---	
		W y		---	0.337	---	---	
Viewing angle	θ_T		CR > 10	---	50	---	Deg.	Note 3
	θ_B			---	20	---		
	θ_L			---	45	---		
	θ_R			---	45	---		

Note 1: Ambient temperature = 25°C.

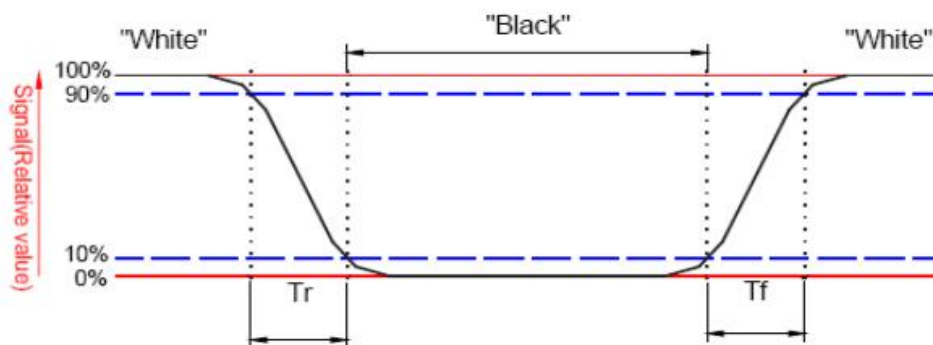
Note 2: To be measured with a viewing cone of 2° by Topcon luminance meter BM-5A.

Note 3: To be measured with Otsuta chromaticity meter LCF-2100M, CF only measure under C light simulation.

Note 4: CTC shipping status is cell without polarizer. Transmittance of Specification is cell with polarizer. The tolerance of Transmittance is $\pm 10\%$.

Note 5: Definition of response time:

The output signals of TRD-100 are measured when the input signals are changed to "White" (falling time) and from "White" to "Black" (rising time), respectively. The interval is between the 10% and 90% of amplitudes. Refer to figure as below.

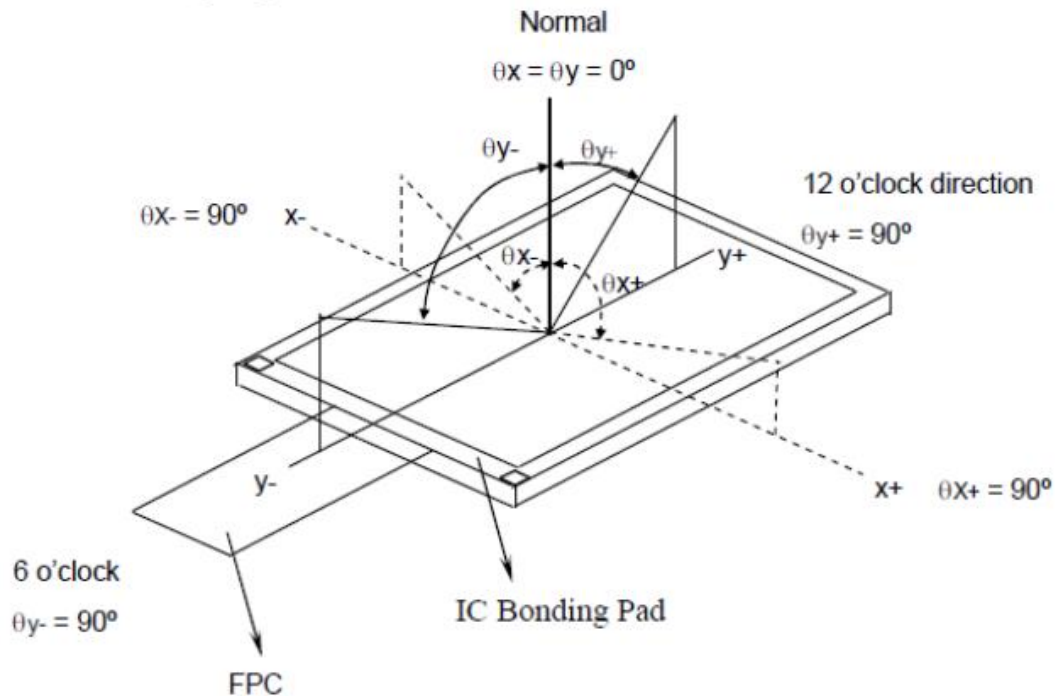


Note 6: Definition of contrast ratio:

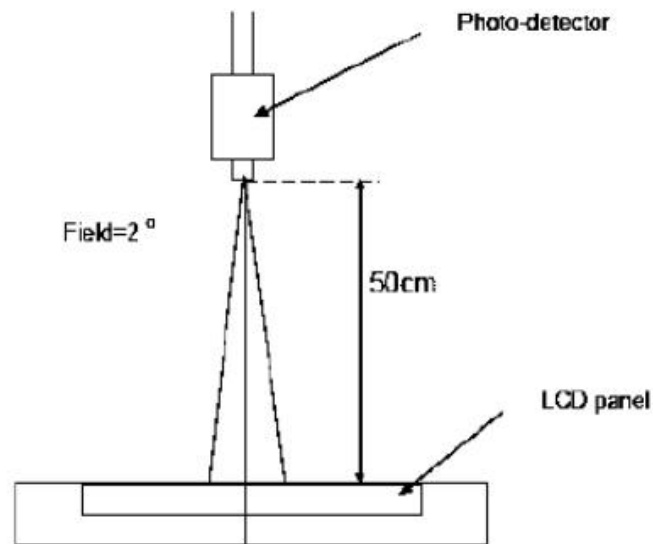
Contrast ratio is calculated by the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "white" state}}{\text{Brightness on the "black" state}}$$

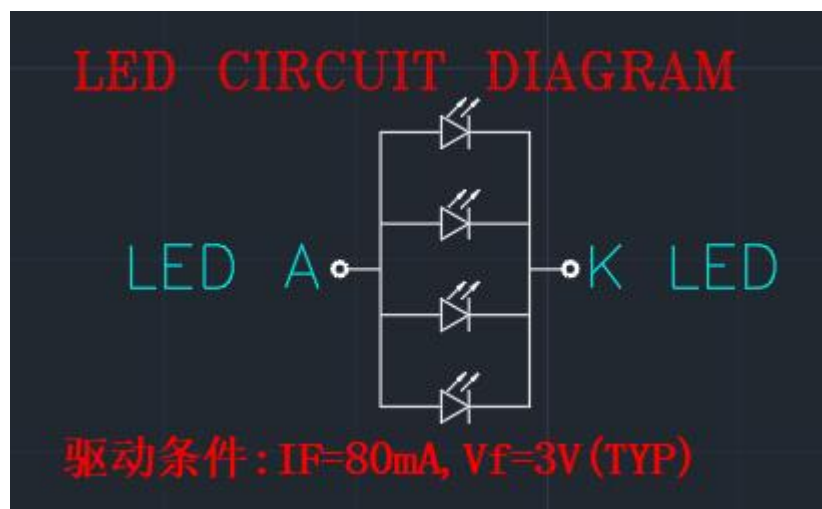
Note 7: Definition of viewing angle



Note 8: Optical characteristic measurement setup.



Note(4) Backlight circuit



9.Records Of Version

Version	Revise Date	Page	Content
00	2026-5-11	ALL	New released