PRODUCT SPECIFICATION FOR LCD MODULE

Revision: 1.0

Model No: LS028I15-R-V1

Module Type: COG+FPC+B/L

APPROVED SIGNATURE

■ Approved Product Specification only

□ Approved Product Specification and Samples

Prepared By	Checked By	Approved By

Contents

目录

1. General Description

LS028I15-R-V1 is a transmissive type a-Si TFT-LCD (amorphous silicon thin film transistor liquid crystal display) module, which is composed of a TFT-LCD panel, a driver circuit and a backlight unit. The panel size is 2.83 inch and the resolution is 240(RGB)*320, the panel can display up to 262k colors.

2. Physical Features

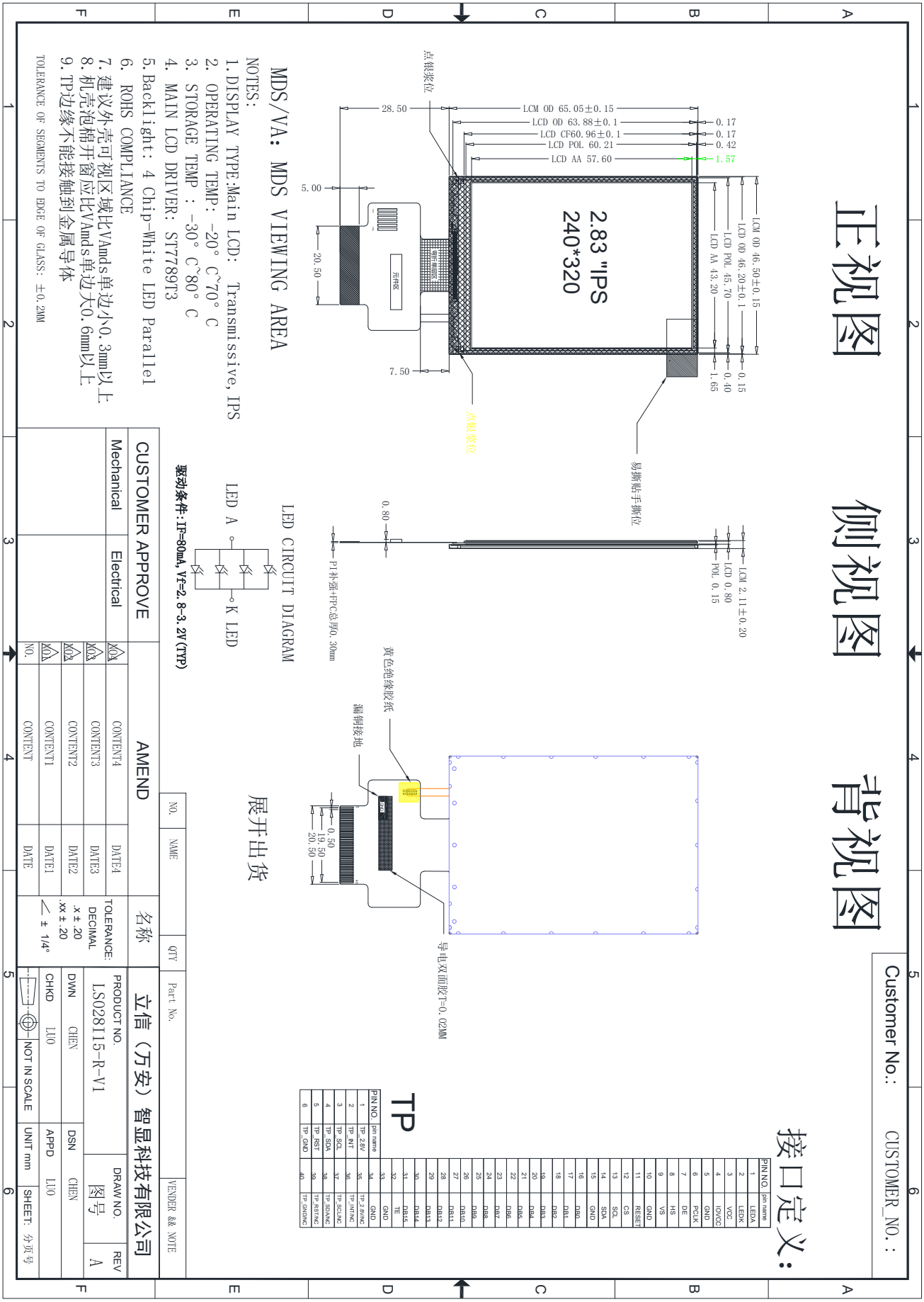
Display Mode	TFT-LCD Module
	Active matrix TFT, Transmissive type
Display Format	Graphic 240(RGB)×320 Dot-matrix
Input Data	RGB
Viewing Direction （Grayscale Inversion）	Free（IPS）
Drive	ST7789T3

3. Mechanical Specification

Item	Specification	Unit
Module size (H×V×D)	46.5 ×65.05×2.11	mm
Number of dots	240(RGB) ×320	pixel
Active area (H×V)	43.2×57.60	mm

60

4. Outline Dimension



PIN NO.	pin name
1	LEDA
2	LEDK
3	VCC
4	IOVCC
5	GND
6	PCLK
7	DE
8	HS
9	VS
10	GND
11	RESET
12	CS
13	SCL
14	SDA
15	GND
16	DB0
17	DB1
18	DB2
19	DB3
20	DB4
21	DB5
22	DB6
23	DB7
24	DB8
25	DB9
26	DB10
27	DB11
28	DB12
29	DB13
30	DB14
31	DB15
32	TE
33	GND
34	GND
35	TP_2.8VNC
36	TP_INTNC
37	TP_SCLNC
38	TP_SDANC
39	TP_RSTNC
40	TP_GNDNC

PIN NO.	pin name
1	TP_2.8V
2	TP_INT
3	TP_SCL
4	TP_SDA
5	TP_RST
6	TP_GND

5. Absolute Maximum Ratings

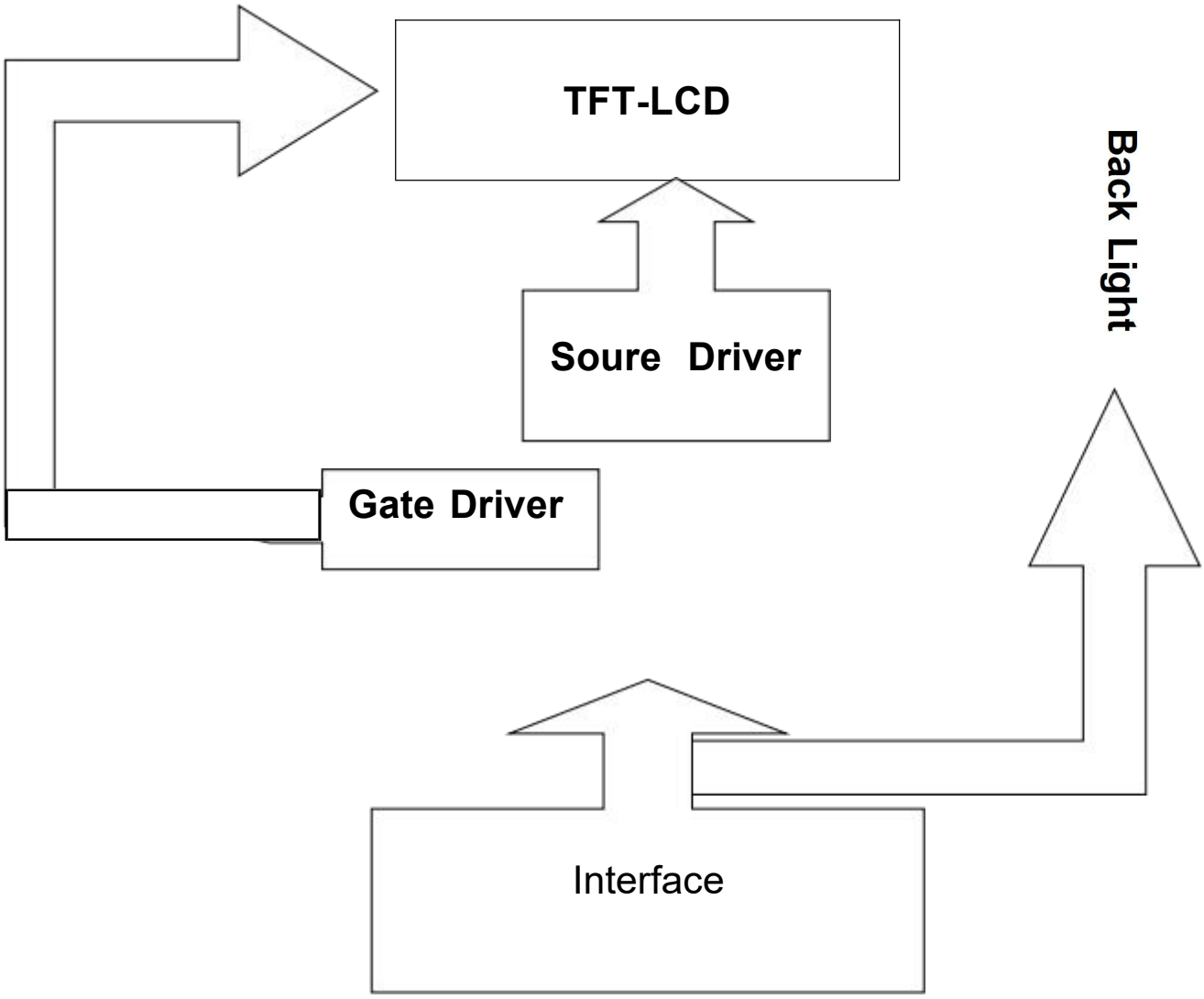
Item	Symbol	Min	Max	Unit	Remark
Supply voltage	VCC	-0.3	4.6	V	Note1 Note2
Supply voltage	IOVCC	-0.3	4.0	V	
Operating temperature	TOPR	-20	70	℃	
Storage temperature	TSTR	-30	80	℃	

6. Electrical Characteristics

Item		Symbol	Rating			Unit	Remark
			Min	Typ	Max		
Supply voltage		VCC	2.4	2.8	3.3	V	Note1
Supply voltage		IOVCC	1.65	1.8	3.3	V	
Input Voltage	L level	VIL	0	---	0.3*IOVCC	V	
	H level	VIH	0.7*IOVCC	---	IOVCC	V	

7. Module Function Description

7-1. Block Diagram Of LCM



7-2. Pin Description

PIN NO.	Symbol	I/O	Description
1	LEDA	P	Power for LED backlight anode
2	LEDK	P	Power for LED backlight cathode
3	VCC	P	Power Supply
4	IOVCC	P	Power Supply
5	GND	P	Ground
6	PCLK	I	Dot clock signal for RGB interface operation
7	DE	I	Data enable signal for RGB interface operation.
8	HS	I	Horizontal (Line) synchronizing input signal for RGB interface operation.
9	VS	I	Vertical (Frame) synchronizing input signal for RGB interface operation.
10	GND	P	Ground
11	RESET	I	This signal will reset the device and it must be applied to properly initialize the chip.
12	CS	I	Chip selection pin
13	SCL	I	Serial interface Clock Input
14	SDA	I/O	Serial interface DATA Input/Output
15	GND	P	Ground
16	R0	I	RGB interface data bus.
17	R1	I	RGB interface data bus.
18	R2	I	RGB interface data bus.
19	R3	I	RGB interface data bus.
20	R4	I	RGB interface data bus.
21	G0	I	RGB interface data bus.
22	G1	I	RGB interface data bus.
23	G2	I	RGB interface data bus.
24	G3	I	RGB interface data bus.
25	G4	I	RGB interface data bus.
26	G5	I	RGB interface data bus.

27	B0	I	RGB interface data bus.
28	B1	I	RGB interface data bus.
29	B2	I	RGB interface data bus.
30	B3	I	RGB interface data bus.
31	B4	I	RGB interface data bus.
32	TE	O	Tearing effect signal is used to synchronize MCU to frame memory MCU writing.
33	GND	P	Ground
34	GND	P	Ground
35	TP_2.8V/NC		
36	TP_INT/NC		
37	TP_SCL/NC		
38	TP_SDA/NC		
39	TP_RST/NC		
40	TP_GND/NC		

7-3 Timing Characteristics

7.4.2 Serial Interface Characteristics (3-line serial):

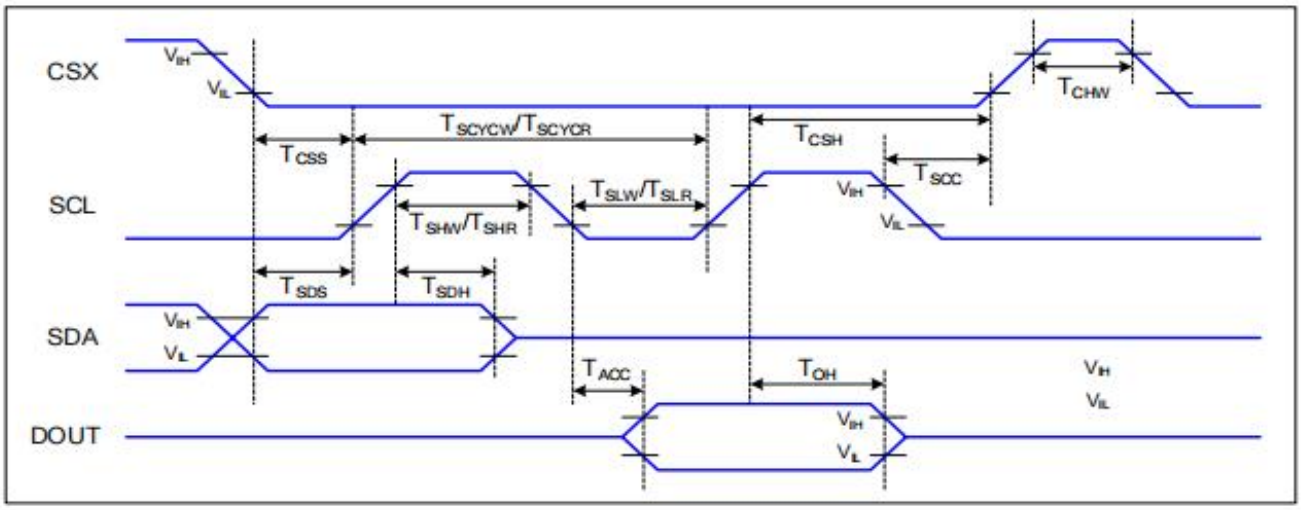


Figure 4 3-line serial Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	Tcss	Chip select setup time (write)	15		ns	
	Tcsh	Chip select hold time (write)	15		ns	
	Tcss	Chip select setup time (read)	60		ns	
	Tscc	Chip select hold time (read)	65		ns	
	Tchw	Chip select "H" pulse width	40		ns	
SCL	Tscycw	Serial clock cycle (Write)	16		ns	
	Tshw	SCL "H" pulse width (Write)	7		ns	
	Tslw	SCL "L" pulse width (Write)	7		ns	
	Tscycr	Serial clock cycle (Read)	150		ns	
	Tshr	SCL "H" pulse width (Read)	60		ns	
	Tslr	SCL "L" pulse width (Read)	60		ns	
SDA (DIN)	Tsds	Data setup time	7		ns	
	Tsdh	Data hold time	7		ns	
DOUT	Tacc	Access time	10	50	ns	For maximum CL=30pF
	Toh	Output disable time	15	50	ns	For minimum CL=8pF

Table 5 3-line serial Interface Characteristics

Note1 : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals

Note2: In the read sequence of serial interface, the 500nsec delay time is needed between read command and first read clock..

7.4.4 RGB Interface Characteristics:

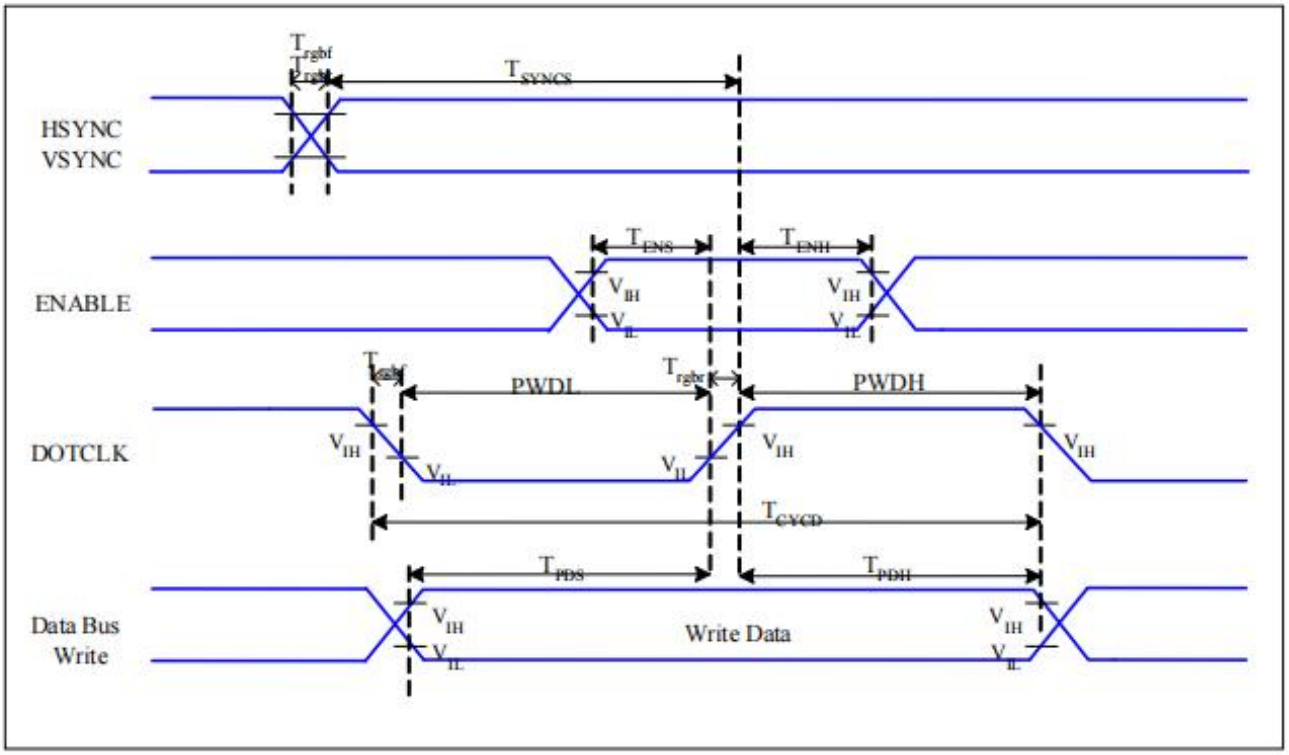


Figure 6 RGB Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	30	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	25	-	ns	
	T_{ENH}	Enable Hold Time	25	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	60	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	60	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	120	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	20	ns	
DB	T_{PDS}	PD Data Setup Time	50	-	ns	
	T_{PDH}	PD Data Hold Time	50	-	ns	

Table 7 18/16 Bits RGB Interface Timing Characteristics

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	35	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	35	-	ns	

	T_{ENH}	Enable Hold Time	35	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	35	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	35	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	80	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	10	ns	
DB	T_{PDS}	PD Data Setup Time	35	-	ns	
	T_{PDH}	PD Data Hold Time	35	-	ns	

Table 8 6 Bits RGB Interface Timing Characteristics

7.4.5 Reset Timing:

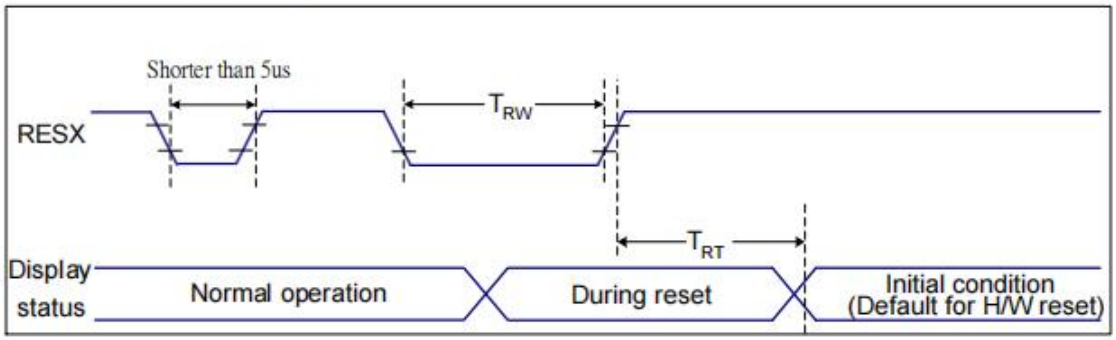


Figure 7 Reset Timing

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120 (Note 1, 6, 7)	ms

Table 9 Reset Timing

Notes:

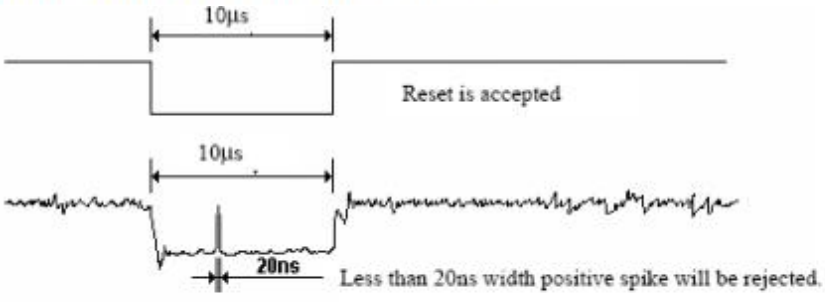
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

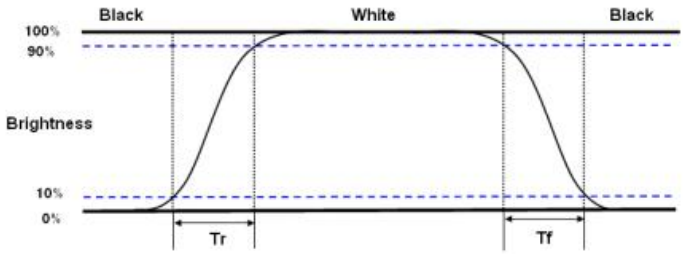
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

8. Electro-Optical Characteristics

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time		Tr +Tf	θx = θy =0	---	---	35	ms	Note 1
Contrast Ratio		CR		1000	1500	---	---	Note 2
Transmittance		T%		4.5	4.8	---	%	
Color Chromaticity (CIE1931)	White	W x	θx = θy =0	---	0.301	---	---	
		W y		---	0.320	---	---	
Viewing angle	θ_T		CR > 10	---	85	---	Deg.	Note 3
	θ_B			---	85	---		
	θ_L			---	85	---		
	θ_R			---	85	---		
Luminance (I_F = 80mA)		L		---	300	---	cd/m2	Note4

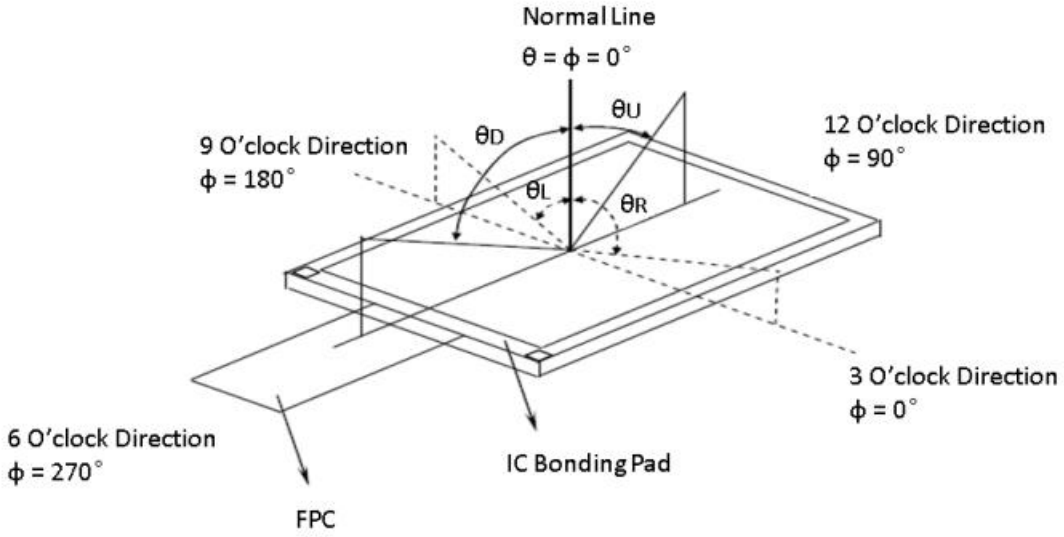
Note 3: Definition of response time:

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (Tr) is the time between photo detector output intensity changed from 10% to 90%. And fail time (Tf) is the time between photo detector out intensity changed from 90% to 10%.

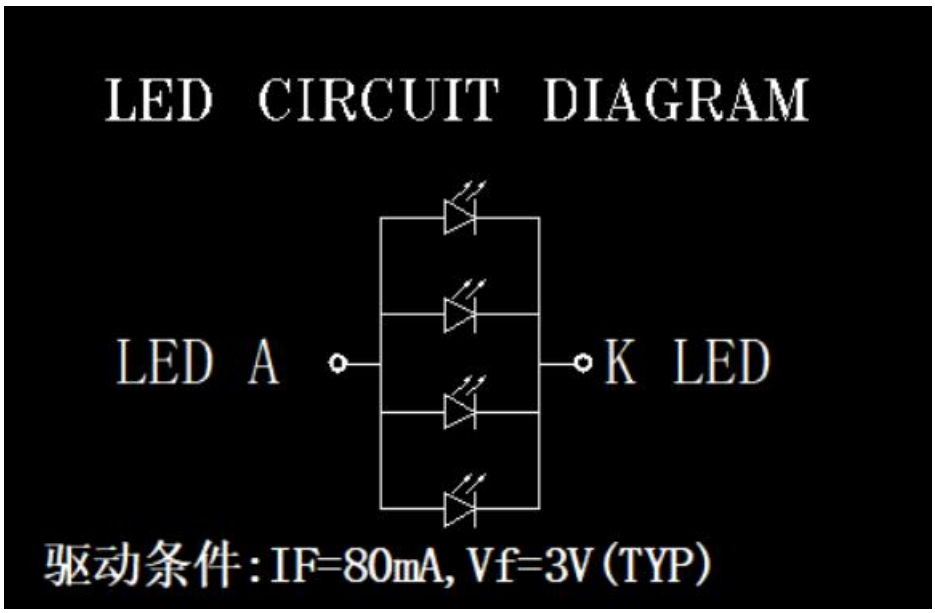


: Definition of viewing angle range and measurement system:

Viewing angle is measured at the center point of the LCD (With Normal Polarizer) by BM-5A.



Note(4) Backlight circuit



9.Records Of Version

Version	Revise Date	Page	Content
00	2025-7-28	ALL	New released