

PRODUCT SPECIFICATION **FOR LCD MODULE**

Revision: 1.0

Model No: LS028I09-X-V1

Module Type: COG+FPC+B/L

APPROVED SIGNATURE

- ☒ Approved Product Specification only
- ☐ Approved Product Specification and Samples

<u>Prepared By</u>	<u>Checked By</u>	<u>Approved By</u>

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1. GENERAL DESCRIPTION

1.1 DESCRIPTION

LS028I09-X-V1 is a transmissive type color active matrix TFT (Thin Film Transistor) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. This model is composed of a TFT-LCD module (TFT-LCD panel, driver IC and FPC), a back-light unit and. The resolution of 2.8" contains 240 RGB X320 pixels and can display up to 262k colors.

1.2 GENERAL INFORMATION

Items	Specification	Unit	Note
Drive element	a-Si TFT	-	-
LCM outline size	50.00 (H) x 69.20 (V)	mm	
Active area	43.20 (H) x 57.60 (V)	mm	-
Number of pixels	240(H)X320(V)	pixels	-
Pixel arrangement	RGB stripe	-	-
Pixel Pitch	0.180x 0.180	um	-
Display color	262k	color	-
Viewing direction	ALL	-	-
Controller / Driver	ST7789T3	-	-
Data interface	RGB/MCU8BIT/16BIT/SPI4W/3W 兼容	-	
Backlight	4 White LEDs In Parallels	-	
Weight	TBD	g	

2. ABSOLUTE MAXIMUM RATING

(Ta=25±2°C, Vss=GND=0V)

Characteristics	Symbol	Min.	Typ	Max.	Unit	Notes
Supply Voltage	IOVCC	-0.3	-	4.6	V	
	VCI	-0.3	-	4.6	V	
TFT Gate On voltage	VGH	-0.3	-	30	V	
TFT Gate Off voltage	VGL	-0.3	-	30	V	
Backlight Forward Current	I _F	-		80	mA	
Operating Temperature	T _{OPR}	-20		+70	°C	(1), (3)
Storage Temperature	T _{STG}	-30		+80	°C	(2), (3)
Humidity	RH	-		90	%	Max. 60 °C

Notes:

- (1) In case of below 0°C, the response time of liquid crystal (LC) becomes slower and the color of panel becomes darker than normal one. Level of retardation depends on temperature, because of the LC characteristics.
- (2) If product is exposed to high temperatures for extended time, there is a possibility of the polarizer film damage which could degrade the optical characteristics.
- (3) Permanent damage to the device may occur if maximum values are exceeded or reverse voltage is loaded.
Functional operation should be restricted to the conditions described under normal operating conditions.

3. ELECTRICAL CHARACTERISTICS

3.1 LCM DC CHARACTERISTICS

(Ta=25±2°C)

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Power Supply Voltage 1	IOVCC	1.65	1.8	3.3	V	
Power Supply Voltage 2	VCI	2.45	2.75	3.3	V	
Power Supply Voltage 3	-	-	-	-	V	
Power Supply for MTP	VPP	-	-	-	V	
Current Consumption	I _{DD}	-	TBD	-	mA	Normal mode
	I _{DD-SLEEP}		TBD		uA	Sleep mode
Input voltage "L" Level	V _{IL}	GND	-	0.3IOVCC	V	IOVCC=1.65~3.3
Input voltage "H" Level	V _{IH}	0.7IOVCC	-	IOVCC	V	
Output voltage "L" Level	V _{OL}	0	-	0.2IOVCC	V	I _{OL} =1mA
Output voltage "H" Level	V _{OH}	0.8IOVCC	-	IOVCC	V	I _{OH} =-1mA

3.2 BACK-LIGHT UNIT CHARACTERISTICS

The back-light system is an edge-lighting type with 4 white LEDs. The characteristics of the back-light are shown in the following tables.

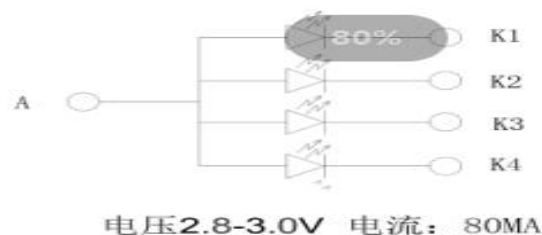
(Ta=25±2°C)

Characteristics	Symbol	Condition	Min.	Type	Max.	Unit	Notes
Forward Voltage	V _f	I _L =80mA	2.8	3.0	-	V	-
Forward current	I _L		-	80	-	mA	-
Luminance	L _v	I _L =80mA	250	300	--	cd/m ²	-
LED life time	-	I _L =80mA	20,000	25,000	--	Hr	Note 1

Note:

- (1) The "LED life time" is defined as the module brightness decrease to 50% of original brightness at I_L=80mA. The LED life time could be decreased if operating I_L is larger than 80mA.

Bcklight circuit diagram shown in below:



4. OPTICAL CHARACTERISTICS

The following items are measured under stable conditions. The optical characteristics should be measured in a dark room.

Measuring equipment: BM-5AS, BM-7, EZ-Contrast.

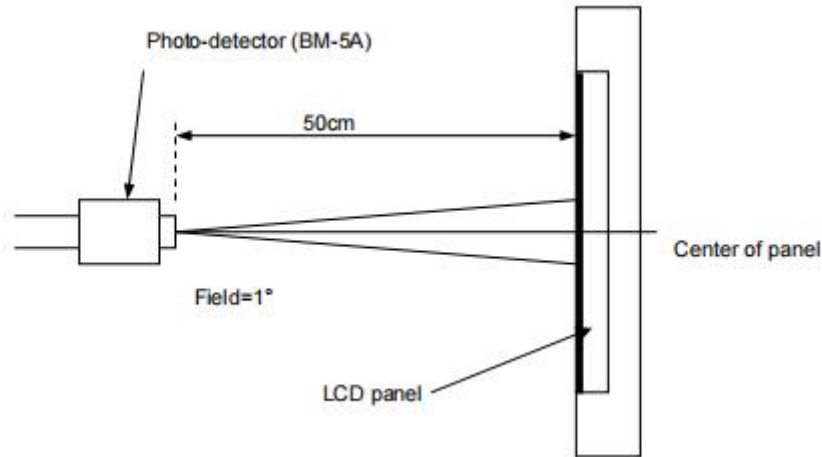
(Ta=25±2°C)

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio (Center point)		C/R	-	250	300	-	cd/m ²	BM-7 Note(2)
Luminance of white (Center point)		L _w	B/L on	15%	TBD	15%	-	CA-210
Luminance uniformity		U _w	θ = 0. Normal viewing angle B/L On Note(1)	80	-	-	%	BM-7 Note(3)
Response Time		Tr + Tf		-	30	35	ms	BM-5AS Note(4)
Color Chromaticity (CIE 1931)	White	W _X		0.305	0.308	0.313	-	CA-210 Note(5)
		W _X		0.336	0.339	0.344		
	Red	R _X		0.655	0.658	0.653		
		R _Y		0.333	0.338	0.343		
	Green	G _X		0.257	0.262	0.267		
		G _Y		0.595	0.600	0.605		
	Blue	B _X		0.129	0.134	0.139		
		B _Y		0.132	0.137	0.142		
Viewing Angle	Hor.	θ _T	C/R≥10	75	80	-	Deg	EZ Contrast Note(6)
		θ _B		75	80	-		
	Ver.	θ _L		75	80	-		
		θ _R		75	80	-		
Optima View Direction			ALL					Note(7)

* This condition will be changed by the evaluation circumstance. If product is exposed to high temperatures for extended time, there is a possibility of the polarizer film damage which could degrade the optical characteristics.

Notes:

- (1) Test Equipment Setup: After stabilizing and leaving the panel alone at a given temperature for 30min, the measurement should be executed. Measurement should be executed in a stable, windless, and dark room 30min after lighting the back-light. This should be measured in the center of screen.

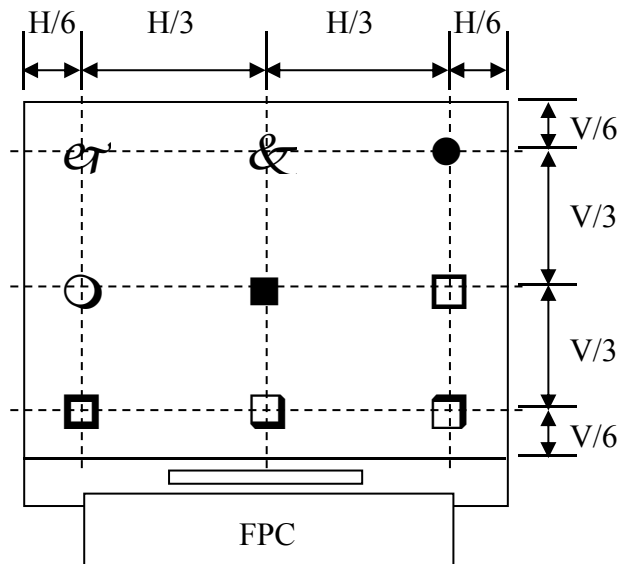


- (2) Definition of Contrast Ratio (CR):

$$\text{Contrast Ratio (CR)} = \frac{\text{Luminance measured when LCD on the "white" state}}{\text{Luminance measured when LCD on the "black" state}}$$

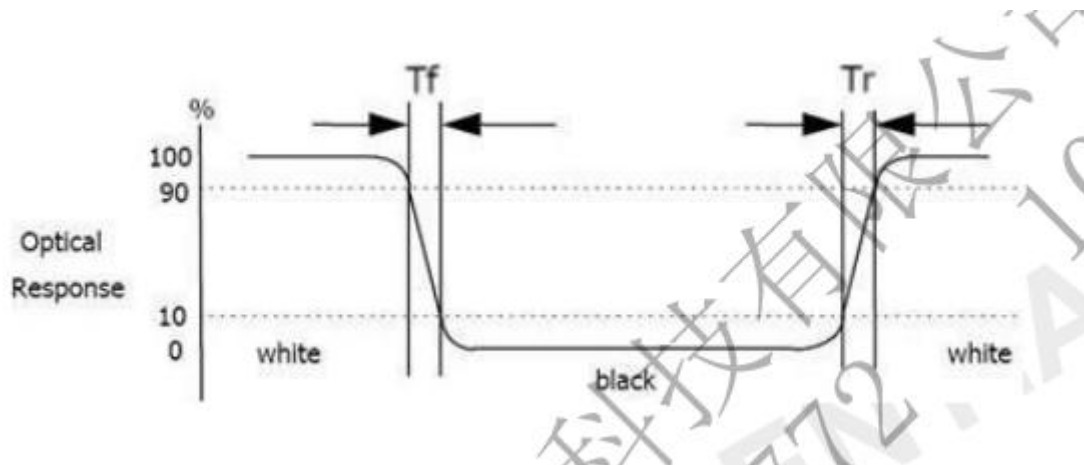
- (3) Definition of Luminance Uniformity: Active area is divided into 9 measuring areas (Shown in below), every measuring point is placed at the center of each measuring area.

$$\text{Luminance Uniformity} = \frac{\text{Min Luminance of white among 9-points}}{\text{Max Luminance of white among 9-points}} \times 100\%$$

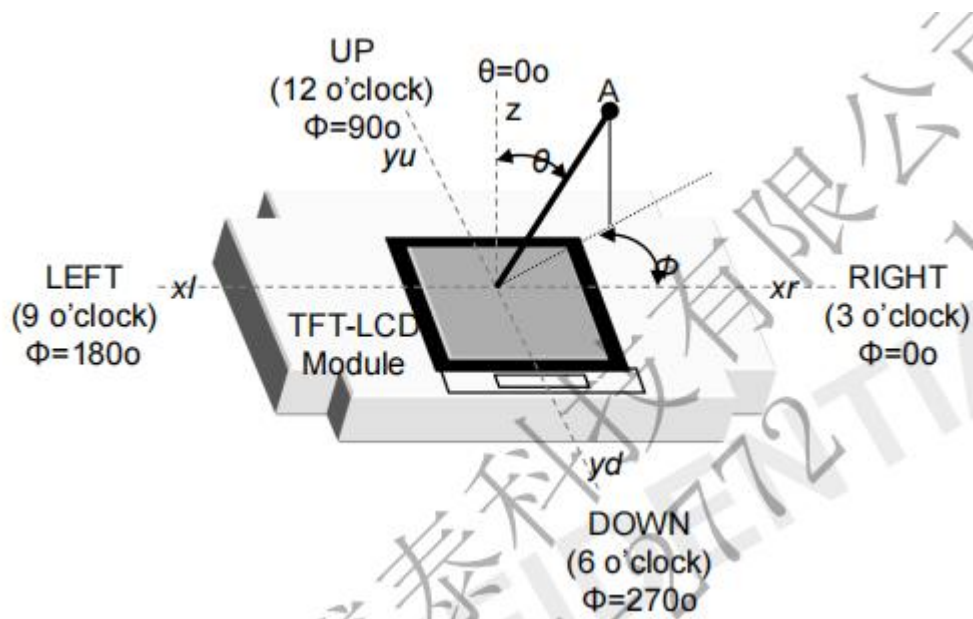


The spot locations for luminance measurement

- (4) Definition of Response time: Sum of T_r and T_f .

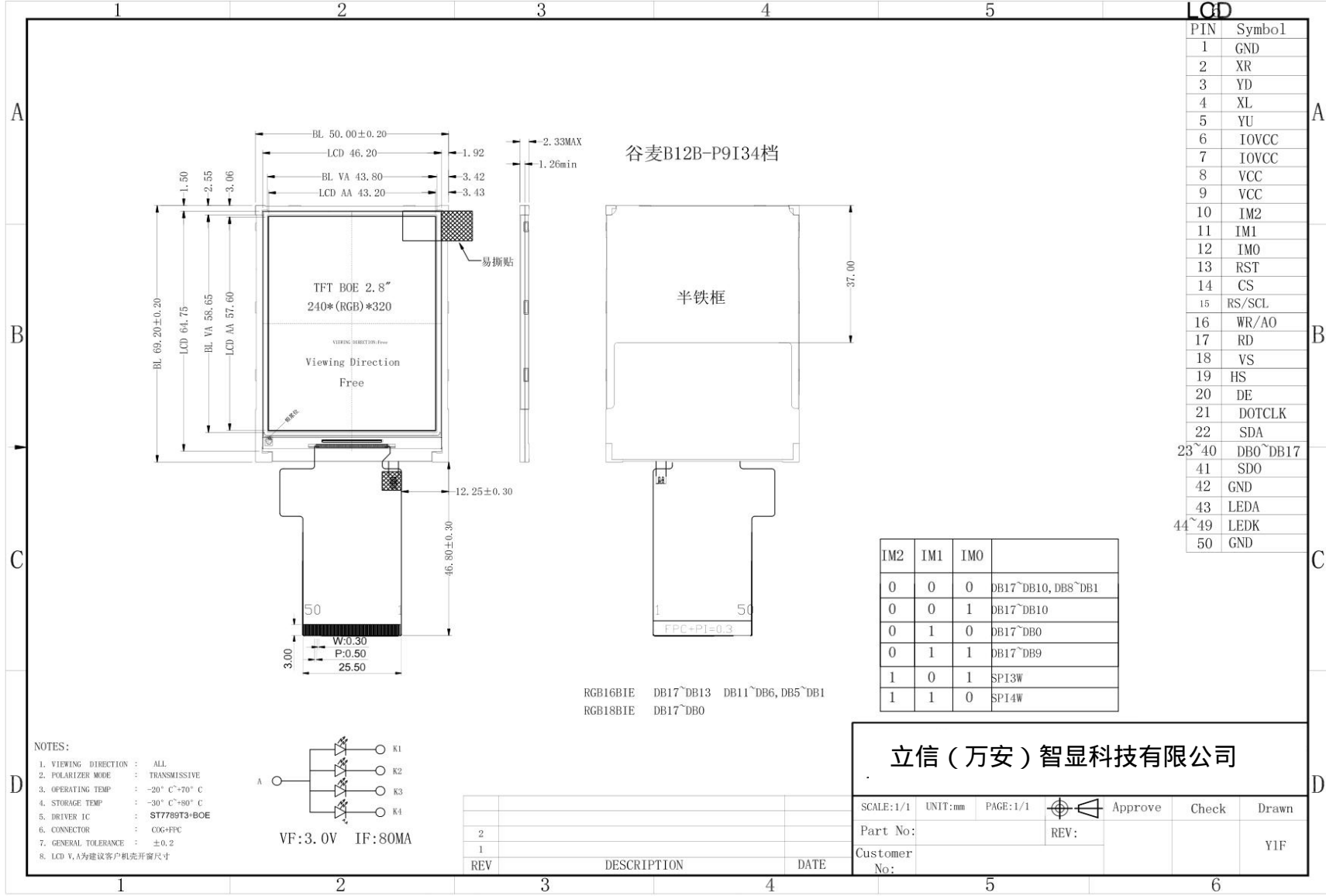


- (5) Definition of Viewing Angle: The viewing angle range that the $CR \geq 10$.



- (6) Definition of Color Chromaticity (CIE 1931)
Color coordinate of white & red, green, blue at center point.
- (7) The different Rubbing Direction will cause the different optima view direction.

5. MODULE OUTLINE DIMENSION



6. MODULE INTERFACE DESCRIPTION

Pin No.	Symbol	Description
1	GND	Power Ground
2	XR	TP
3	YD	TP
4	XL	TP
5	YU	TP
6	IOVCC	Power supply for I/O block. 1.8V
7	IOVCC	Power supply for I/O block. 1.8V
8	VCC	Power supply for I/O block. 2.8-3.3V
9	VCC	Power supply for I/O block. 2.8-3.3V
10	IM2	Select the MCU interface mode
11	IM1	Select the MCU interface mode
12	IM0	Select the MCU interface mode
13	RST	Reset input pin
14	CS	Chip select input pin
15	RS/SPI SCK	Data or Command select pin in the parallel interface / This pin is used serial interface clock in 3-wire 9-bit / 4-wire 8-bit serial data interface.
16	WR/A0	Write signal input pin / 4-line system (D/CX): Serves as command or parameter select.
17	RD	Serial output signal
18	VS	Frame synchronizing signal for RGB interface operation
19	HS	Line synchronizing signal for RGB interface operation
20	DE	Data enable signal for RGB interface operation
21	DOTCLK	Dot clock signal for RGB interface operation
22	SDA	Serial data input / output bidirectional pin for SPI .
23-40	DB0-DB17	parallel bi-directional data bus for MCU/RGB system
41	SD0	Serial output signal.

42	GND	Power Ground
43	LEDA	Back-light Anode
44	LEDK	Back-light Cathode
45	LEDK	Back-light Cathode
46	LEDK	Back-light Cathode
47	LEDK	Back-light Cathode
48	LEDK	Back-light Cathode
49	LEDK	Back-light Cathode
50	GND	Power Ground

- Select the MCU interface mode

IM3	IM2	IM1	IM0	MCU-Interface Mode	DB Pin in use	
					Register/Content	GRAM
1	0	0	0	80 MCU 16-bit bus interface II	D[8:1]	D[17:10], D[8:1]
1	0	0	1	80 MCU 8-bit bus interface II	D[17:10]	D[17:10]
1	0	1	0	80 MCU 18-bit bus interface II	D[8:1]	D[17:0]
1	0	1	1	80 MCU 9-bit bus interface II	D[17:10]	D[17:9]
1	1	0	1	3-wire 9-bit data serial interface II	SDI: In SDO: Out	
1	1	1	0	4-wire 8-bit data serial interface II	SDI: In SDO: Out	

RESX	I	-This signal will reset the device and it must be applied to properly initialize the chip. -Signal is active low.	MCU
CSX	I	-Chip selection pin Low enable. High disable.	MCU
DCX	I	-Display data/command selection pin in parallel interface. -This pin is used to be serial interface clock.	MCU

		DCX='1': display data or parameter. DCX='0': command data. -If not used, please fix this pin at VDDI or DGND.	
RDX	I	-Read enable in 8080 MCU parallel interface. -If not used, please fix this pin at VDDI or DGND.	MCU
WRX	I	-Write enable in MCU parallel interface. - Display data/command selection pin in 4-line serial interface. - Second Data lane in 2 data lane serial interface. -If not used, please fix this pin at VDDI or DGND.	MCU

VSYNC	I	-Vertical (Frame) synchronizing input signal for RGB interface operation. -If not used, please fix to the VDDI or DGND.	MCU
HSYNC	I	-Horizontal (Line) synchronizing input signal for RGB interface operation. - If not used, please fix to VDDI or DGND.	MCU
ENABLE	I	-Data enable signal for RGB interface operation. -If not used, please fix this pin at VDDI or DGND.	MCU
DOTCLK	I	-Dot clock signal for RGB interface operation. -If not used, please fix this pin at VDDI or DGND.	MCU

7. REFERENCE APPLICATION CIRCUIT

Please consult our technical department for detail information.

8.TIMINGS FOR MCU SPI RGB Interface

7.4.2 Serial Interface Characteristics (3-line serial):

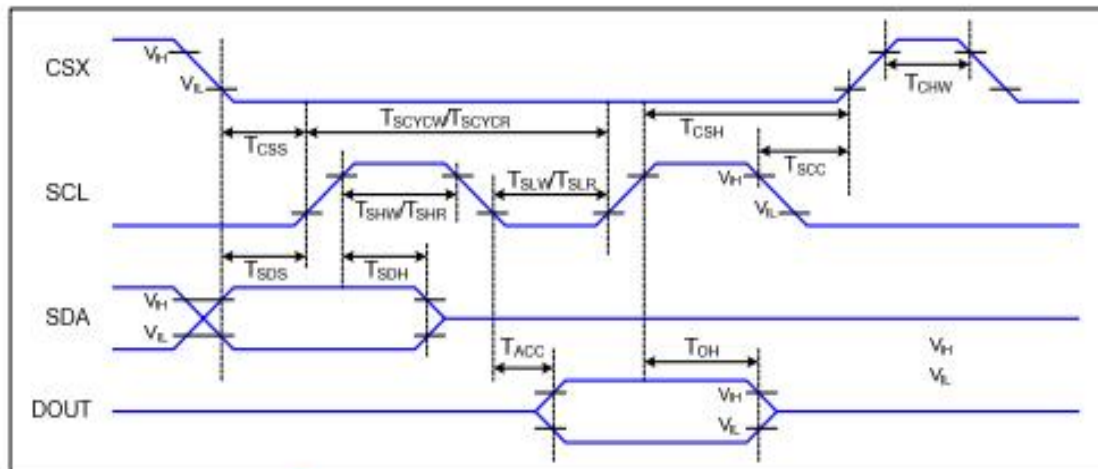


Figure 4 3-line serial Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 to 70 °C

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	
	T_{SLW}	SCL "L" pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

Table 5 3-line serial Interface Characteristics

Note : The rising time and falling time (T_r , T_f) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for input signals.

7.4.3 Serial Interface Characteristics (4-line serial):

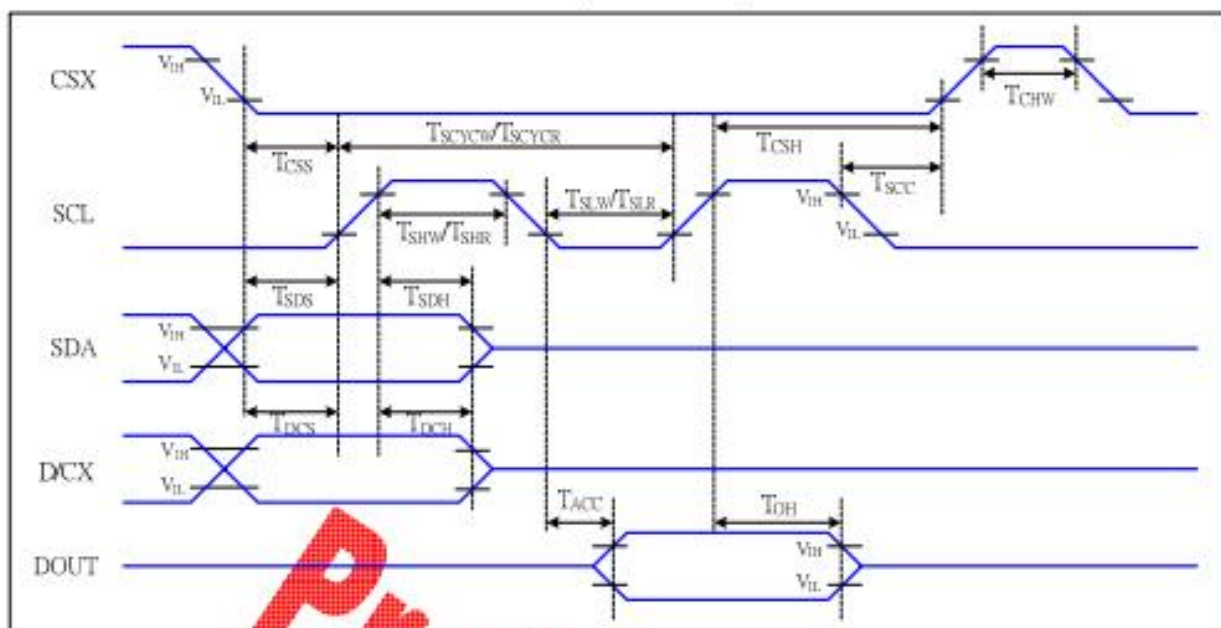


Figure 5 4-line serial Interface Timing Characteristics

$V_{DD1}=1.65$ to $3.3V$, $V_{DD}=2.4$ to $3.3V$, $AGND=DGND=0V$, $T_a=-30$ to 70 °C

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	-write command & data ram
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	
	T_{SLW}	SCL "L" pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	-read command & data ram
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
D/CX	T_{DCS}	D/CX setup time	10		ns	
	T_{DCH}	D/CX hold time	10		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum $CL=30pF$
	T_{OH}	Output disable time	15	50	ns	For minimum $CL=8pF$

7.4 AC Characteristics

7.4.1 8080 Series MCU Parallel Interface Characteristics: 18/16/9/8-bit Bus

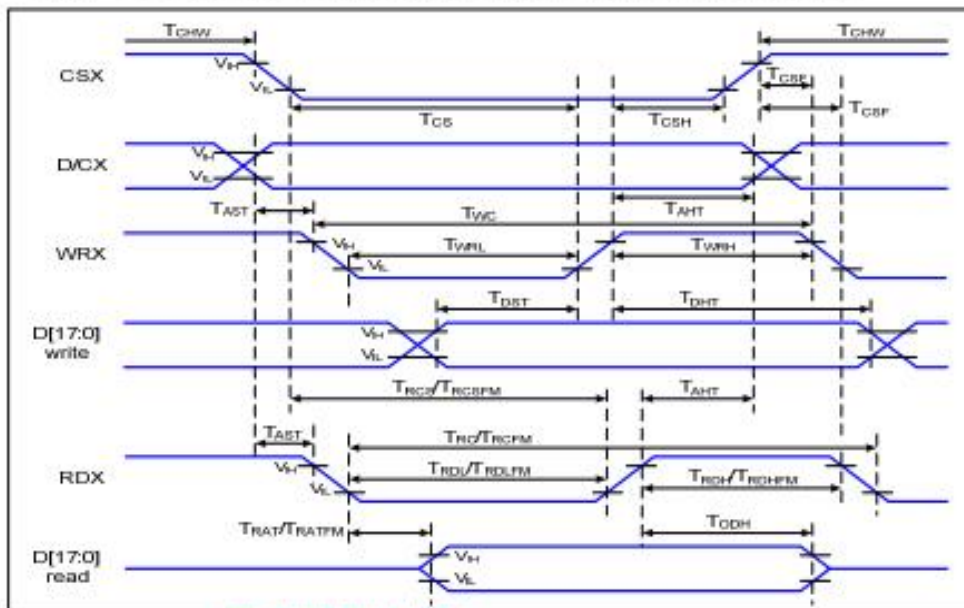


Figure 1 Parallel Interface Timing Characteristics (8080-Series MCU Interface)

VDD=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ts= -30 to 70 °C

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T _{AST}	Address setup time	0		ns	
	T _{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T _{CHW}	Chip select "H" pulse width	0		ns	
	T _{CS}	Chip select setup time (Write)	15		ns	
	T _{RCS}	Chip select setup time (Read ID)	45		ns	
	T _{RCSFM}	Chip select setup time (Read FM)	355		ns	
	T _{CSF}	Chip select wait time (Write/Read)	10		ns	
	T _{CSH}	Chip select hold time	10		ns	
WRX	T _{WC}	Write cycle	66		ns	
	T _{WRH}	Control pulse "H" duration	15		ns	
	T _{VRL}	Control pulse "L" duration	15		ns	
RDX (ID)	T _{RC}	Read cycle (ID)	160		ns	When read ID data
	T _{RDH}	Control pulse "H" duration (ID)	90		ns	
	T _{RDL}	Control pulse "L" duration (ID)	45		ns	
RDX (FM)	T _{RCFM}	Read cycle (FM)	450		ns	When read from frame memory
	T _{RDHF}	Control pulse "H" duration (FM)	90		ns	
	T _{RDLF}	Control pulse "L" duration (FM)	355		ns	
D[17:0]	T _{DST}	Data setup time	10		ns	For CL=30pF

7.4.4 RGB Interface Characteristics.

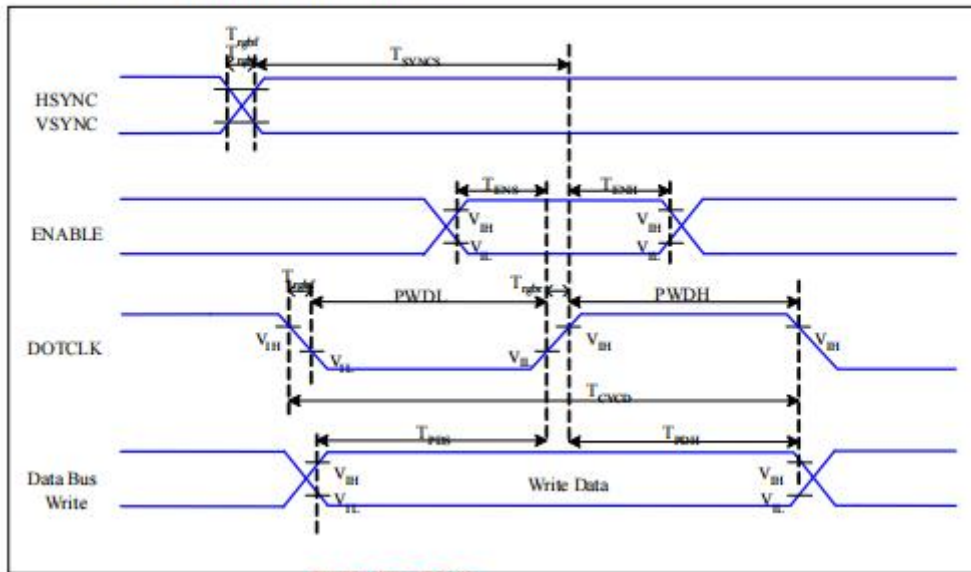


Figure 6 RGB Interface Timing Characteristics

VDD=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 ~ 70 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCs}	VSYNC, HSYNC Setup Time	30	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	25	-	ns	
	T_{ENH}	Enable Hold Time	25	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	60	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	60	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	120	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	20	ns	
DB	T_{PDS}	PD Data Setup Time	50	-	ns	
	T_{PDH}	PD Data Hold Time	50	-	ns	

Table 7 18/16 Bits RGB Interface Timing Characteristics

9.RELIABILITY TEST CONDITIONS

No.	Test Item	Test Condition	Notes
1	High Temperature Storage	+80°C / 240H	Inspection after 2~4h storage at room temperature, the sample shall be free from defects: 1. Air bubble in the LCD; 2. Seal leak; 3. Non-display; 4. Missing segments; 5. Glass crack; 6. The surface shall be free from damage. 7. The electrical characteristics requirements shall be satisfied.
2	Low Temperature Storage	-30°C / 240H	
3	High Temperature Operating	+70°C / 240H	
4	Low Temperature Operating	-20°C / 240H	
5	Temperature Cycle	Ta=-10°C~+25~+50°C, 10 Cycle, per 30min	
6	High Temperature /Humidity storage	60°C ,90%RH / 120H	
7	Vibration Test	Frequency: 10Hz~55Hz~10Hz Amplitude: 1.5mm, 2 hours for each direction of X, Y, Z	
8	Packing Drop Test	Drop to the ground from 1m height, 1 corner, 3 edges, 6 surfaces.	
9	ESD test	Voltage: ±8KV R: 330Ω C: 150pF Air discharge, Three or five times.	

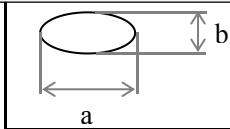
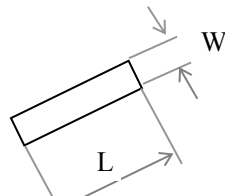
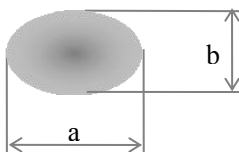
Remarks:

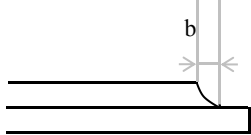
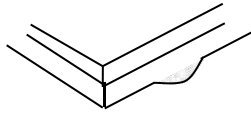
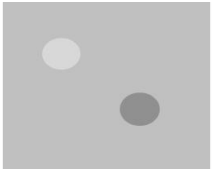
- (1) The test samples should be applied to only one test item.
- (2) Sample size for each test item is 5~10pcs.
- (3) For High Temperature/Humidity storage test, pure water (resistance>10MΩ) should be used.
- (4) In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judge as a good part.
- (5) Failure judgment criterion: basic specification, electrical characteristic, mechanical characteristic, optical characteristic.

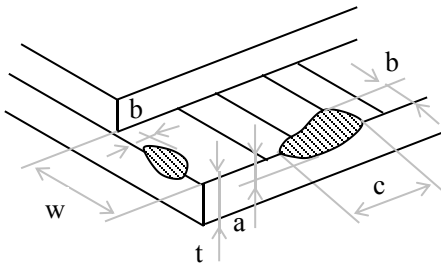
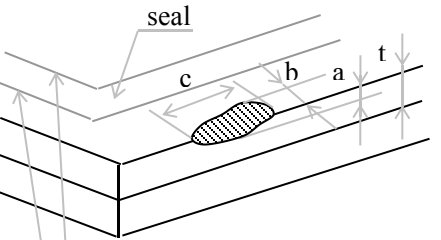
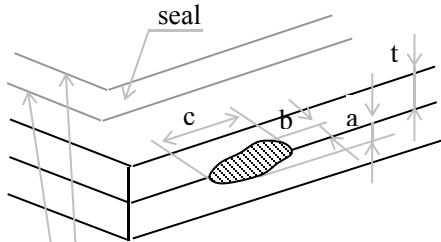
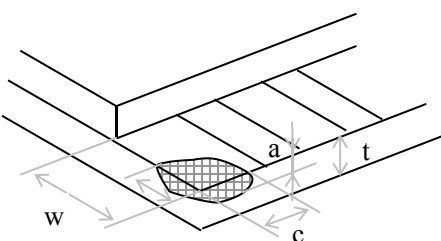
10.PACKING SPECIFICATION

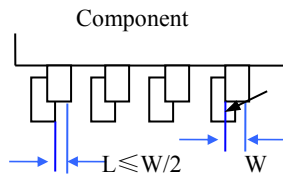
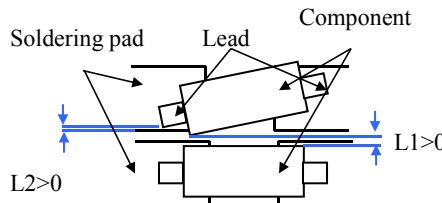
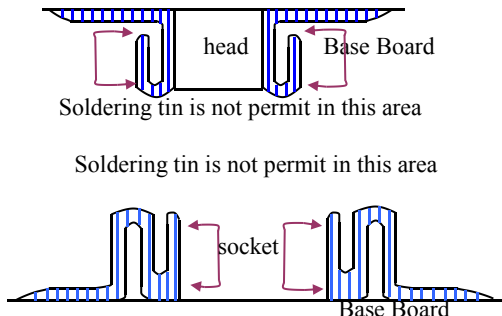
TBD

11.INSPECTION CRITERION

Inspection item			Judgement standard					
			Category		Acceptable number			
					A zone	B zone		
1	Black spot, White spot, Bright Spot, Pinhole Foreign Particle, Bubble and Particle Between polarizer and glass, scratch on polarizer			A	$\Phi \leq 0.10$	Ignored	Ignored	
				B	$0.10 < \Phi \leq 0.20$	2		
				C	$\Phi > 0.2$	0		
				Total defective point(B,C)		3		
	Pixel point defect	Bright spot		$0.15 < \Phi \leq 0.20$		$N \leq 2$	Ignored	
		Dark spot/ Black spot		$0.15 < \Phi \leq 0.20$		$N \leq 2$		
		Attached to the two pixels are bright spots		$0.15 < \Phi \leq 0.20$		$N \leq 2$		
		Even a two pixel is dark		$0.15 < \Phi \leq 0.20$		$N \leq 2$		
		Pixel total number		$0.15 < \Phi \leq 0.20$		$N \leq 2$		
		Note1: the spot defect caused by foreign matter is judged according to the defect of the foreign body. Note 2: when the light is not wired to show the type of defects.						
	2	Black line, White line, Bubble and Particle Between Polarizer and glass, Scratch on polarizer			A	$W \leq 0.03 \quad L \leq 3.0$	Ignored	Ignored
					B	$0.03 < W \leq 0.05 \quad L \leq 3.0$	2	
			C	$0.05 < W$	0			
			Total defective point(B,C)		2			
3	Contrast variation			A	$\Phi \leq 0.1$	Ignored	Ignored	
				B	$0.1 < \Phi \leq 0.3$	2		
				C	$\Phi > 0.3$	0		
			Total defective point(B,C)		2			
4	Bubble inside cell		any size		none	none		
5	Polarizer defect (if Polarizer is used)	Scratch and damage on polarizer, particle on polarizer or between polarizer and glass.		Refer to item 1 and item 2.				
		Bubble, dent and convex	A	$\Phi \leq 0.3$	Ignored	Ignored		
			B	$0.3 < \Phi \leq 0.5$	2			
			C	$0.5 < \Phi$	0			
			Total defective point(B,C)		2			

Inspection item		Judgement standard	
		Category	Acceptable number
			A zone B zone
6	Surplus glass	①Stage surplus glass 	$b \leq 0.3\text{mm}$
		②Surrounding surplus glass 	Should not influence outline dimension and assembling.
7	MURA	①MURA	Naked eye examination: red, green, blue screen does not allow the appearance, black screen requires visual is not obvious, the specific reference limit samples. Note: the principle of closing the sample is to be installed on the whole machine and the end user will not find it in the normal usage scenario. Inspection basis: 6%ND (MURA mainly in the black screen and indoor light is relatively dark will be found, it is recommended to turn off the indoor lighting inspection.)
		②Point Black / White / point(MURA) 	1, under the black / gray screen check: $D \leq 0.10\text{mm}$ Ignored; $0.10\text{mm} < D \leq 0.3\text{mm}$, $N \leq 2$; $D > 0.3\text{mm}$: Unqualified. 2, switch to the red, green, blue in which any one of the screen appears black or white or point to point white or point of failure. 

Inspection item			Judgment standard	
			Category(application: B zone)	
8	Glass defect crack	①The front of lead terminals	A	If $a \leq t$ and $b \leq 1.0$, c is not limited
			B	$a \leq t$, $1 \leq b \leq 2\text{mm}$, $c \leq 3\text{mm}$
			C	If glass crack cover alignment mark, $b \leq 0.5\text{mm}$.
			D	Crack at two sides of lead terminals should not cover patterns and alignment mark
		②Surrounding crack—non-contact side	 <u>Inner border line of the seal</u> <u>Outer border line of the seal</u> $b < \text{Inner borderline of the seal}$	
		③ Surrounding crack— contact side	 <u>Inner border line of the seal</u> <u>Outer border line of the seal</u> $b < \text{Outer borderline of the seal}$	
		④Corner	A	$a \leq t$, $b \leq 3.0$, $c \leq 3.0$
			*Glass crack should not cover patterns used for	

Inspection item			Judgement standard
9	FPC defect	Component soldering: No cold soldering, short/open circuit, burr, tin ball. The flat encapsulation component position deviation must be less than 1/2 width of the pin (Pic.1); The sheet component deviation: pin deviates from the pad and contact with the near components is not permitted (Pic.2)	 Component $L \leq W/2$ W
		lead defect: The lead lack must be less than 1/2 of its width; The lead burr must be less than 1/2 of the seam; Impurities connect with the near leads is not permitted	 Soldering pad Lead Component $L1 > 0$ $L2 > 0$
		Connector soldering: Soldering tin is at contact position of the plug and socket is not permitted No foundation is scald Serious cave distortion on plug and socket contact pin is not permitted	 head Base Board Soldering tin is not permit in this area Soldering tin is not permit in this area socket Base Board

12.GENERAL PRECAUTIONS

1.1 HANDING

- (1) When the module is assembled, it should be attached to the system firmly. Be careful not to twist and bent the module.
- (2) Refrain from strong mechanical shock and / or any force to the module. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
- (3) Note that display modules are very fragile and could be easily damaged. Do not press or scratch the surface harder than a HB pencil lead.
- (4) Wipe off water droplets or oil immediately. If you leave the droplets for a long time, straining and discoloration may occur.
- (5) If the display module surface becomes contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If it is heavily contaminated, should be wiped by moisten cloth with isopropyl alcohol or ethyl alcohol solvents, DO NOT with water, ketone type materials (e.g. acetone), aromatic, toluene, ethyl acid or methyl chloride, and so on.
- (6) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs or clothes, it must be washed away thoroughly with soap.
- (7) Use finger-stalls with sort gloves in order to keep display clean during the incoming inspection and assembly process.
- (8) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
- (9) Do not touch directly conductive parts such as the CMOS LSI pad and the interface terminals with bare hands, therefore operations should be grounded whenever he/she comes into contact with the modules.
- (10) Do not exceed the absolute maximum rating value. (The supply voltage variation, input voltage variation, variation in part contents and environmental temperature, and so on), otherwise the module may be damaged.

1.2 SOLDERING

- (1) Use soldering irons with proper grounding and no leakage.
- (2) For No RoHS Product: soldering temperature is 290~350°C, soldering time is 3~5s; for RoHS Product: soldering temperature is 340~370°C, soldering time is 3~5s.
- (3) If soldering flux is used, be sure to remove any remaining flux after soldering (This does not apply in the case of a non-halogen type of flux).

1.3 STORAGE

- (1) DO NOT leave the module in high temperature and high humidity for a long times, keep the temperature from 0°C to 35°C and relative humidity of less than 60%.
- (2) It is highly recommended to store the module in a dark place. The Liquid crystal is deteriorated by ultraviolet, DO NOT leave it in direct sunlight and strong ultraviolet ray for many hours.