PRODUCT SPECIFICATION FOR LCD MODULE

Revision: 1.0

Model No: LSC028I05-MP-V1

Module Type: COG+FPC+B/L

APPROVED SIGNATURE

■ Approved Product Specification only

□ Approved Product Specification and Samples

Prepared By	Checked By	Approved By

Contents

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1. General Description

LSC028I05-MP-V1 is a transmissive type a-Si TFT-LCD (amorphous silicon thin film transistor liquid crystal display) module, which is composed of a TFT-LCD panel, a driver circuit and a backlight unit. The panel size is 2.76 inch and the resolution is 480(RGB)*480, the panel can display up to 16.7M colors.

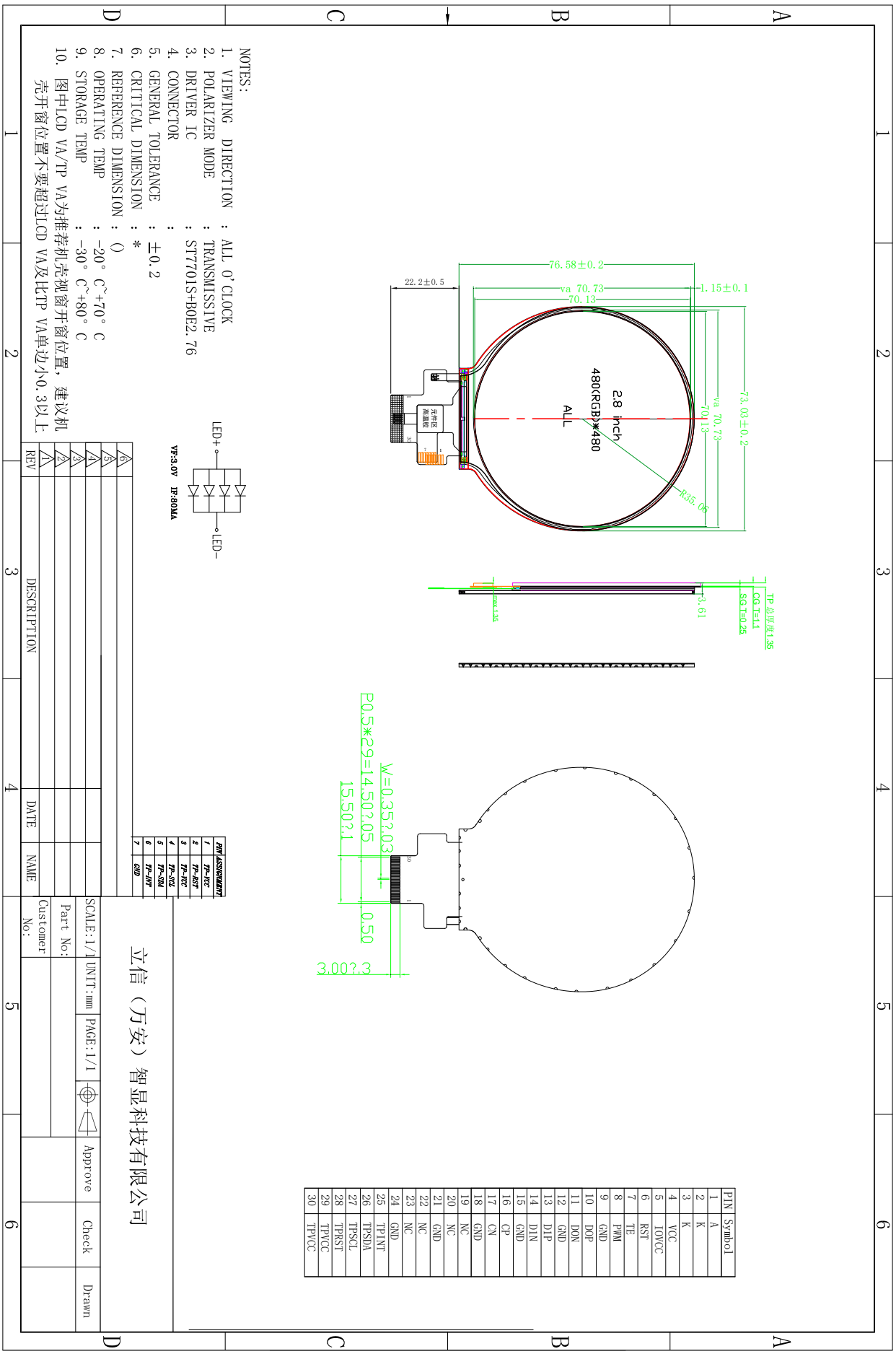
2. Physical Features

Display Mode	TFT-LCD Module
	Active matrix TFT, Transmissive type
Display Format	Graphic 480(RGB)×480 Dot-matrix
Input Data	MIPI
Viewing Direction （Grayscale Inversion）	Free（IPS）
Drive	ST7701SN

3. Mechanical Specification

Item	Specification	Unit
Module size (H×V×D)	73.03 ×76.58 ×2.26	mm
Number of dots	480(RGB) ×480	pixel
Active area (H×V)	70.13×70.13	mm

4. Outline Dimension



PIN	Symbol
1	A
2	K
3	K
4	VCC
5	IOVCC
6	RST
7	TE
8	PWM
9	GND
10	DOP
11	DON
12	GND
13	D1P
14	D1N
15	GND
16	CP
17	CN
18	GND
19	NC
20	NC
21	GND
22	NC
23	NC
24	GND
25	TPINT
26	TPSDA
27	TPSCL
28	TPRST
29	TPVCC
30	TPVCC

5. Absolute Maximum Ratings

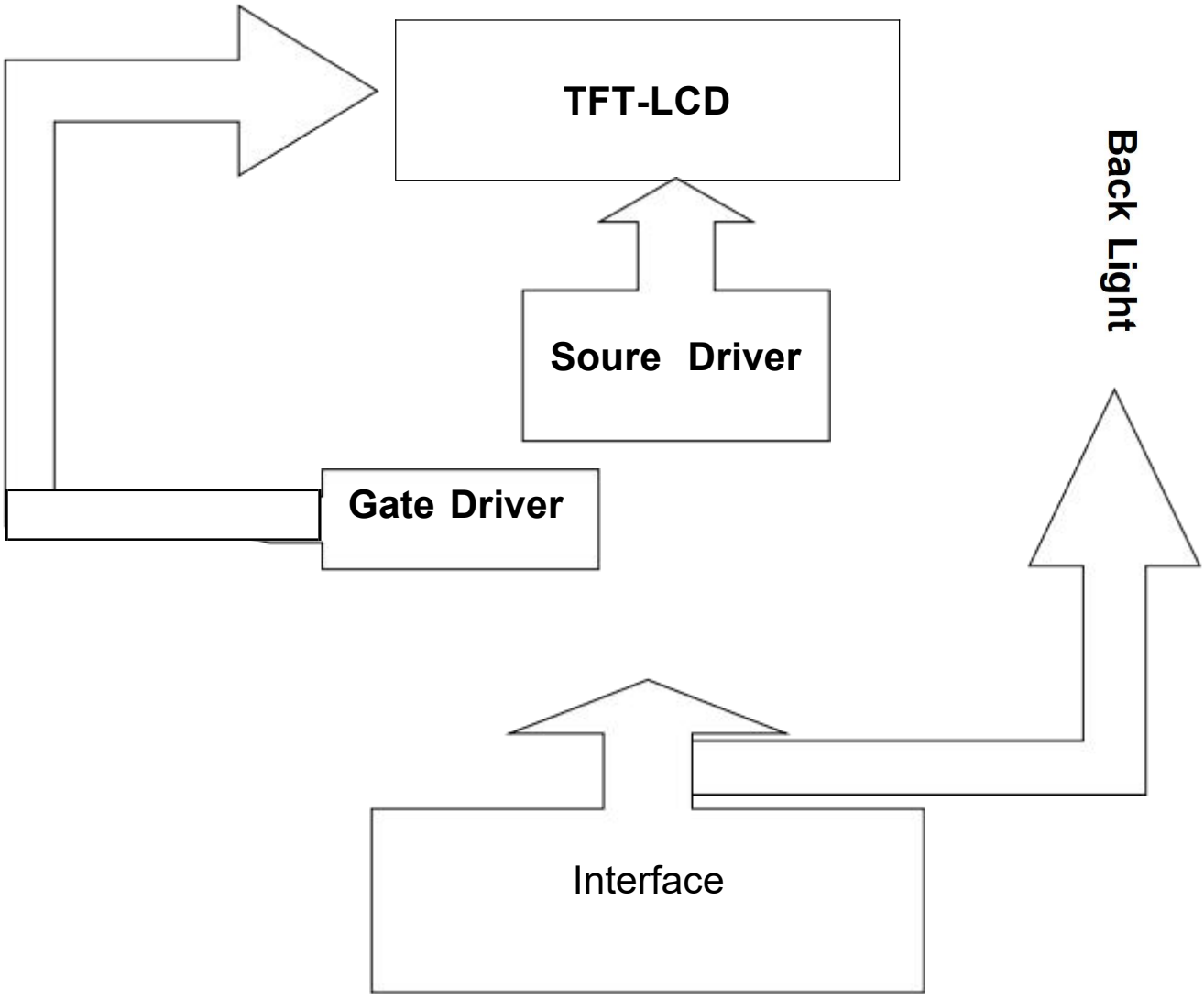
Item	Symbol	Min	Max	Unit	Remark
Supply voltage	VCC	-0.3	4.6	V	Note1 Note2
Supply voltage	IOVCC	-0.3	4.6	V	
Operating temperature	TOPR	-20	70	℃	
Storage temperature	TSTR	-30	80	℃	

6. Electrical Characteristics

Item		Symbol	Rating			Unit	Remark
			Min	Typ	Max		
Supply voltage		VCC	2.5	2.8	3.6	V	Note1
Supply voltage		IOVCC	1.65	1.8	3.3	V	
Input Voltage	L level	VIL	0	---	0.3*IOVCC	V	
	H level	VIH	0.7*IOVCC	---	IOVCC	V	

7. Module Function Description

7-1. Block Diagram Of LCM



7-2. Pin Description

PIN NO.	Symbol	I/O	Description
1	A	P	Power for LED backlight anode
2	K	P	Power for LED backlight cathode
3	K	P	Power for LED backlight cathode
4	VCC	P	power supply
5	IOVCC	P	power supply
6	RST	I	The external reset input
7	TE	O	For IC Test. Leave the pin open when not in use.
8	PWM	O	The PWM frequency output for LCD driver control.
9	GND	P	Ground
10	D0P	I	MIPI DSI differential data pair
11	D0N	I	MIPI DSI differential data pair
12	GND	P	Ground
13	D1P	I	MIPI DSI differential data pair
14	D1N	I	MIPI DSI differential data pair
15	GND	P	Ground
16	CLKP	I	MIPI DSI differential clock pair
17	CLKN	I	MIPI DSI differential clock pair
18	GND	P	Ground
19	NC		
20	NC		
21	GND	P	Ground
22	NC		
23	NC		
24	GND	P	Ground
25	TP_INT	I	Interrupt signal

26	TP_SDA	I	Serial data input/output bidirection pin
27	TP_SCL	I	Serial clock pin
28	TP_RST	I	Reset signal pin
29	TP_VCC	P	power supply
30	TP_VCC	P	power supply

7-3 Timing Characteristics

7.5.4.1 High Speed Mode

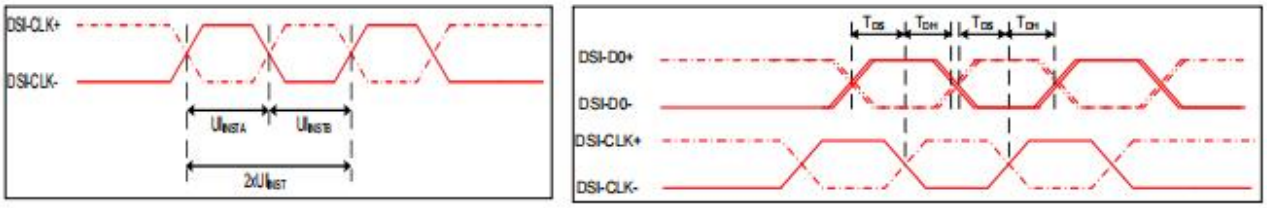


Figure 4 DSI clock channel timing

Figure 5 Rising and falling time on clock and data channel

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 °C

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-CLK+/-	$2xUI_{INSTA}$	Double UI instantaneous	2.5	25	ns	
DSI-CLK+/-	UI_{INSTA} UI_{INSTB}	UI instantaneous halfs	1.25	12.5	ns	$UI = UI_{INSTA} = UI_{INSTB}$
DSI-Dn+/-	tDS	Data to clock setup time	0.15	-	UI	
DSI-Dn+/-	tDH	Data to clock hold time	0.15	-	UI	

Table 7 Mipi Interface- High Speed Mode Timing Characteristics

7.5.4.2 Lowe Power Mode

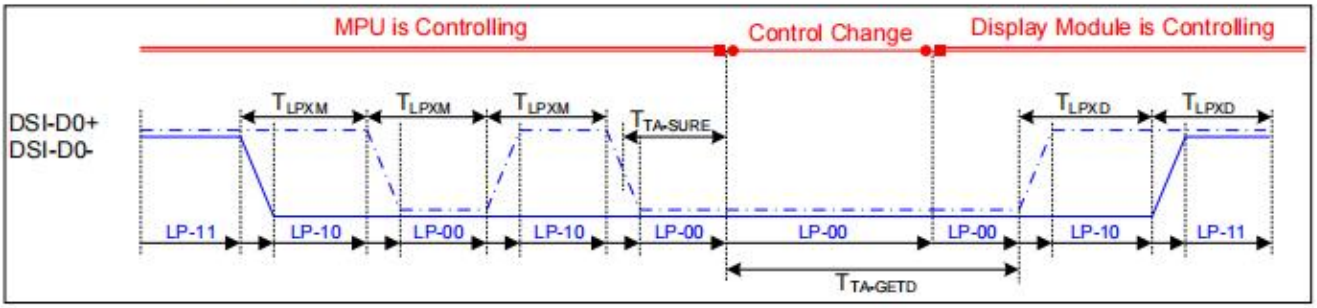


Figure 6 Bus Turnaround (BTA) from display module to MPU Timing

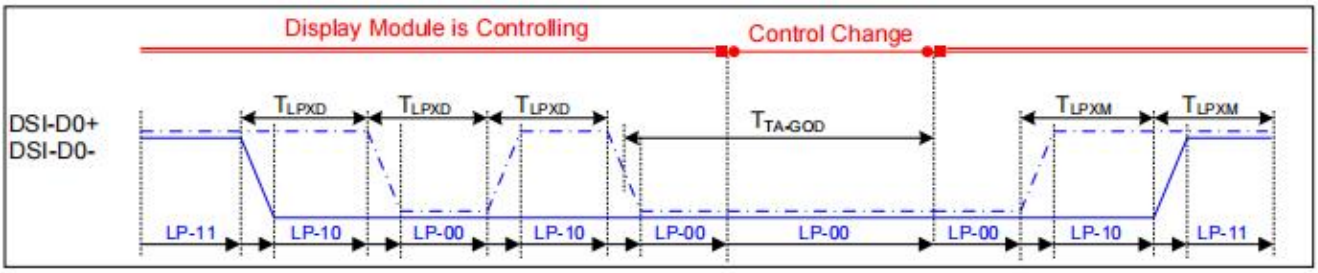


Figure 7 Bus Turnaround (BTA) from MPU to display module Timing

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-D0+/-	TLPXM	Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Input
DSI-D0+/-	TLPXD	Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Output
DSI-D0+/-	TTA-SURED	Time-out before the MPU start driving	T_{LPXD}	$2xT_{LPXD}$	ns	Output
DSI-D0+/-	TTA-GETD	Time to drive LP-00 by display module	$5xT_{LPXD}$		ns	Input
DSI-D0+/-	TTA-GOD	Time to drive LP-00 after turnaround request-MPU	$4xT_{LPXD}$		ns	Output

Table 8 Mipi Interface Low Power Mode Timing Characteristics

7.5.4.3 DSI Bursts Mode

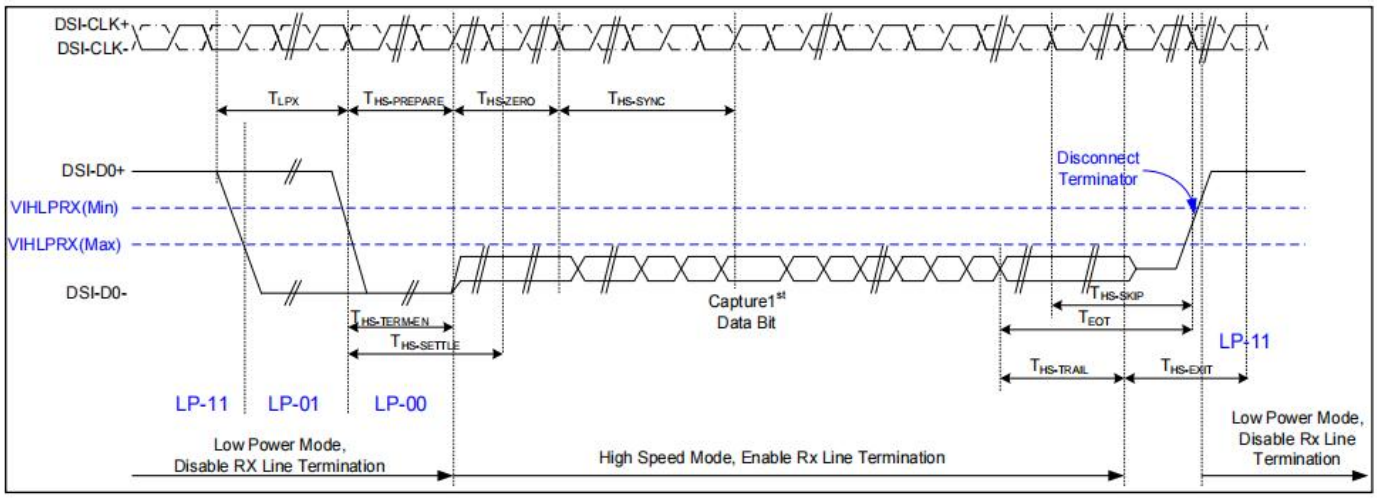


Figure 7 Data lanes-Low Power Mode to/from High Speed Mode Timing

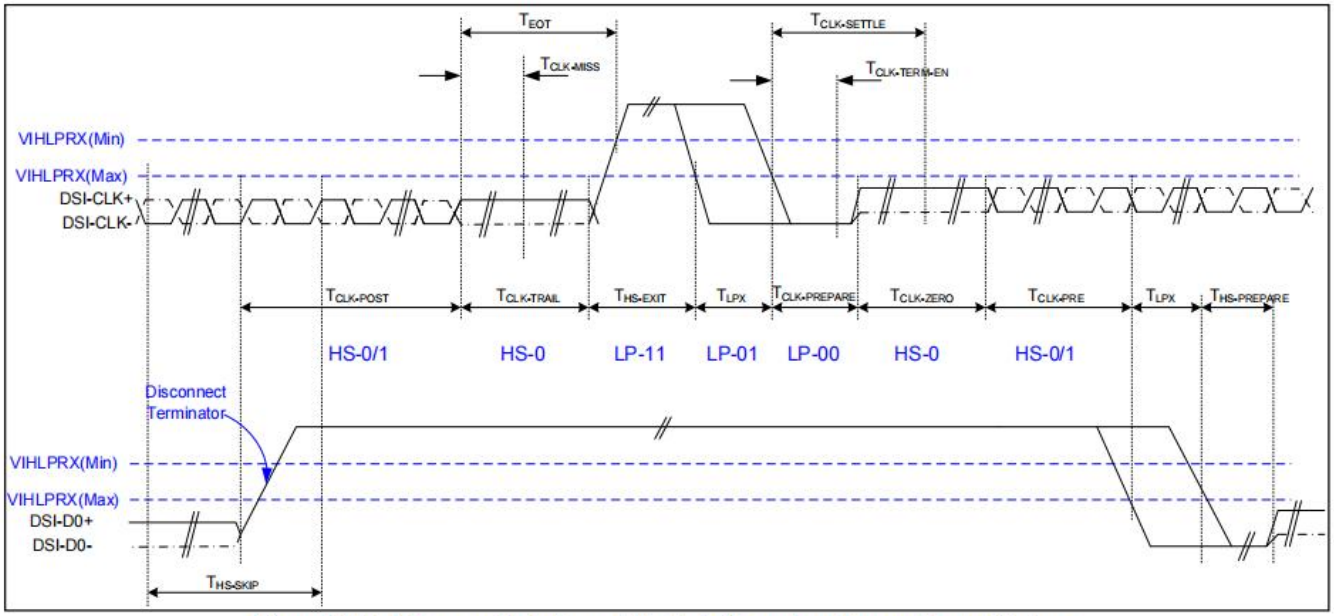


Figure 8 Clock lanes- High Speed Mode to/from Low Power Mode Timing

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
Low Power Mode to High Speed Mode Timing						
DSI-Dn+/-	TLPX	Length of any low power state period	50	-	ns	Input
DSI-Dn+/-	THS-PREPARE	Time to drive LP-00 to prepare for HS transmission	40+4 UI	85+6 UI	ns	Input
DSI-Dn+/-	THS-TERM-EN	Time to enable data receiver line termination measured from when Dn crosses VILMAX	-	35+4 UI	ns	Input
DSI-Dn+/-	THS-PREPARE + THS-ZERO	THS-PREPARE + time to drive HS-0 before the sync sequence	140+ 10UI	-	ns	Input
High Speed Mode to Low Power Mode Timing						
DSI-Dn+/-	THS-SKIP	Time-out at display module to ignore transition period of EoT	40	55+4 UI	ns	Input
DSI-Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-Dn+/-	THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4 UI	-	ns	Input
High Speed Mode to/from Low Power Mode Timing						
DSI-CLK+/-	TCLK-POS	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+5 2UI	-	ns	Input
DSI-CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns	Input
DSI-CLK+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS transmission	38	95	ns	Input
DSI-CLK+/-	TCLK-TERM-EN	Time-out at clock lan display module to enable HS transmission	--	38	ns	Input
DSI-CLK+/-	TCLK-PREPARE + TCLK-ZERO	Minimum lead HS-0 drive period before starting clock	300	-	ns	Input
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8UI	-	ns	Input
DSI-CLK+/-	TEOT	Time form start of TCLK-TRAIL period to start of LP-11 state	-	105n s+12 UI	ns	Input

7-4 Reset Timing

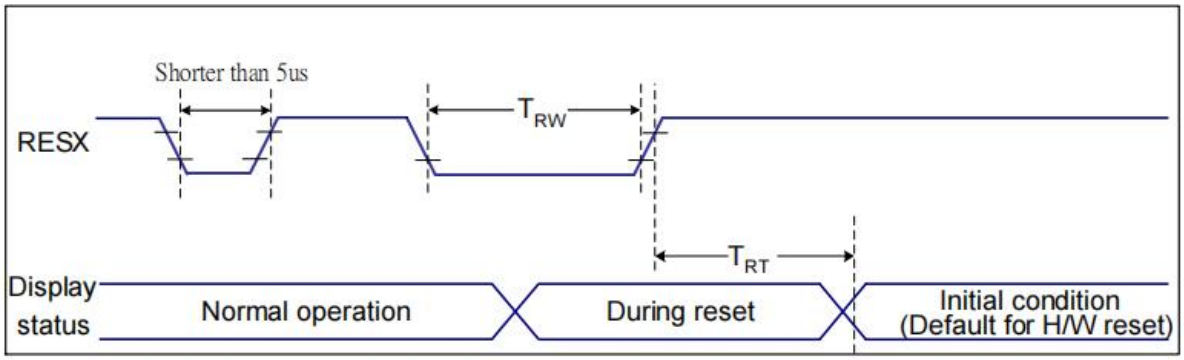


Figure 9 Reset Timing

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120(Note 1, 6, 7)	ms

Table 9 Reset Timing

Notes:

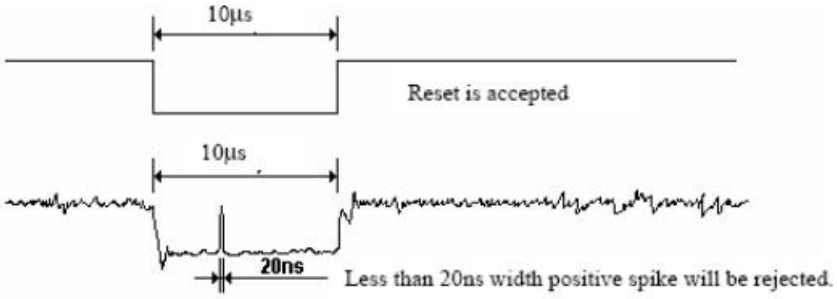
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

8. Electro-Optical Characteristics

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time		Tr +Tf	θx = θy =0	---	35	40	ms	Note 1
Contrast Ratio		CR		1000	1200	---	---	Note 2
Transmittance		T%		3.91	4.6	---	%	
Color Chromaticity (CIE1931)	White	W x	θx = θy =0	---	0.298	---	---	
		W y		---	0.327	---	---	
Viewing angle	θ_T		CR > 10	80	85	---	Deg.	Note 3
	θ_B			80	85	---		
	θ_L			80	85	---		
	θ_R			80	85	---		
Luminance (I_F = 80mA)		L		--	TBD	---	cd/m2	Note4

Notes : 1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see FIGURE 1).

2. Contrast measurements shall be made at viewing angle of Θ= 0 and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state . (see FIGURE 1) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Transmittance is the Value with Polarizer(HC+Clear) & silicate BLU (Film structure is on Table 5.1) .

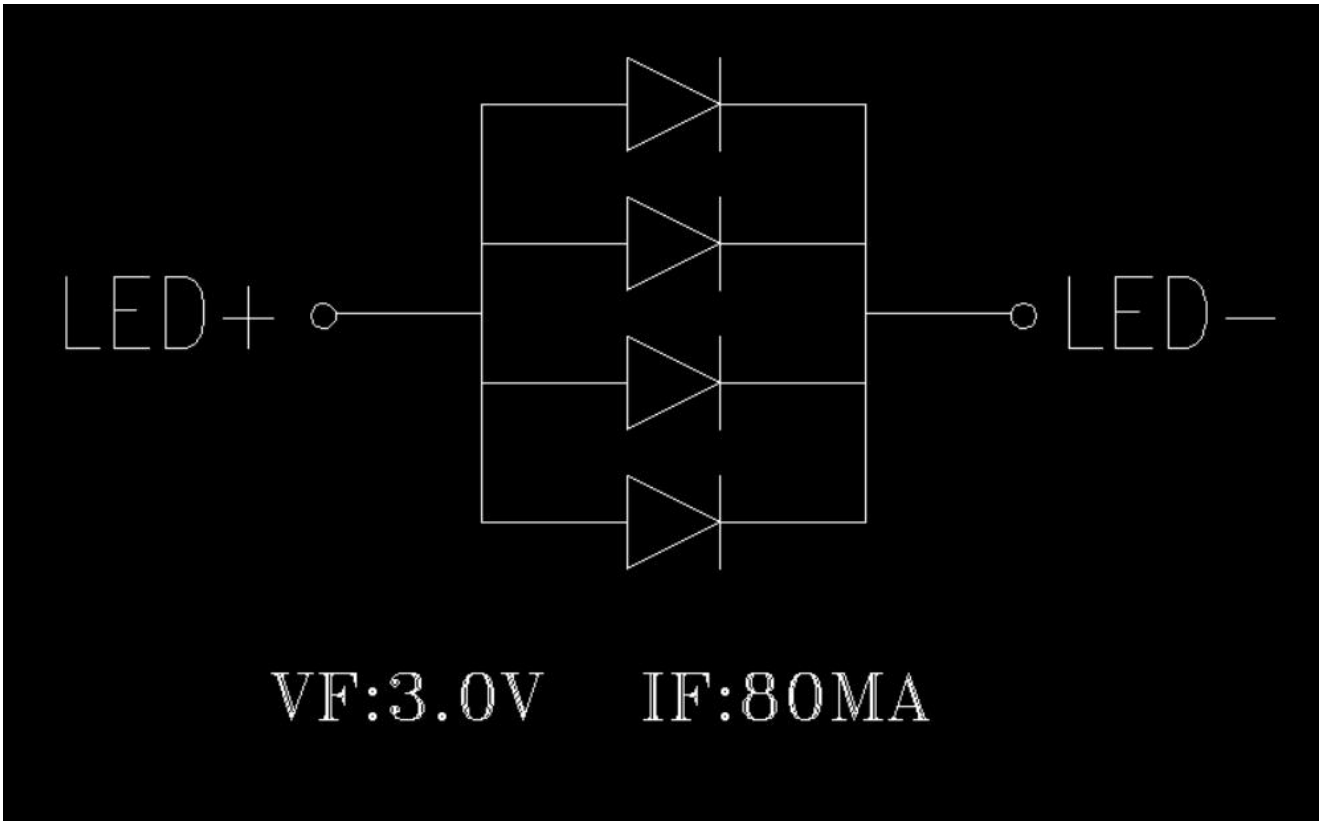
遮光	Soken	SK8906B
BEF	光耀	SG43+QG42
DIF	Kimoto	38TMQ
LGP	住友	TR1801A
REF	丽光	75W28
胶铁	乐天	LB1010W
LED	AOT	3004 Silicate

Table 5

4. The color chromaticity coordinates specified in Table 5. shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the CF and based on C Light

5. The electro-optical response time measurements shall be made as FIGURE 2. The times needed for the luminance to change from 10% to 90% is Tr, and 90% to 10% is Tf.

Note(4) Backlight circuit



9.Records Of Version

Version	Revise Date	Page	Content
00		ALL	New released