PRODUCT SPECIFICATION FOR LCD MODULE

Revision: 1.0

Model No: LS035I15-R-V1

Module Type: COG+FPC+B/L

APPROVED SIGNATURE

■ Approved Product Specification only

□ Approved Product Specification and Samples

Prepared By	Checked By	Approved By

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1. General Description

LS035I15-R-V1 is a transmissive type a-Si TFT-LCD (amorphous silicon thin film transistor liquid crystal display) module, which is composed of a TFT-LCD panel, a driver circuit and a backlight unit. The panel size is 3.45 inch and the resolution is 640(RGB)*480, the panel can display up to 16.7M colors.

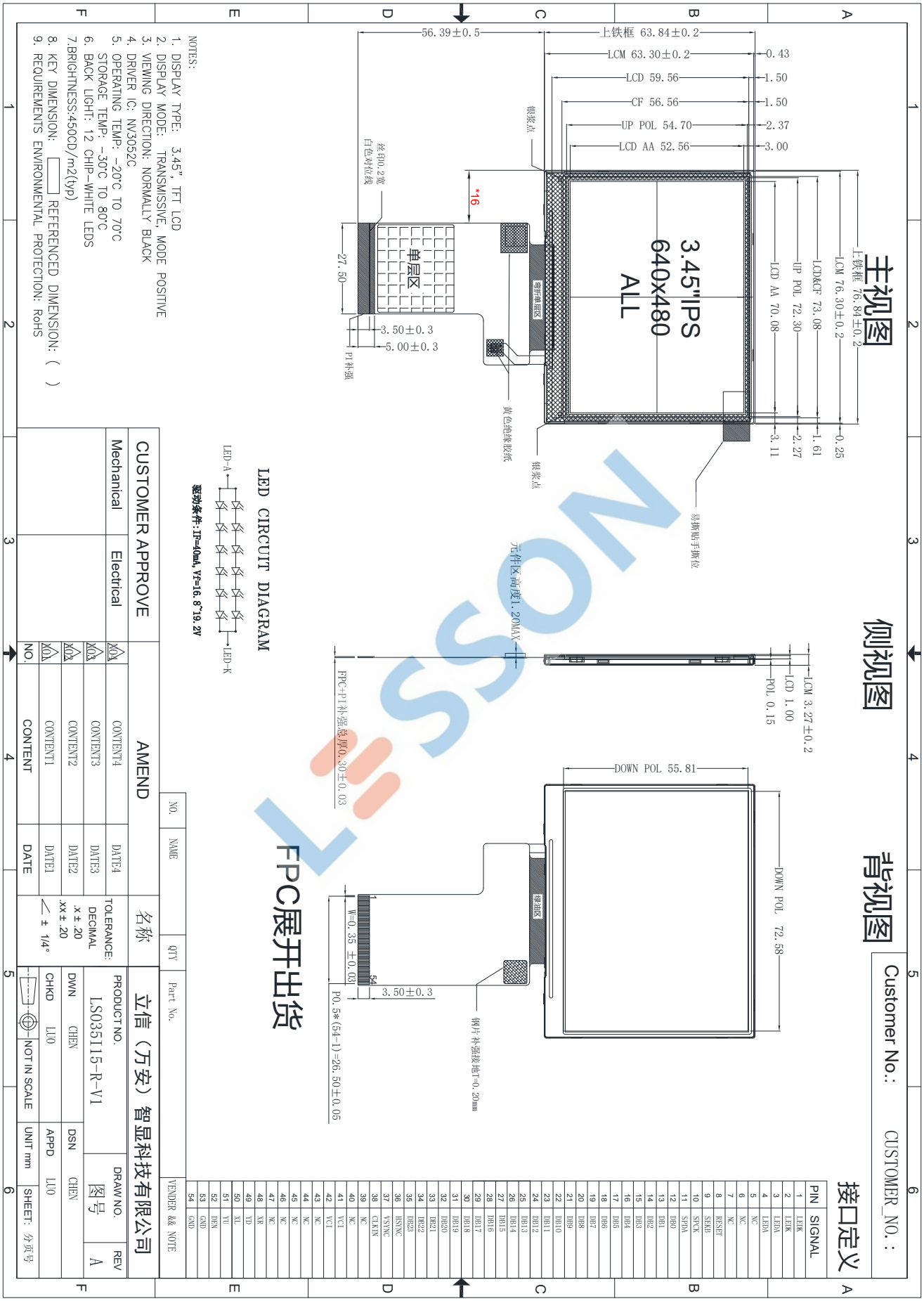
2. Physical Features

Display Mode	TFT-LCD Module
	Active matrix TFT, Transmissive type
Display Format	Graphic 640(RGB)×480 Dot-matrix
Input Data	24bit RGB
Viewing Direction （Grayscale Inversion）	Free（IPS）
Drive	NV3052C

3. Mechanical Specification

Item	Specification	Unit
LCM+LENS Module size (H×V×D)	76.84 ×63.84×3.27	mm
Number of dots	640(RGB) ×480	pixel
Active area (H×V)	70.08×52.56	mm

4. Outline Dimensio



5. Absolute Maximum Ratings

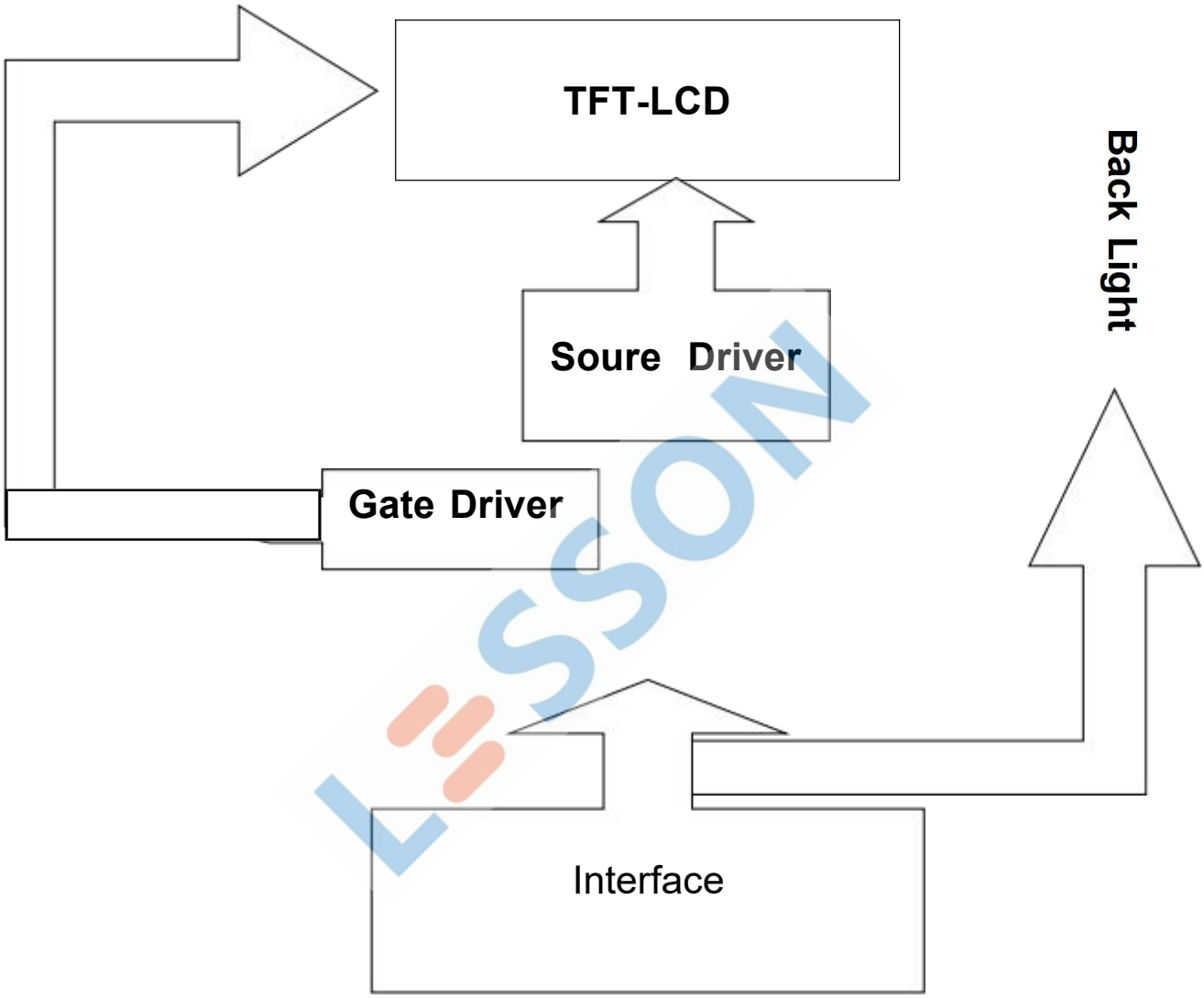
Item	Symbol	Min	Max	Unit	Remark
Supply voltage	VDD	-0.3	6.6	V	
Supply voltage	IOVCC	---	---	V	
Operating temperature	TOPR	-20	70	℃	
Storage temperature	TSTR	-30	80	℃	

6. Electrical Characteristics

Item		Symbol	Rating			Unit	Remark
			Min	Typ	Max		
Supply voltage		VDD	2.5	2.8	3.3	V	Note1
Supply voltage		IOVCC	---	---	---	V	
Input Voltage	L level	VIL	0	---	0.3*IOVCC	V	
	H level	VIH	0.7*IOVCC	---	IOVCC	V	

7. Module Function Description

7-1. Block Diagram Of LCM

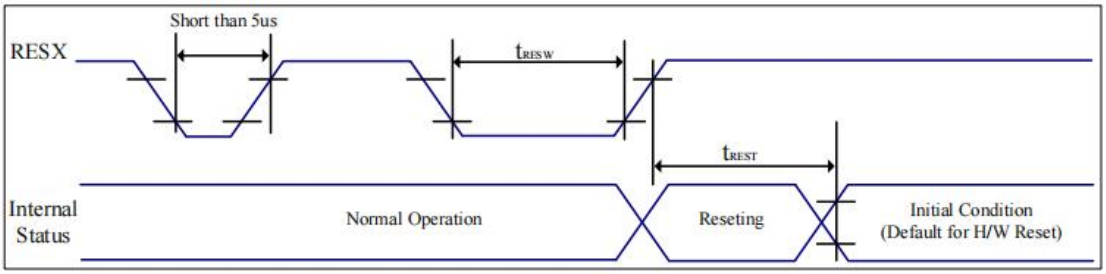


7-2. Pin Description

Pin No.	Symbol	Description
1-2	LEDK	POWER SUPPLY- FOR BACKLIGHT CATHODE
3-4	LEDA	POWER SUPPLY+ FOR BACKLIGHT ANODE
5-6	NC	NC
7	NC	NC
8	RESET	RESET
9	SEKB	3-WIRE COMMUNICATION ENABLE.
10	SPCK	3-WIRE COMMUNICATION CLOCK INPUT. RISING EDGE LATCH.
11	SPDA	3-WIRE COMMUNICATION DATA INPUT/OUTPUT.
12-35	DB0-DB23	24-BIT MODE: DB[0:7]=B[0:7] ; DB[8:15]=G[0:7] ; DB [16:23]=R[0:7] DATA.
36	HSYNC	Horizontal sync. Signal in RGB I/F
37	VSYNC	Vertical sync. Signal in RGB I/F
38	DCLK	Pixel clock signal in RGB I/F
39-40	NC	NC
41-42	VDD	POWER SUPPLY
43-47	NC	NC
48	XR	XR
48	YD	YD
50	XL	XL
51	YU	YU
52	DE	Data enable signal in RGB I/F mode 1
53	GND	GND
54	GND	GND

7-3 Timing Characteristics

7.3.1. Reset timing characteristics



VSS=0V, IOVCC=1.65V to 3.6V, VCI=2.5V to 6.0V,Ta = -30℃ to 85℃

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse width	RESX	10	-	-	-	us
t_{REST}	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-	-	-	120	When reset applied during Sleep out mode	ms

Table: Reset input timing

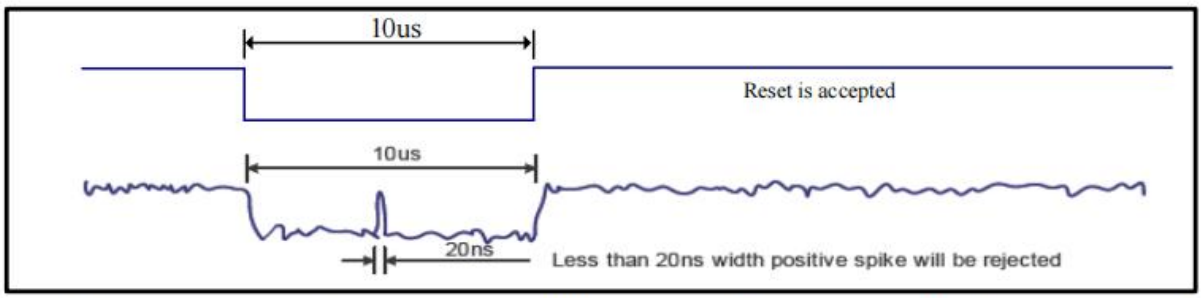
Note 1: Due to an electrostatic discharge on RESX line,spike does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts (It depends on voltage and temperature condition.)

Note 2: During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120ms, when Reset Starts in Sleep Out mode. The display remains the blank state in Sleep In mode) , then return to default condition for H/W reset.

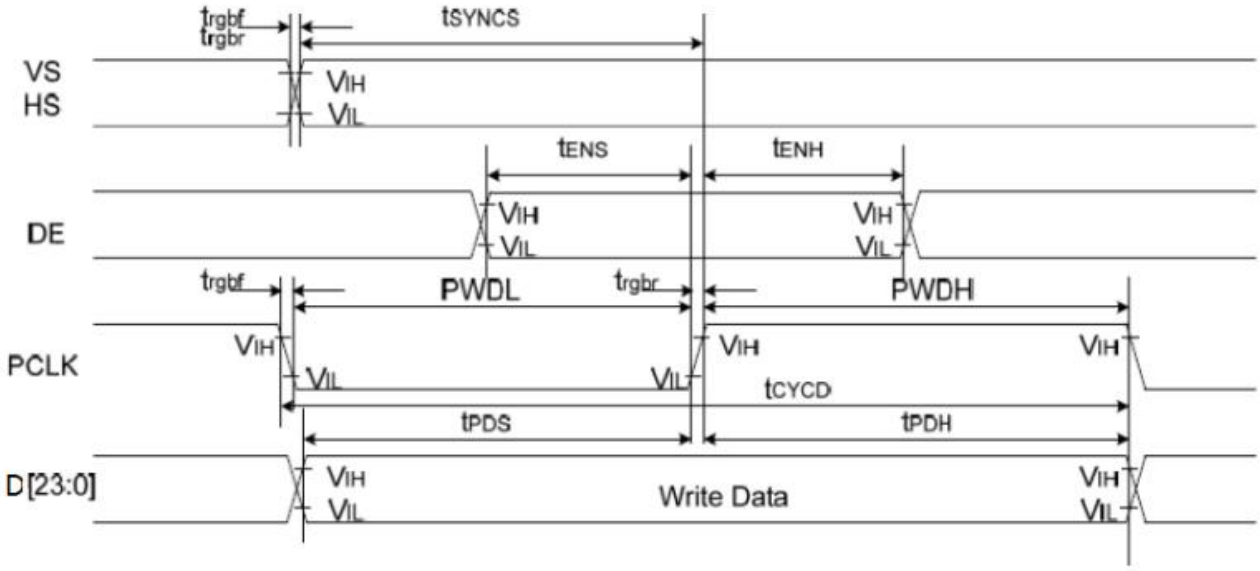
Note 3: During Reset Complete Time, ID1/ID2/ID3 and VCOM value in OTP will be latched to internal register. After a rising edge of RESX, there is a H/W reset complete time (Trest) which lasted 5ms..The loading operation will be done every time during this reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:



Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120 msec.

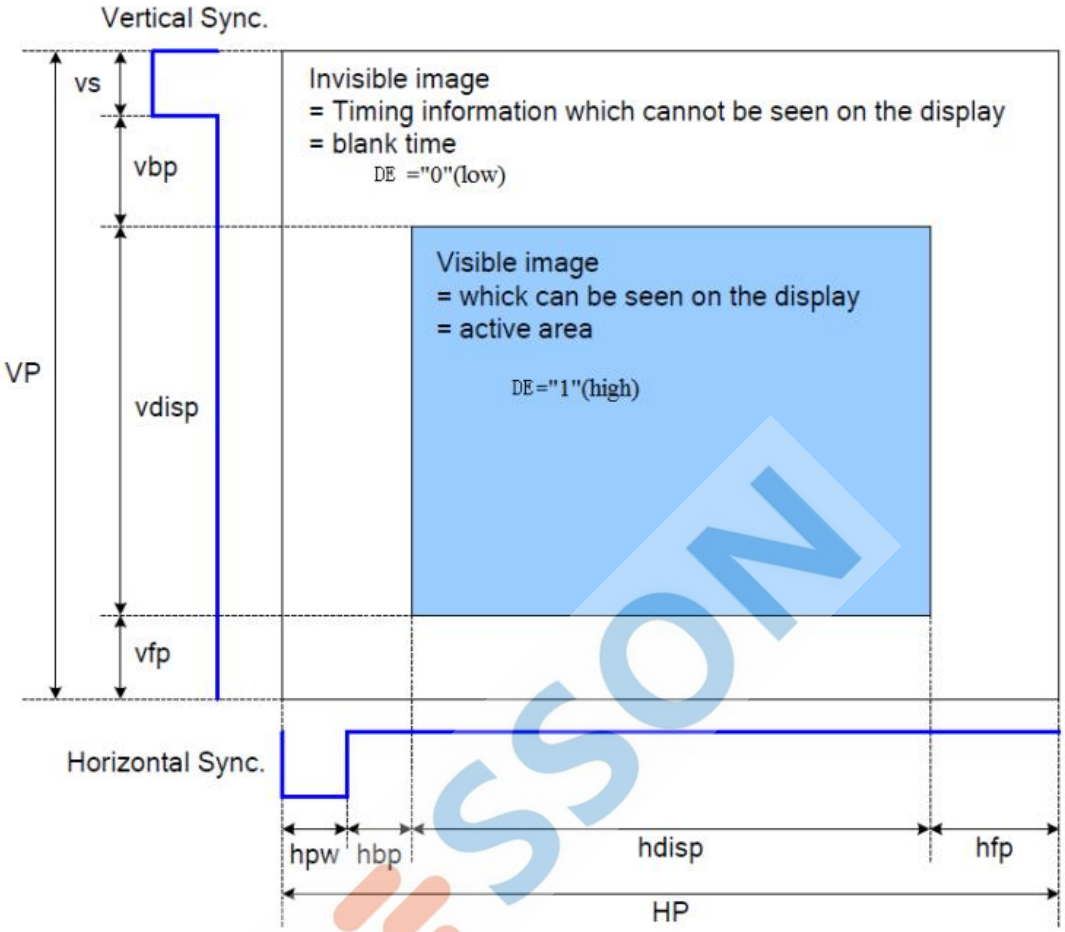
7.3.2. Parallel 24/18/16-bit RGB Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VS/HS	tSYNCS	VS/HS setup time	5	-	ns	24/18/16-bit bus RGB interface mode
	tSYNCH	VS/HS hold time	5	-	ns	
DE	tENS	DE setup time	5	-	ns	
	tENH	DE hold time	5	-	ns	
D[23:0]	tPOS	Data setup time	5	-	ns	
	tPDH	Data hold time	5	-	ns	
PCLK	PWDH	PCLK high-level period	7	-	ns	
	PWDL	PCLK low-level period	7	-	ns	
	tCYCD	PCLK cycle time	14	-	ns	
	trgbr,trgbf	PCLK,HS,VS rise/fall time	-	15	ns	

Note 1: IOVCC=1.65 to 3.6V, VCI=2.5 to 6V, VSSA=VSS=0V, Ta=-30 to 85℃

D[23:0] are used to tell what is the information of the image that is transferred on the display(When DE= ’0’ (low) and there is a rising edge of PCLK). D[23:0] can be ‘0’ (low) or ‘1’(high). These lines are read by a rising edge of the PCLK signal.



DRAM Access Area by RGB Interface

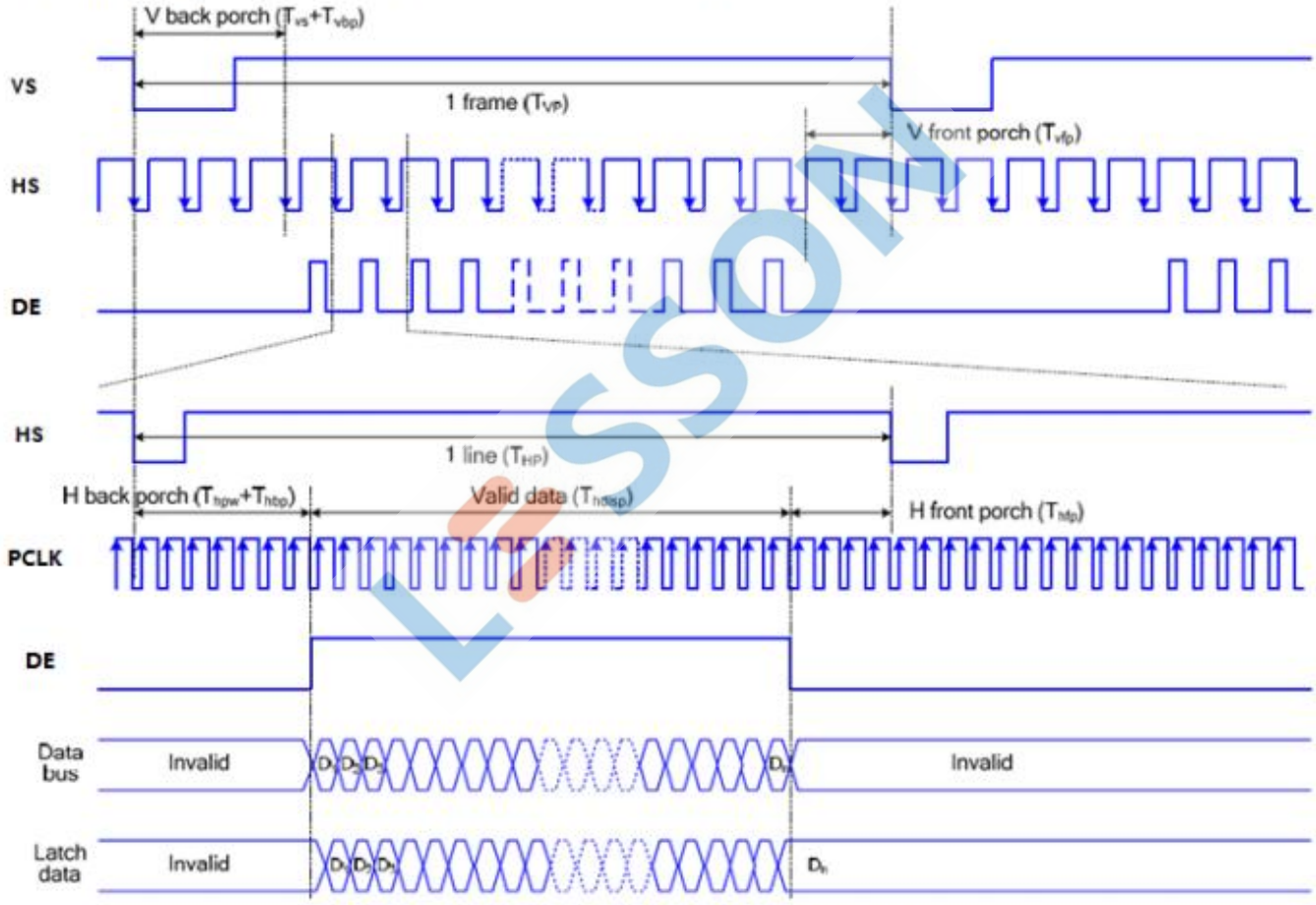
6.1.2 RGB Interface Mode Selection

NV3052CGRB supports two kinds of RGB interface, DE mode and SYNC mode.The table shown below uses command 23h to select RGB interface mode.

sync_mode[1:0]	RGB Mode
00	SYNC+DE mode
01	SYNC mode
10	DE mode
11	SYNC+DE mode

6.1.3 RGB Interface Timing

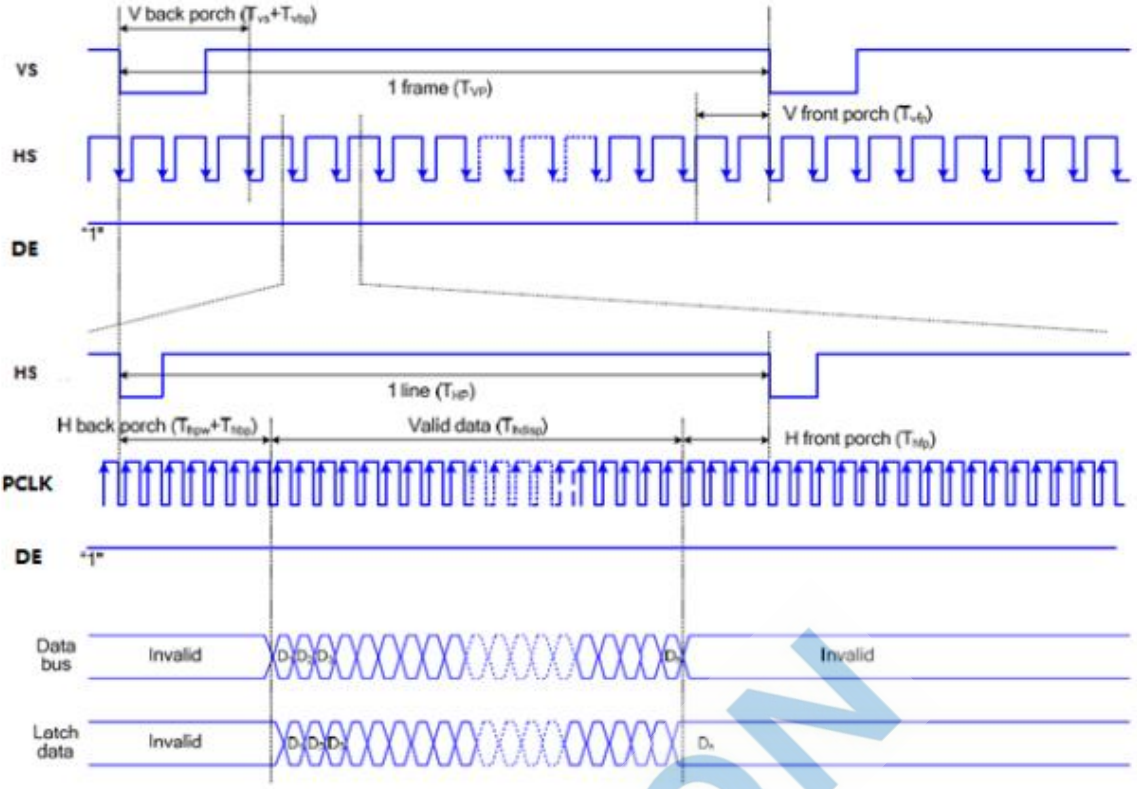
The timing chart of RGB interface DE mode is shown as follows.



Timing Chart of Signals in RGB Interface DE Mode

Note: The setting of front porch and back porch in host must match that in IC as this mode.

The timing chart of RGB interface SYNC mode is shown as follows.



Timing chart of RGB interface SYNC mode

Below Table provide the timing parameter by external Vertical-cycle

(Resolution for 720/640 horizontal x 1280 vertical display with Frame-Rate of 60Hz)

Parameters	Symbols	Min.	Typ	Max.	Unit
Horizontal Synchronization	hpw	-	2	-	PCLK
Horizontal Back Porch	hbp	-	42	-	PCLK
Horizontal Front Porch	hfp	-	44	-	PCLK
Hsync+ HBP+ HFP	-	-	88*Note1	-	PCLK
Horizontal Address (Display area)	hdisp	-	720	-	PCLK
Horizontal cycle	-	-	12.703	-	us
Vertical Synchronization	VS	-	2	-	Line
Vertical Back Porch	vbp	-	14	-	Line
Vertical Front Porch	vfp	-	16	-	Line
Vsync+ VBP+ VFP	-	-	32	-	Line
Vertical Address (Display area)	vdisp	-	1280	-	Line
Vertical cycle	-	-	16.66	16.181	ms
Frame-Rate	-	-	60	61.8	Hz

"-" means no limit.

Note : 1. If using Image Process Algorithm, Type value for H-blanking is minimum requirement.

7.3.3. Serial interface characteristics (SPI)

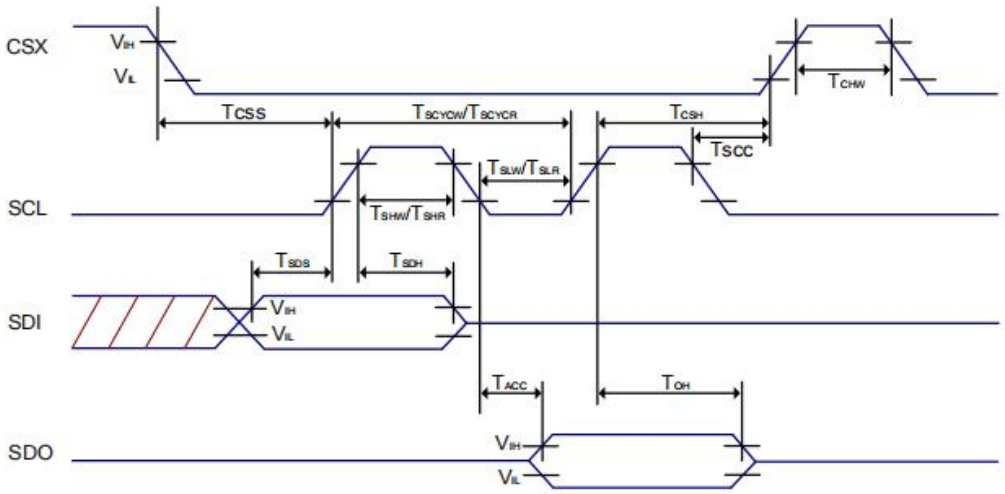


Figure: 3-pin Serial Interface Characteristics

Table: SPI Interface Characteristics

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time	15	-	ns	-
	T_{CSH}	Chip select hold time	15	-	ns	
	T_{SCC}	Chip select setup time	20	-	ns	
	T_{CHW}	Chip "H" pulse width	40	-	ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66	-	ns	-
	T_{SHW}	SCL "H" pulse width (Write)	10	-	ns	
	T_{SLW}	SCL "L" pulse width (Write)	10	-	ns	
	T_{SCYCR}	Serial clock cycle (Read)	150	-	ns	-
	T_{SHR}	SCL"H" pulse width (Read)	60	-	ns	
	T_{SLR}	SCL"L" pulse width (Read)	60	-	ns	
SDI	TSDS	Data setup time	10	-	ns	-
	T_{SDH}	Data hold time	10	-	ns	
	T_{ACC}	Access time	10	50	ns	For maximum C_L=30pF For minimum C_L=8pF
	T_{OH}	Output disable time	15	50	ns	

Note 1: IOVCC=1.65 to 3.6V, VCI=2.5 to 6V, VSSA=VSS=0V, Ta=-30 to 85℃

Note 2: The rise time and fall time (tr, tf) of input signal is specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

8. Electro-Optical Characteristics

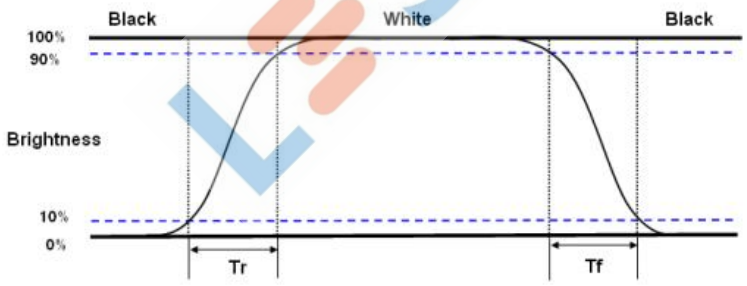
Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time		Tr +Tf	θx = θy =0	---	25	50	ms	Note 1
Contrast Ratio		CR		600	800	---	---	Note 2
Transmittance		T%		3.7	4.4	---	%	
Color Chromaticity (CIE1931)	White	W x	θx = θy =0	---	0.297	---	---	
		W y		---	0.317	---	---	
Viewing angle	θ_T		CR > 10	75	85	---	Deg.	Note 3
	θ_B			75	85	---		
	θ_L			75	85	---		
	θ_R			75	85	---		
LCM Luminance (I_F = 40mA)		L		---	450	---	cd/m2	Note4

Note 1: Measuring Conditions:

The optical characteristics are determined after the unit has been 'ON' and stable at the maximum brightness, in a dark environment at an ambient temperature at 25°C ± 2°C.

Note 2: Definition of response time:

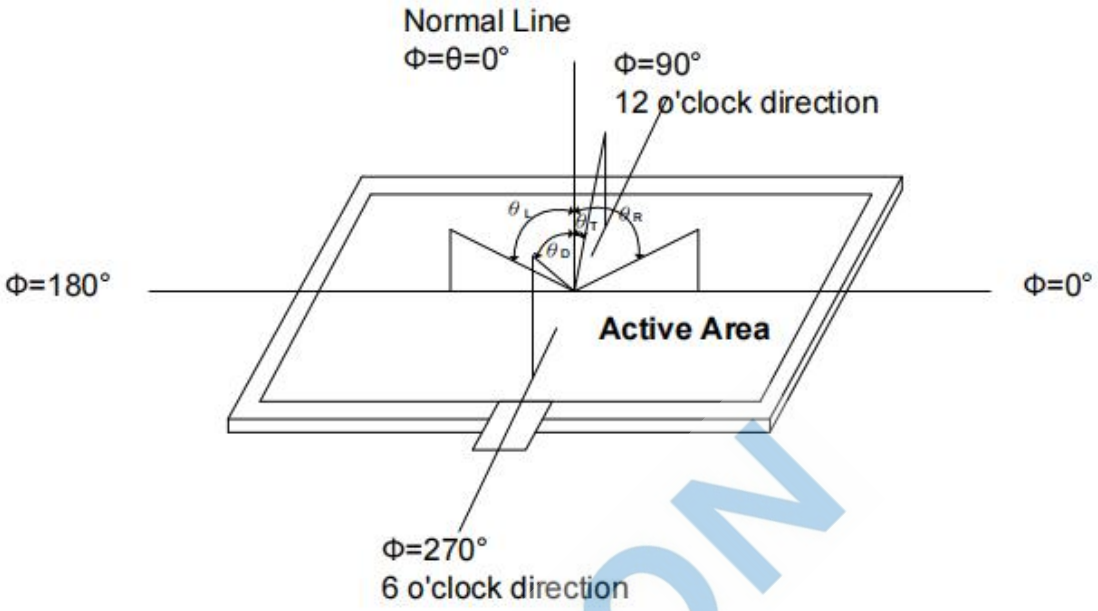
The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time is the time between photo detector output intensity changed from 10% to 90%. And fall time is the time between photo detector output intensity changed from 90% to 10%.



Note 3: Definition of contrast ratio:

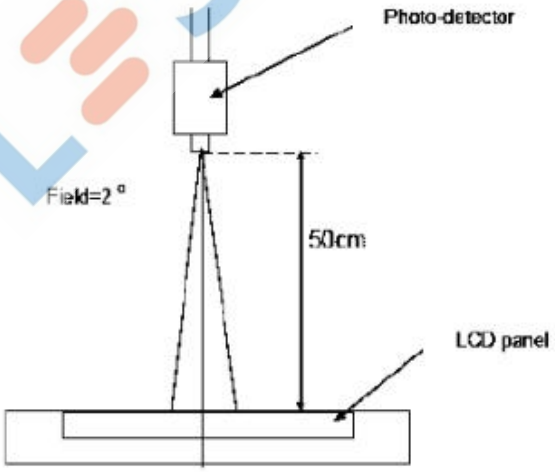
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the " White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 4: Definition of viewing angle



Note 5: Optical characteristic measurement setup.

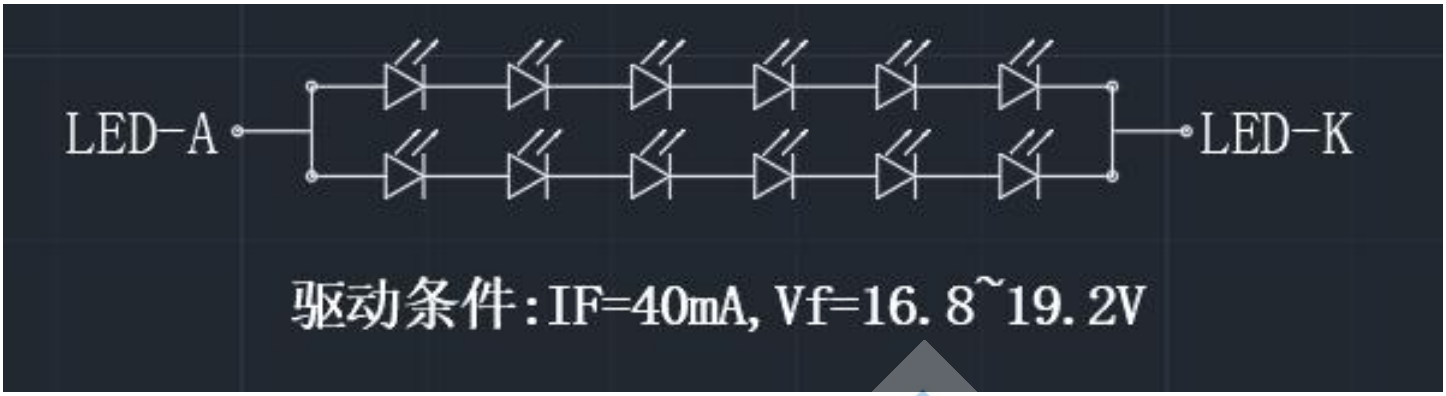
The LCD module should be stabilized at given temperature for 10 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 10 minutes in a windless room.



Note 6: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

Note(4) Backlight circuit



9.Records Of Version

Version	Revise Date	Page	Content
00	2025-12-23	ALL	New released