PRODUCT SPECIFICATION FOR LCD MODULE

Revision: 1.0

Model No: LS035I06-M-V1

Module Type: COG+FPC+B/L

APPROVED SIGNATURE

■ Approved Product Specification only

□ Approved Product Specification and Samples

Prepared By	Checked By	Approved By

Contents

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1. General Description

LS035I06-M-V1 is a transmissive type a-Si TFT-LCD (amorphous silicon thin film transistor liquid crystal display) module, which is composed of a TFT-LCD panel, a driver circuit and a backlight unit. The panel size is 3.5 inch and the resolution is 320(RGB)*480, the panel can display up to 16.7M colors.

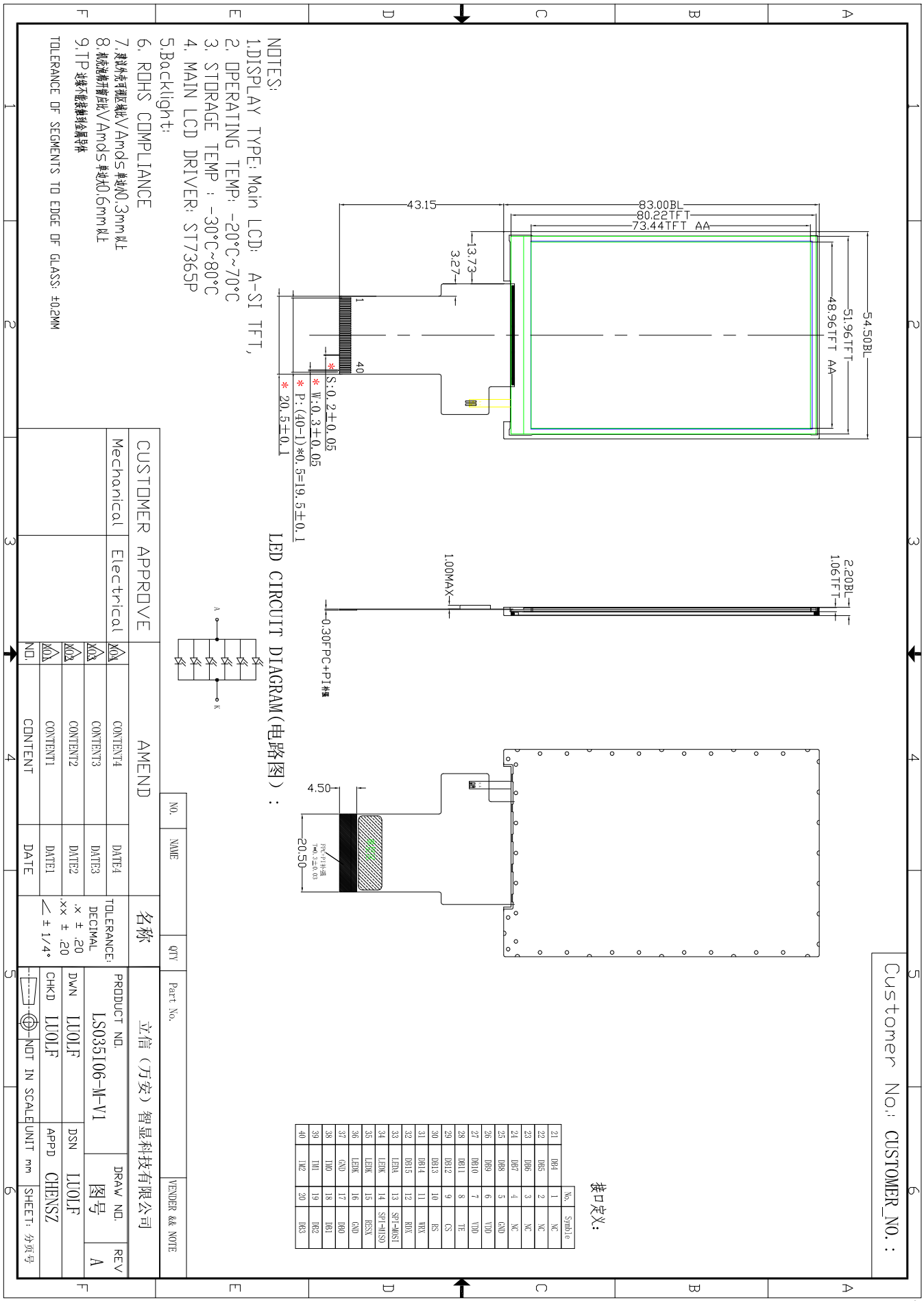
2. Physical Features

Display Mode	TFT-LCD Module
	Active matrix TFT, Transmissive type
Display Format	Graphic 320(RGB)×480 Dot-matrix
Input Data	8080/SPI
Viewing Direction （Grayscale Inversion）	Free（IPS）
Drive	ST7365P

3. Mechanical Specification

Item	Specification	Unit
Module size (H×V×D)	54.5 ×83.0 ×2.2	mm
Number of dots	320(RGB) ×480	pixel
Active area (H×V)	48.96×73.44	mm

4. Outline Dimension



No.	Symbole
1	NC
2	NC
3	NC
4	NC
5	GND
6	VDD
7	VDD
8	TE
9	CS
10	RS
11	WRX
12	RDX
13	SPI-MOSI
14	SPI-MISO
15	RESX
16	GND
17	DD0
18	DD1
19	DD2
20	DD3
21	DB4
22	DB5
23	DB6
24	DB7
25	DB8
26	DB9
27	DB10
28	DB11
29	DB12
30	DB13
31	DB14
32	DB15
33	LEDA
34	LEDK
35	LEDK
36	LEDK
37	GND
38	IM0
39	IM1
40	IM2

5. Absolute Maximum Ratings

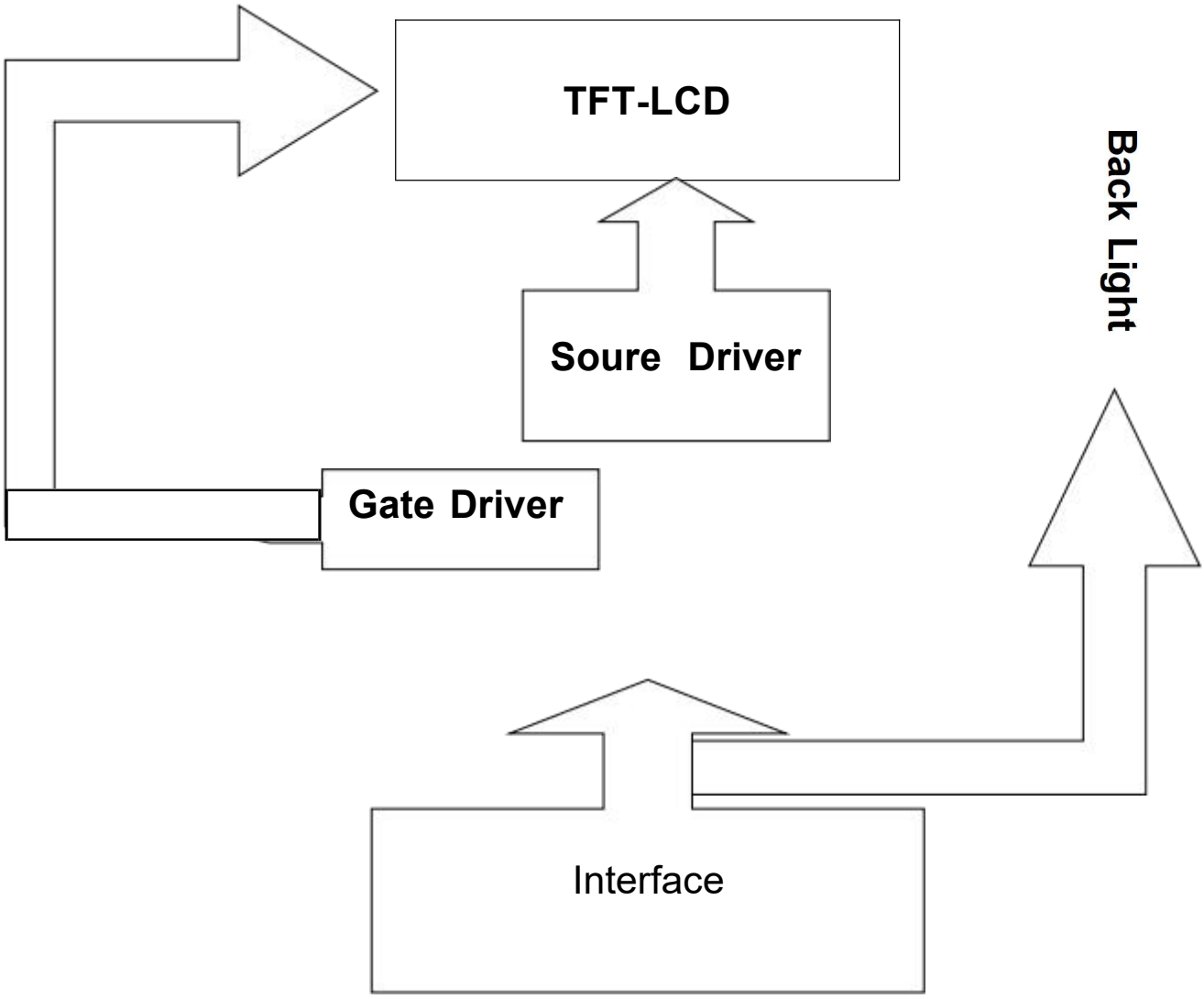
Item	Symbol	Min	Max	Unit	Remark
Supply voltage	VCC	-0.3	4.6	V	Note1 Note2
Supply voltage	IOVCC	-0.3	4.0	V	
Operating temperature	TOPR	-10	60	℃	
Storage temperature	TSTR	-20	70	℃	

6. Electrical Characteristics

Item		Symbol	Rating			Unit	Remark
			Min	Typ	Max		
Supply voltage		VCC	2.4	2.75	3.3	V	Note1
Supply voltage		IOVCC	1.65	1.8	3.3	V	
Input Voltage	L level	VIL	0	---	0.3*IOVCC	V	
	H level	VIH	0.7*VCC	---	IOVCC	V	

7. Module Function Description

7-1. Block Diagram Of LCM



7-2. Pin Description

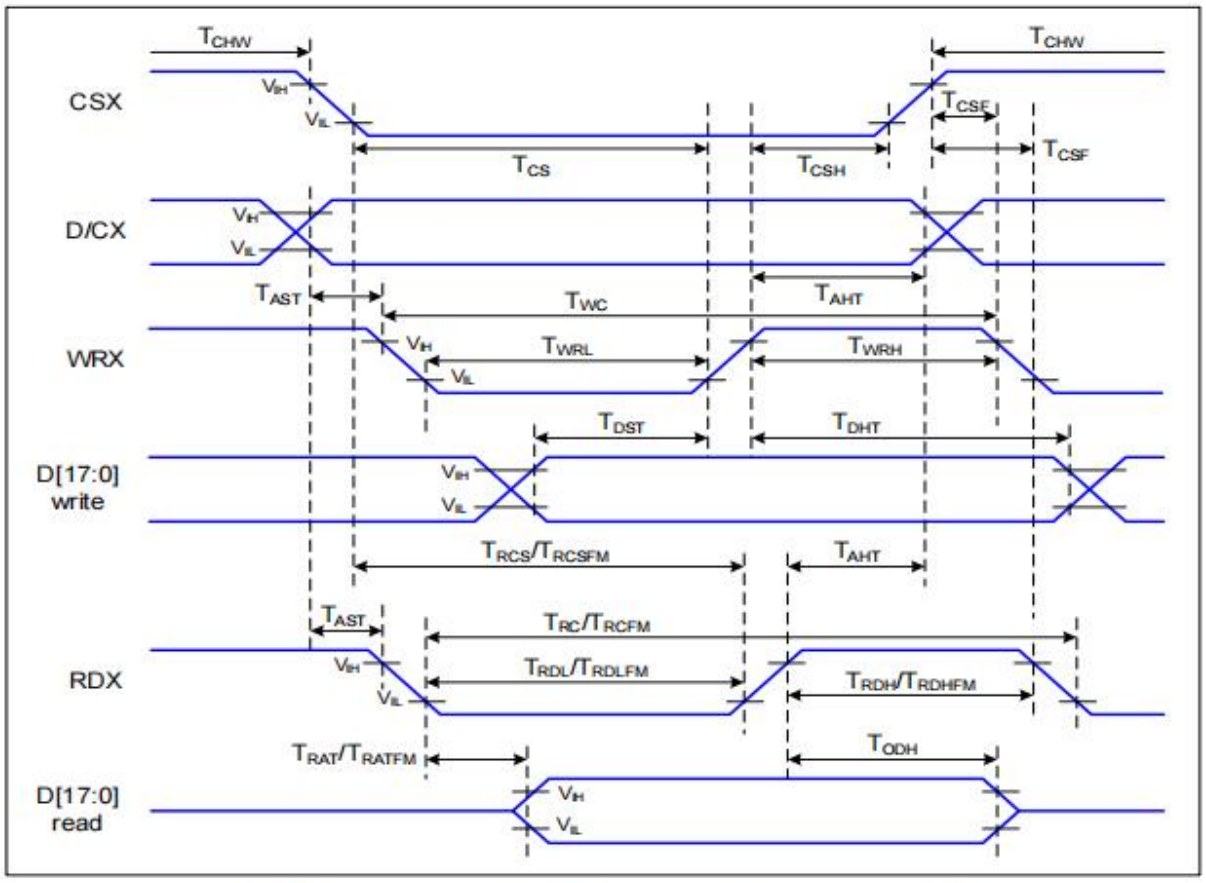
PIN NO.	Symbol	I/O	Description
1	NC		
2	NC		
3	NC		
4	NC		
5	GND	P	System ground
6	VDD	P	Power supply
7	VDD	P	Power supply
8	TE	O	Tearing effect output.
9	CS	I	- Chip selection pin. Low-active. - If not used, please fix this pin at VDDI or DGND level.
10	RS	I	Display data/command selection (RS) pin in MCU interface. DCX='1': display data or parameter. DCX='0': register index / command. - If not used, please fix this pin at VDDI or DGND level.
11	WR	I	Write enable in MCU parallel interface. - In SPI mode, this pin is used as SCL. - If not used, please fix this pin at VDDI or DGND level.
12	RDX	I	Read enable in 8080 MCU parallel interface. Low-active. - If not used, please fix this pin at VDDI or DGND level
13	SDA	I	SPI interface input/output pin. - The data is latched on the rising edge of the SCL signal. - If not used, please fix this pin at VDDI or DGND level
14	SDO	O	SPI interface output pin. - The data is outputted on the falling edge of the SCL signal. - If not used, please fix this pin at floating
15	REST	I	This signal will reset the device and it must be applied to properly initialize the chip
16	GND	P	System ground
17-32	DB0-DB15	I/O	In MCU 8080 parallel interface, DB[15:0] are used as data bus. 8-bit I/F: DB[7:0] is used. 9-bit I/F: DB[8:0] is used. 16-bit I/F: DB[15:0] is used If not used, please fix this pin at VDDI or DGND level.
33	LEDA	P	Power for LED backlight anode
34	LEDK	P	Power for LED backlight cathode
35	LEDK	P	Power for LED backlight cathode
36	LEDK	P	Power for LED backlight cathode

37	GND	P	System ground
38	IM0	I	-The MCU interface mode select.
39	IM1	I	
40	IM2	I	

IM2	IM1	IM0	MPU Interface Mode	Data pin
[illegible]				
0	0	1	8080 9-bit Interface	DB[8:0]
0	1	0	8080 16-bit Interface	DB[15:0]
0	1	1	8080 8-bit Interface	DB[7:0],
1	0	0	Reserve	--
1	0	1	3SPI	SDA, SDO
[illegible]				
1	1	1	4Line SPI	SDA, SDO

7-3 Timing Characteristics

7.4.1 8080 Series MCU Parallel Interface Characteristics: 18/16/9/8-bit Bus



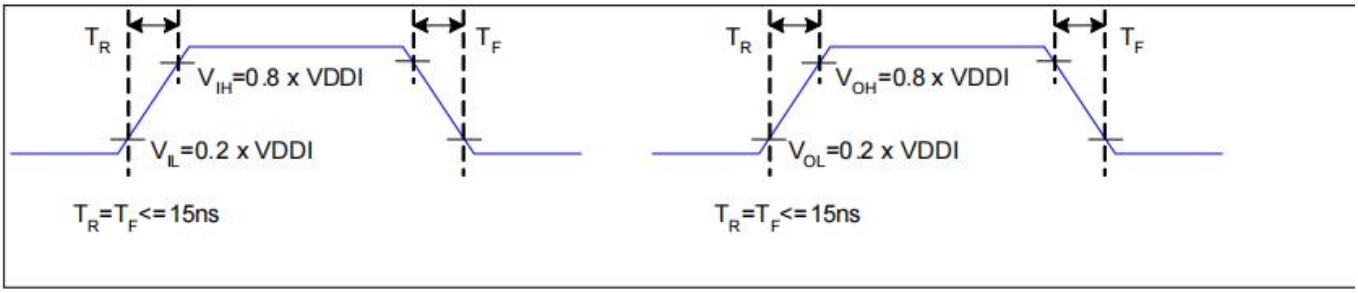
Parallel Interface Timing Characteristics (8080-Series MCU Interface)

VDDI=1.8V,VDDA=2.8V, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T_{AST}	Address setup time	0		ns	-
	T_{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T_{CHW}	Chip select "H" pulse width	0		ns	-
	T_{CS}	Chip select setup time (Write)	15		ns	
	T_{RCS}	Chip select setup time (Read ID)	45		ns	
	T_{RCSFM}	Chip select setup time (Read FM)	355		ns	
	T_{CSF}	Chip select wait time (Write/Read)	10		ns	
	T_{CSH}	Chip select hold time	10		ns	
WRX	T_{WC}	Write cycle	66		ns	
	T_{WRH}	Control pulse "H" duration	15		ns	

	T_{WRL}	Control pulse “L” duration	15		ns	
RDX (ID)	T_{RC}	Read cycle (ID)	160		ns	When read ID data
	T_{RDH}	Control pulse “H” duration (ID)	90		ns	
	T_{RDL}	Control pulse “L” duration (ID)	45		ns	
RDX (FM)	T_{RCFM}	Read cycle (FM)	450		ns	When read from frame memory
	T_{RDHFM}	Control pulse “H” duration (FM)	90		ns	
	T_{RDLFM}	Control pulse “L” duration (FM)	355		ns	
D[17:0]	T_{DST}	Data setup time	10		ns	For CL=30pF
	T_{DHT}	Data hold time	10		ns	
	T_{RAT}	Read access time (ID)	-	40	ns	
	T_{RATFM}	Read access time (FM)	-	340	ns	
	T_{ODH}	Output disable time	20	80	ns	

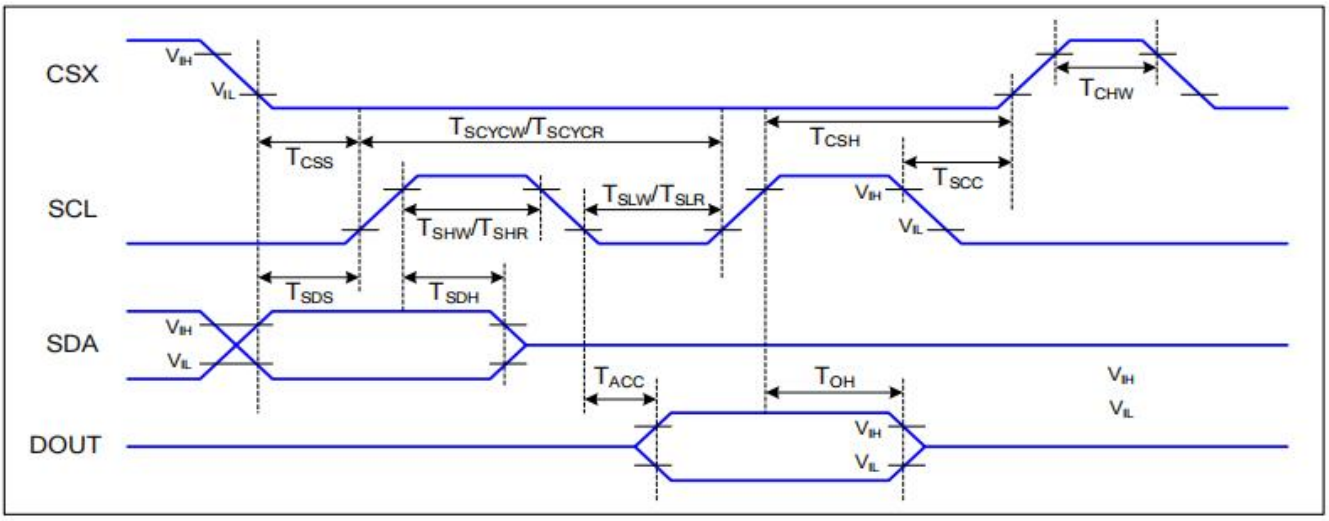
8080 Parallel Interface Characteristics



Rising and Falling Timing for I/O Signal

Note: The rising time and falling time (Tr, Tf) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 20% and 80% of VDDI for Input signals.

7.4.2 3-SPI Serial Data Transfer Interface Characteristics:



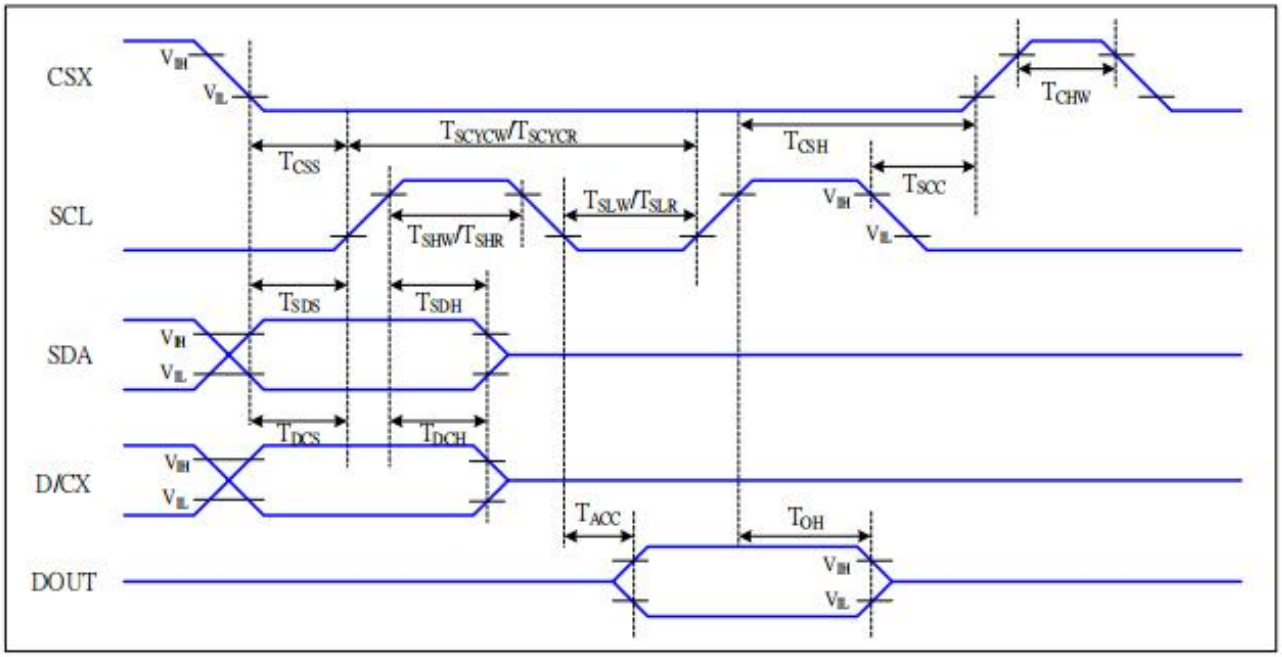
3-SPI Interface Timing Characteristics

VDDI=1.8V,VDDA=2.8V, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select “H” pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	
	T_{SHW}	SCL “H” pulse width (Write)	15		ns	
	T_{SLW}	SCL “L” pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL “H” pulse width (Read)	60		ns	
	T_{SLR}	SCL “L” pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

3-SPI Interface Characteristics

7.4.3 4-SPI Serial Data Transfer Interface Characteristics:

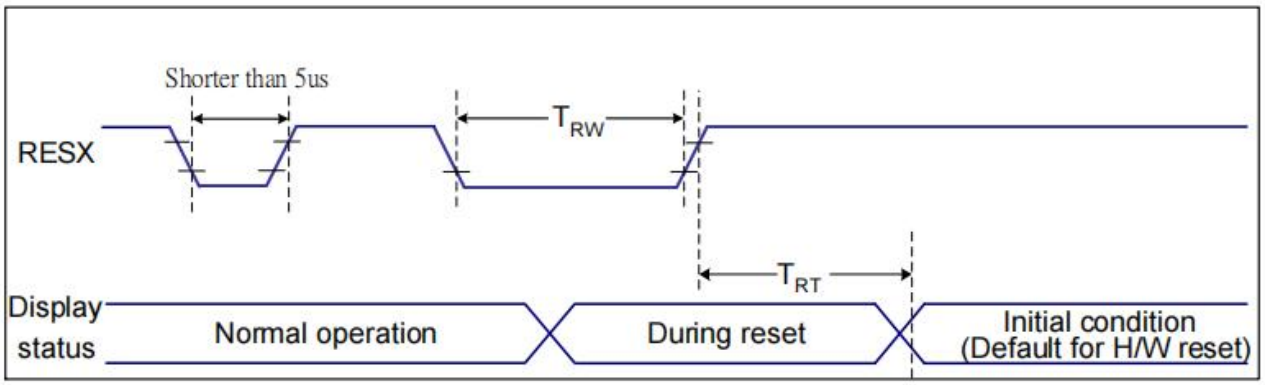


4-SPI Interface Timing Characteristics

VDDI=1.8V,VDDA=2.8V, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select “H” pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	-write command & data ram
	T_{SHW}	SCL “H” pulse width (Write)	15		ns	
	T_{SLW}	SCL “L” pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	-read command & data ram
	T_{SHR}	SCL “H” pulse width (Read)	60		ns	
	T_{SLR}	SCL “L” pulse width (Read)	60		ns	
D/CX	T_{DCS}	D/CX setup time	10		ns	
	T_{DCH}	D/CX hold time	10		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF For minimum CL=8pF
	T_{OH}	Output disable time	15	50	ns	

7.4.6 Reset Timing



Reset Timing

VDDI=1.8V,VDDA=2.8V, AGND=DGND=0V, Ta=25℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120 (Note 1, 6, 7)	ms

Table 1 Reset Timing

Notes:

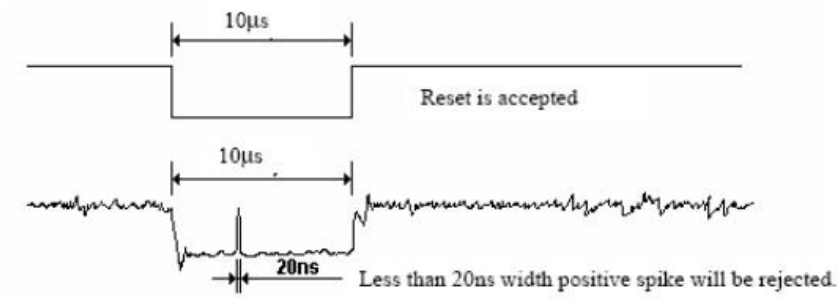
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

8. Electro-Optical Characteristics

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time		Tr +Tf	θx = θy =0	---	25	35	ms	Note 1
Contrast Ratio		CR		800	1000	---	---	Note 2
Transmittance		T%		3.45	4.05	---	%	
Color Chromaticity (CIE1931)	White	W x	θx = θy =0	---	0.304	---	---	
		W y		---	0.332	---	---	
Viewing angle	θ_T		CR > 10	80	85	---	Deg.	Note 3
	θ_B			80	85	---		
	θ_L			80	85	---		
	θ_R			80	85	---		

1.Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o' clock direction and the vertical or 6, 12 o' clock direction with respect to the optical axis which is normal to the LCD surface (see FIGURE 1).

2.Contrast measurements shall be made at viewing angle of Θ= 0 and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state . (see FIGUR 1) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3.Transmittance is the Value without APF and without CG.

4.The color chromaticity coordinates specified in the above table shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

5.The electro-optical response time measurements shall be made as FIGURE 2. The times needed for the luminance to change from 10% to 90% is Tr, and 90% to 10% is Tf.

Figure1 Measurement Set Up

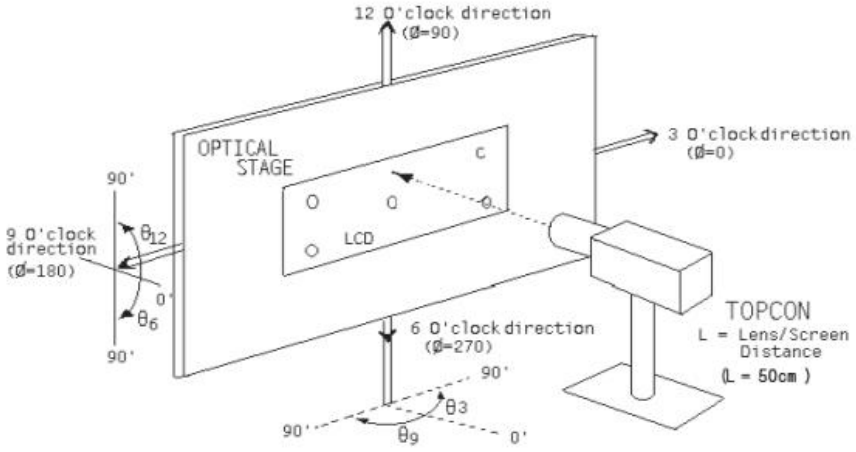
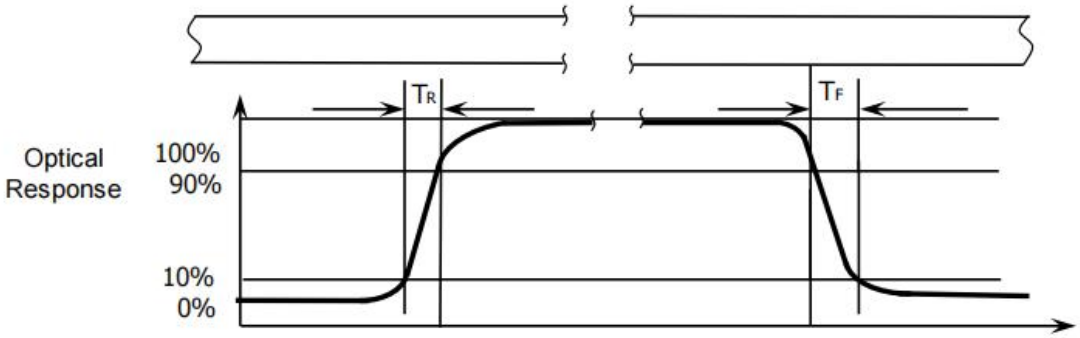
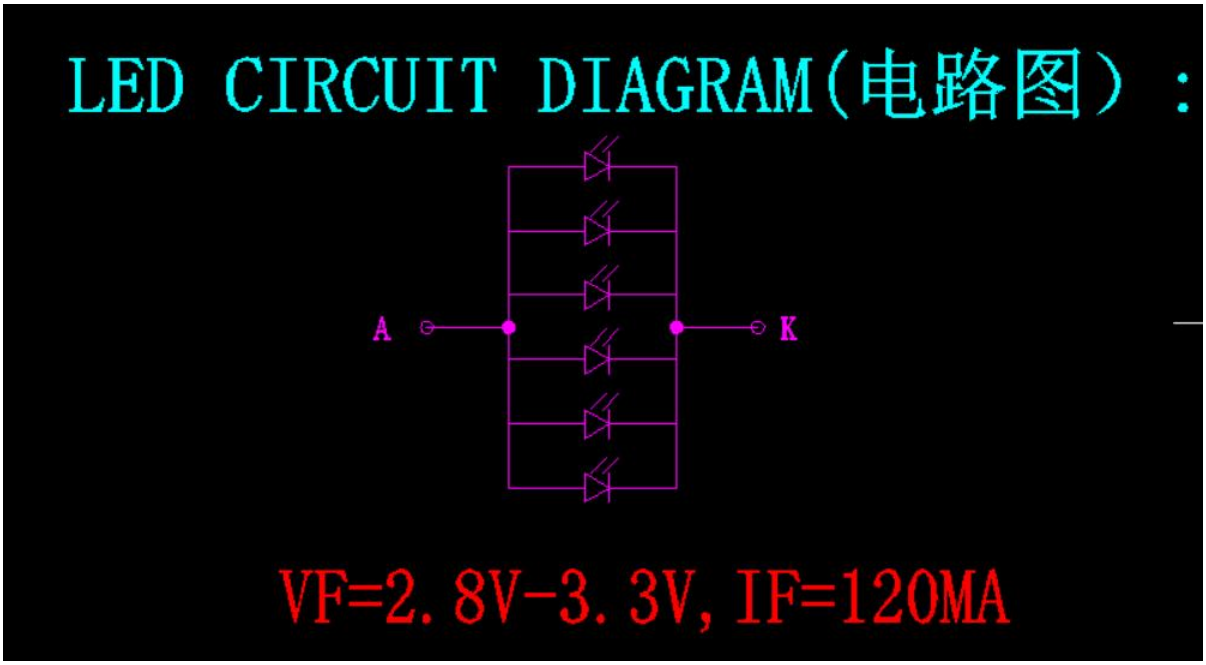


Figure2 Response Time Testing



Note(4) Backlight circuit



9.Records Of Version

Version	Revise Date	Page	Content
00	2024-12-30	ALL	New released