

PRODUCT SPECIFICATION **FOR LCD MODULE**

Revision: 1.0

Model No: LS035I10-MP-V1

Module Type: COG+FPC+B/L

APPROVED SIGNATURE

- ☒ Approved Product Specification only
- ☐ Approved Product Specification and Samples

<u>Prepared By</u>	<u>Checked By</u>	<u>Approved By</u>

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1. General Description

LS035I10-MP-V1 is a transmissive type a-Si TFT-LCD (amorphous silicon thin film transistor liquid crystal display) module, which is composed of a TFT-LCD panel, a driver circuit and a backlight unit. The panel size is 3.45 inch and the resolution is 640(RGB)*480, the panel can display up to 16.7 M colors.

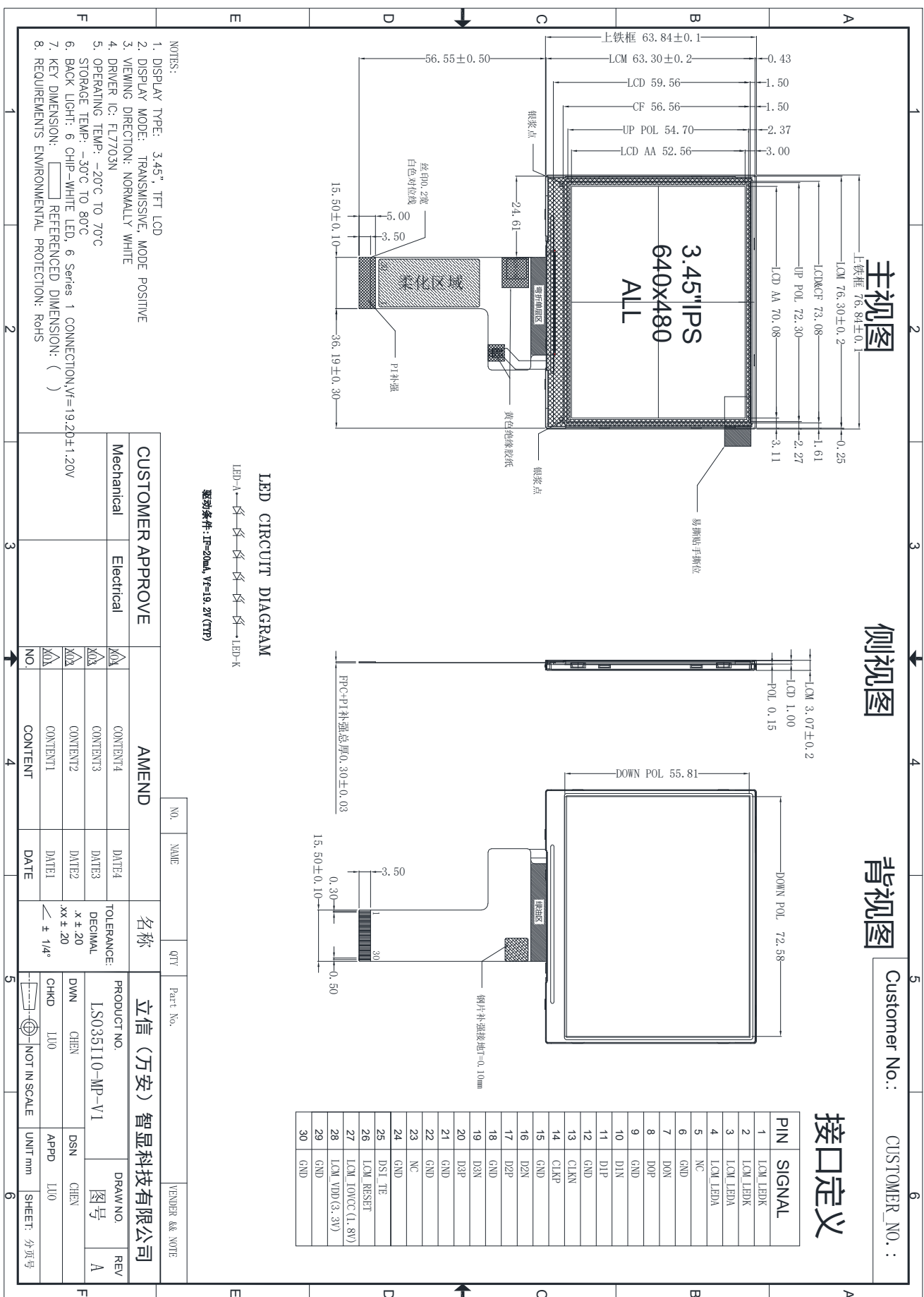
2. Physical Features

Display Mode	TFT-LCD Module
	Active matrix TFT, Transmissive type
Display Format	Graphic 640(RGB)×480 Dot-matrix
Input Data	MIPI
Viewing Direction (Grayscale Inversion)	Free (IPS)
Drive	FL7703NI

3. Mechanical Specification

Item	Specification	Unit
LCM+LENS Module size (H×V×D)	76.84 ×63.84×3.07	mm
Number of dots	640(RGB) ×480	pixel
Active area (H×V)	70.08×52.56	mm

4. Outline Dimensio



5. Absolute Maximum Ratings

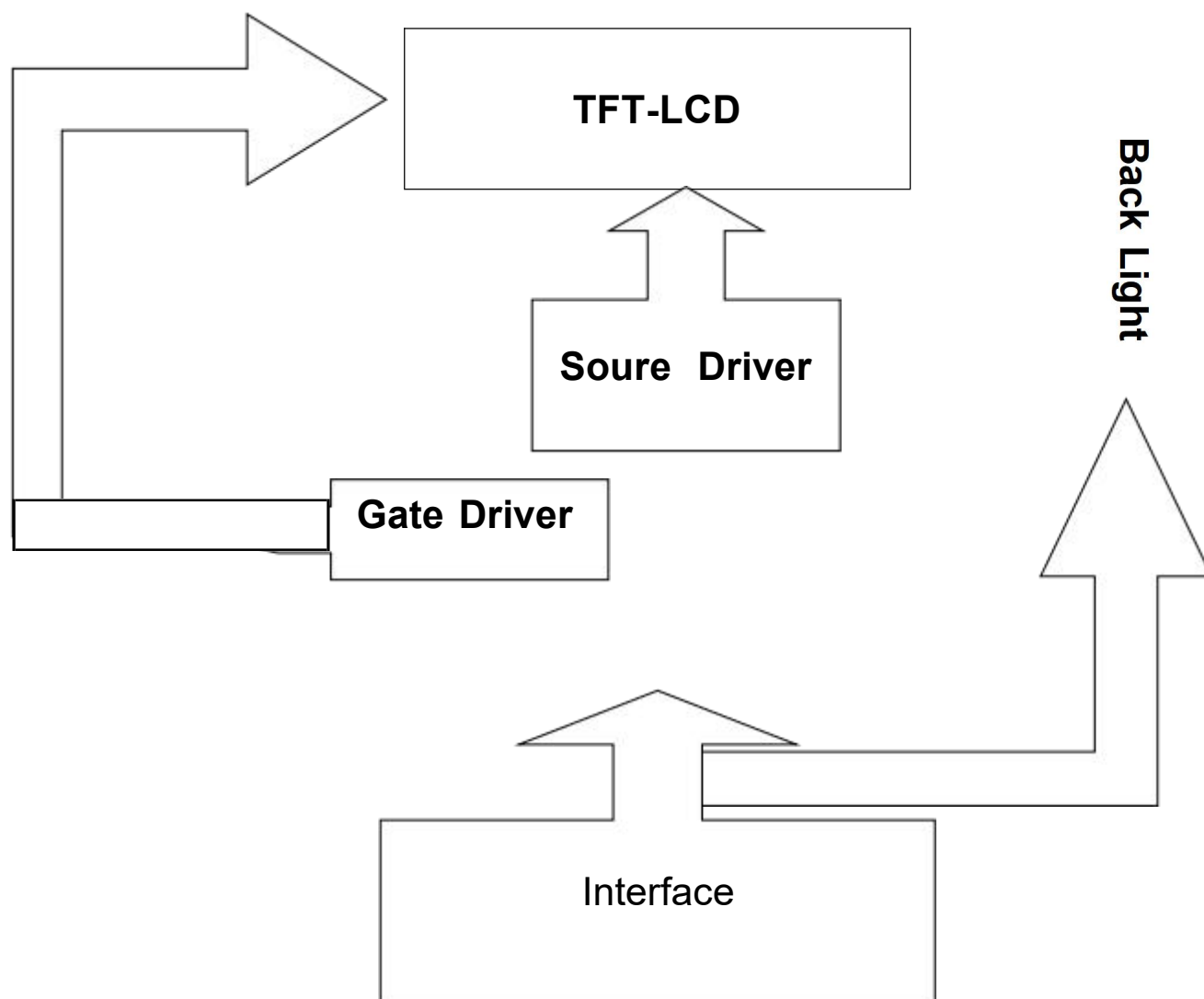
Item	Symbol	Min	Max	Unit	Remark
Supply voltage	VDD	-0.3	6.6	V	
Supply voltage	IOVCC	-0.3	5.5	V	
Operating temperature	TOPR	-20	70	°C	
Storage temperature	TSTR	-30	80	°C	

6. Electrical Characteristics

Item		Symbol	Rating			Unit	Remark
			Min	Typ	Max		
Supply voltage		VDD	2.5	2.8	3.3	V	Note1
Supply voltage		IOVCC	1.65	1.8	3.3	V	
Input Voltage	L level	VIL	0	---	0.3*IOVCC	V	
	H level	VIH	0.7*IOVCC	---	IOVCC	V	

7. Module Function Description

7-1. Block Diagram Of LCM



7-2. Pin Description

PIN NO.	Symbol	I/O	Description
1	LEDK	P	Power for LED backlight cathode
2	LEDK	P	Power for LED backlight cathode
3	LEDA	P	Power for LED backlight anode
4	LEDA	P	Power for LED backlight anode
5	NC		
6	GND	P	ground
7	D0N	I/O	High speed interface data differential signal input/output pins
8	D0P	I/O	High speed interface data differential signal input/output pins
9	GND	P	ground
10	D1N	I	High speed interface data differential signal input pins.
11	D1P	I	High speed interface data differential signal input pins.
12	GND	P	ground
13	CLKN	I	High speed interface clock differential signal input pins.
14	CLKP	I	High speed interface clock differential signal input pins.
15	GND	P	ground
16	D2N	I	High speed interface data differential signal input pins.
17	D2P	I	High speed interface data differential signal input pins.
18	GND	P	ground
19	D3N	I	High speed interface data differential signal input pins.
20	D3P	I	High speed interface data differential signal input pins.
21	GND	P	ground
22	GND	P	ground
23	NC		
24	GND	P	ground
25	TE	O	Serves TE (Tearing Effect) output pin /NC

26	RESET	I	Reset pin
27	IOVCC	P	Power supply
28	VDD	P	Power supply
29	GND	P	ground
30	GND	P	ground

7-3 Timing Characteristics

High Speed Mode

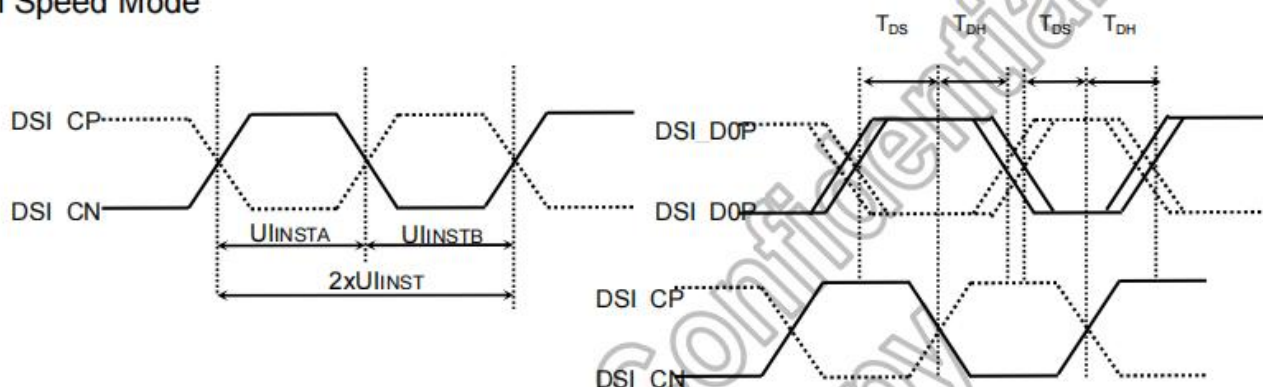


Figure 7-4: DSI clock timing Characteristics

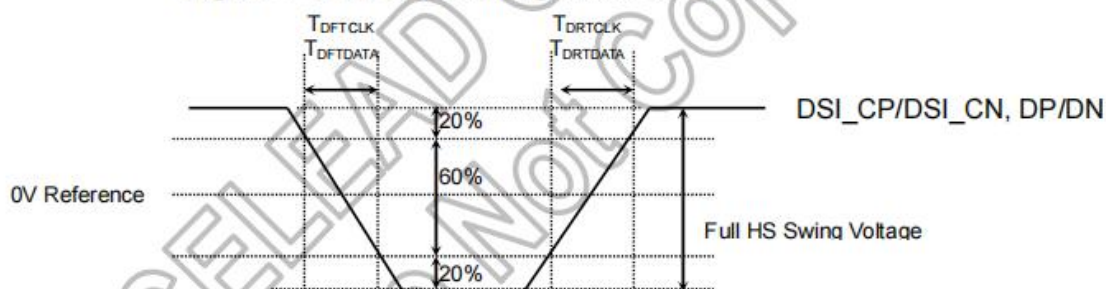


Figure 7-5: Rising and falling time on clock and data channel

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, $T_A = -30$ to 70°C)

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Double UI instantaneous	$2xUI_{INST}$	4LANE: 3.30 3LANE: 2.85 @ VDDD=1.8V	-	25	ns
	UI instantaneous	UI_{INSTA} UI_{INSTB}	4LANE: 1.67 3LANE: 1.43 @ VDDD=1.8V	-	12.5	ns
DP/DN	Data to clock setup time	T_{DS}	$0.15xUI$	-	-	ps
	Data to clock hold time	T_{DH}	$0.15xUI$	-	-	ps
DSI_CP/ DSI_CN	Differential rise time for clock	T_{DRTCLK}	150	-	$0.3UI$	ps
	Differential fall time for clock	T_{DFTCLK}	150	-	$0.3UI$	ps
DP/DN	Differential rise time for data	$T_{DRTDATA}$	150	-	$0.3UI$	ps
	Differential fall time for data	$T_{DFTDATA}$	150	-	$0.3UI$	ps

Table 7-3: DSI High Speed Mode Characteristics

Low Power Mode

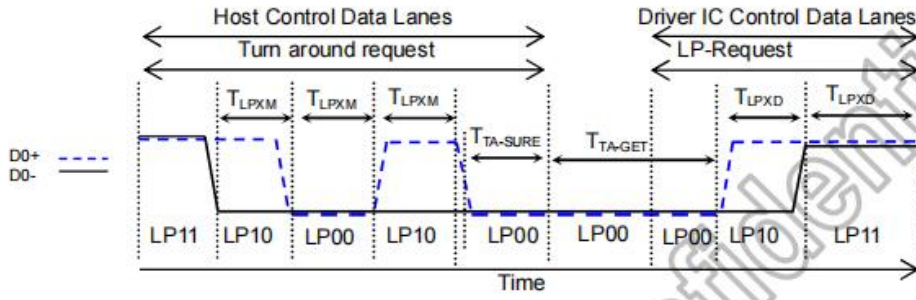


Figure 7-6: BTA from HOST to Display Module Timing

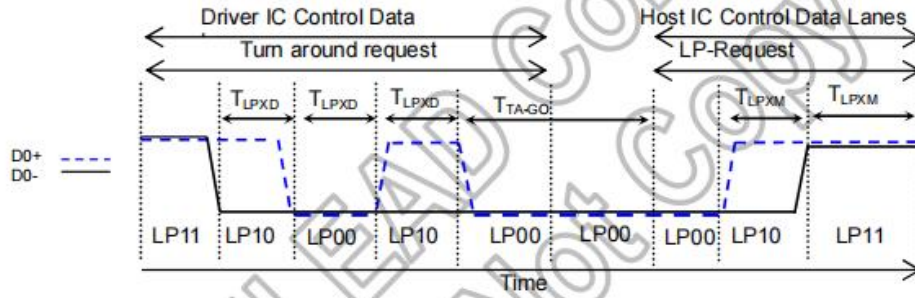


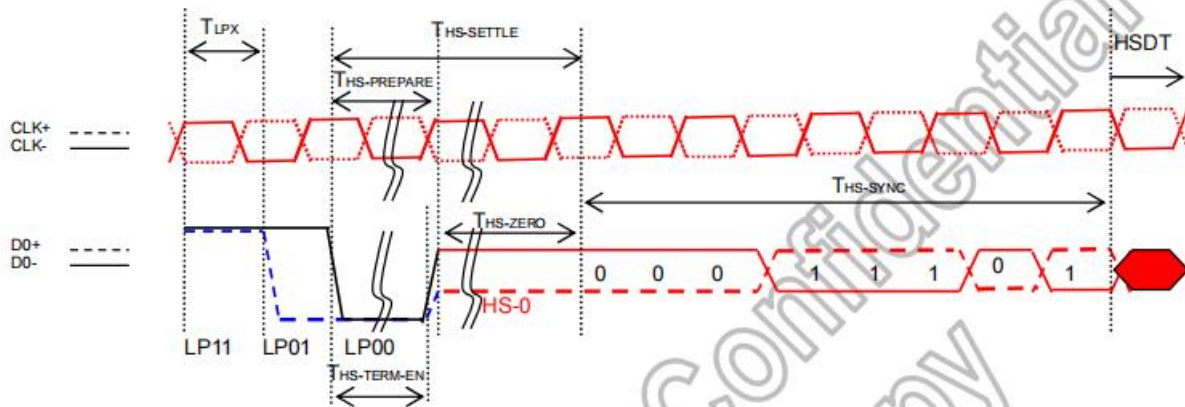
Figure 7-7: BTA from Display Module Timing to HOST

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V, $T_A = -30$ to 70°C)

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11 Host → Display module	T_{LPXM}	50	-	-	ns
	Length of LP-00/LP01/LP10/LP11 Display module → Host	T_{LPXD}	50	-	-	ns
	Time-out before the MPU start driver	$T_{TA-SURE}$	T_{LPXD}	-	$2 \times T_{LPXD}$	ns
	Time to drive LP-00 by display module	T_{TA-GET}	$5 \times T_{LPXD}$	-	-	ns
	Time to drive LP-00 after turnaround request Host	T_{TAGO}	$4 \times T_{LPXD}$	-	-	ns

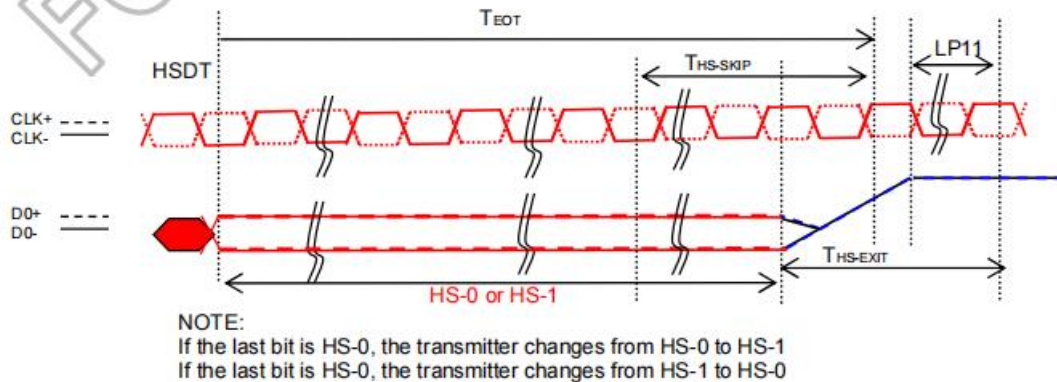
Table 7-4: DSI Low Power Mode Characteristics

DSI BURSTS



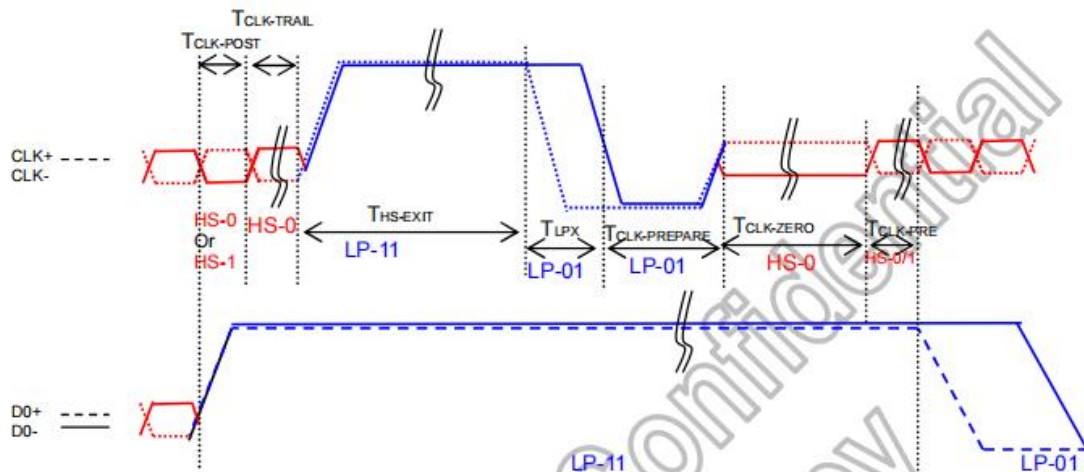
Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11	T _{LPX}	50	-	-	ns
	Time to Driver LP-00 to prepare for HS transmission	T _{HS-PREPARE}	40+4UI	-	85+6UI	ns
	Time to enable data receiver line termination	T _{HS-TERM-EN}	-	-	35+4xUI	ns
	Time to drive LP-00 by display module	T _{TA-GET}	5xT _{LPXD}	-	-	ns
	Time to drive LP-00 after turnaround request Host	T _{TAGO}	4xT _{LPXD}	-	-	ns

Table 7-5: DSI Low Power Mode to High Speed Mode Timing



Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Time-Out at Display Module to Ignore Transition Period of EoT	T _{HS-SKIP}	40	-	55+4xUI	ns
	Time to Driver LP-11 after HS Burst	T _{HS-EXIT}	100	-	-	ns

Table 7-6: DSI Low Power Mode to High Speed Mode Timing



Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Time that the MCU shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	T _{CLK-POST}	60+52xUI	-	-	ns
	Time to drive HS differential state after last payload clock bit of a HS transmission burst	T _{CLK-TRAIL}	60	-	-	ns
	Time to drive LP-11 after HS burst	T _{HS-EXIT}	100	-	-	ns
	Time to drive LP-00 to prepare for HS transmission	T _{CLK-PREPARE}	38	-	95	ns
	Time-out at Clock Lane Display Module to enable HS Termination	T _{CLK-TERM-EN}	-	-	38	ns
	Minimum lead HS-0 drive period before starting Clock	T _{CLK-PREPARE} + T _{CLK-ZERO}	300	-	-	ns
	Time that the HS clock shall be driven prior to any associated data Lane beginning the transition from LP to HS mode	T _{CLK-PRE}	8xUI			

Table 7-7: Clock Lanes High Speed Mode to/from Low Power Mode Timing

7.3.3 Reset input timing

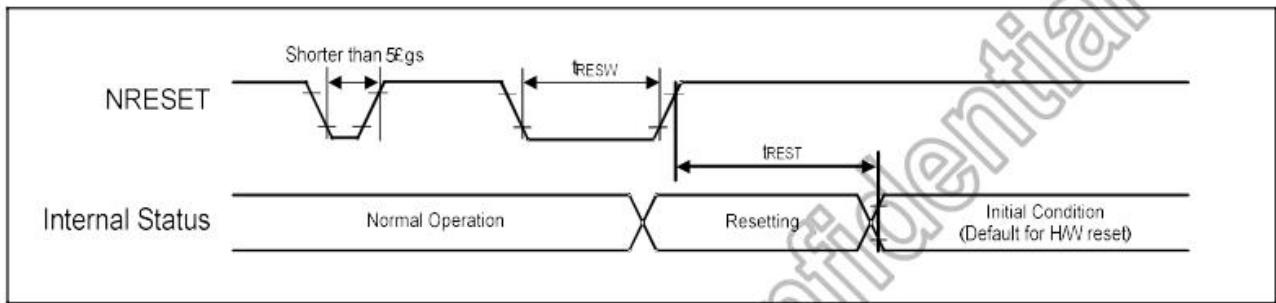


Figure 7-8: Reset input timing

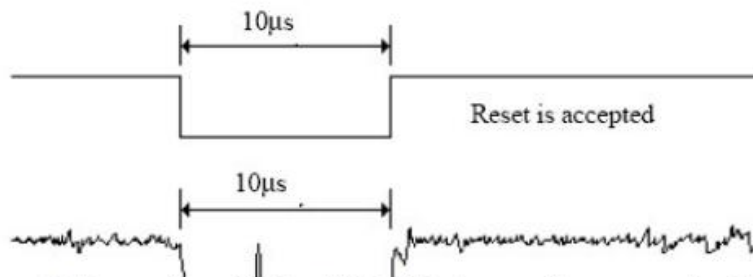
Symbol	Parameter	Related Pins	Spec.			Note	Unit
			Min.	Typ.	Max.		
tRESW	Reset low pulse width ⁽¹⁾	NRESET	10	-	-	-	μs
tREST	Reset complete time ⁽²⁾	-	15	-	-	When reset applied during SLPIN mode	ms
		-	120	-	-	When reset applied during SLPOUT mode	ms

Table 7-8: Reset Input Timing

Note: (1) Spike due to an electrostatic discharge on NRESET line does not cause irregular system reset according to the following table.

NRESET Pulse	Action
Shorter than 5 μs	Reset Rejected
Longer than 10 μs	Reset
Between 5 μs and 10 μs	Reset Start

- (2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which Maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.
- (3) During Reset Complete Time, ID and VCOM value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 15ms after a rising edge of NRESET.
- (4) Spike Rejection also applies during a valid reset pulse as shown as below:



- (5) It is necessary to wait 15msec after releasing NRESET before sending commands. Also Sleep Out command cannot be sent for 120msec.

8. Electro-Optical Characteristics

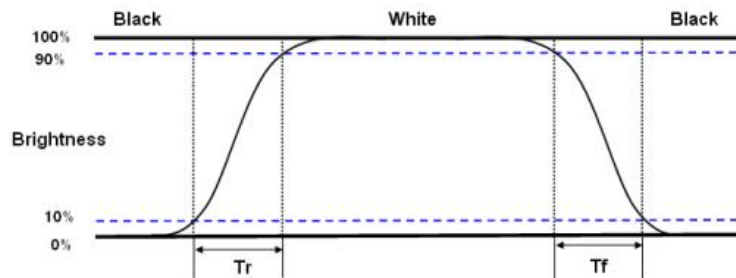
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time	Tr +Tf	$\theta_x = \theta_y = 0$	---	25	50	ms	Note 1
Contrast Ratio	CR		600	800	---	---	Note 2
Transmittance	T%		3.7	4.4	---	%	
Color Chromaticity (CIE1931)	White	W x	$\theta_x = \theta_y = 0$	0.297	---	---	
		W y		0.317	---	---	
Viewing angle	θ_T	CR > 10	75	85	---	Deg.	Note 3
	θ_B		75	85	---		
	θ_L		75	85	---		
	θ_R		75	85	---		
LCM Luminance ($I_F = 40mA$)	L		---	300	---	cd/m2	Note4

Note 1: Measuring Conditions:

The optical characteristics are determined after the unit has been 'ON' and stable at the maximum brightness, in a dark environment at an ambient temperature at $25^{\circ}\text{C} \pm 2^{\circ}\text{C}$.

Note 2: Definition of response time:

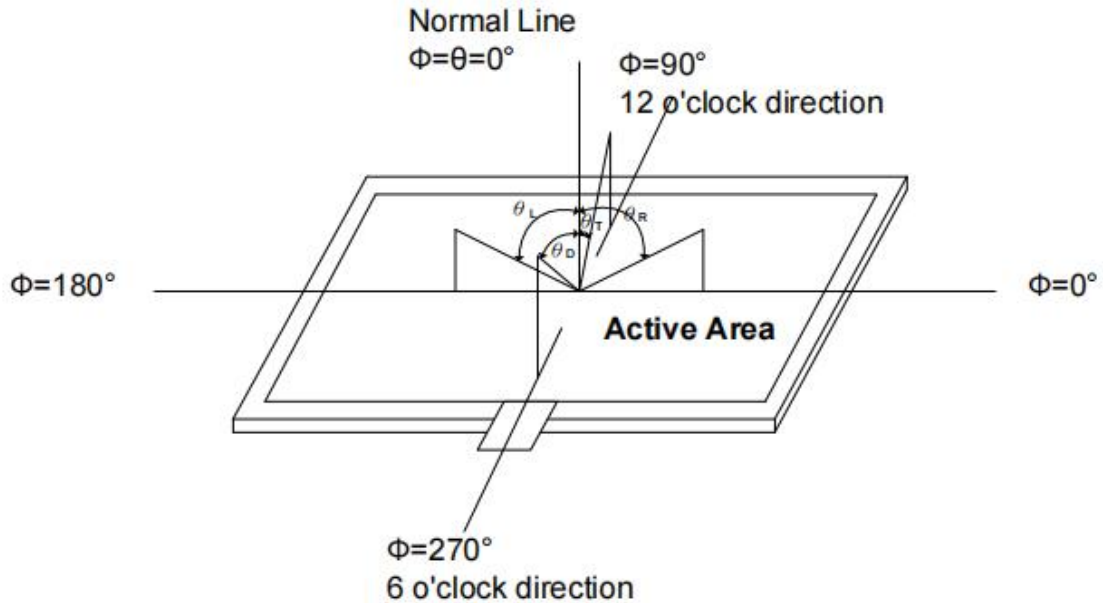
The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time is the time between photo detector output intensity changed from 10% to 90%. And fall time is the time between photo detector output intensity changed from 90% to 10%.



Note 3: Definition of contrast ratio:

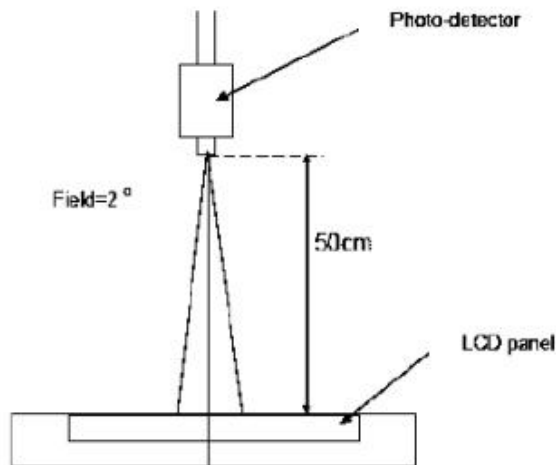
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 4: Definition of viewing angle



Note 5: Optical characteristic measurement setup.

The LCD module should be stabilized at given temperature for 10 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 10 minutes in a windless room.



Note 6: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

Note(4) Backlight circuit

LED CIRCUIT DIAGRAM



驱动条件: $I_F=20\text{mA}$, $V_f=19.2\text{V (TYP)}$

9.Records Of Version

Version	Revise Date	Page	Content
00	2025-12-9	ALL	New released