PRODUCT SPECIFICATION FOR LCD MODULE

Revision: 1.0

Model No: LSC0397I07-R-V1

Module Type: COG+FPC+B/L+CTP

APPROVED SIGNATURE

■ Approved Product Specification only

□ Approved Product Specification and Samples

Prepared By	Checked By	Approved By

Contents

目录

1. General Description

LSC0397I07-R-V1 is a transmissive type a-Si TFT-LCD (amorphous silicon thin film transistor liquid crystal display) module, which is composed of a TFT-LCD panel, a driver circuit and a backlight unit. The panel size is 3.97 inch and the resolution is 480(RGB)*800, the panel can display up to 16.7M colors.

2. Physical Features

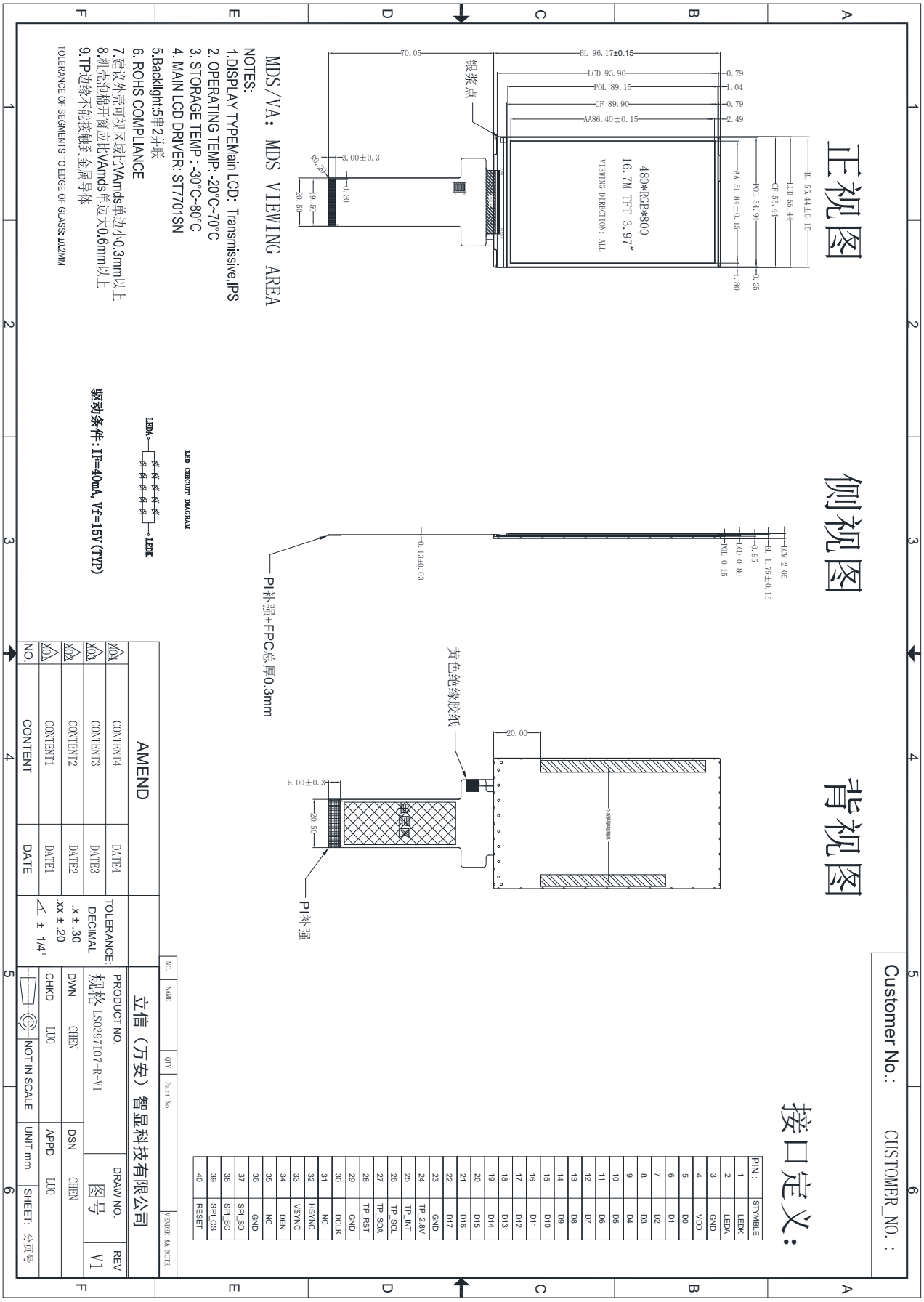
Display Mode	TFT-LCD Module
	Active matrix TFT, Transmissive type
Display Format	Graphic 480(RGB)×800 Dot-matrix
Input Data	18BIT RGB
Viewing Direction （Grayscale Inversion）	Free（IPS）
Drive	ST7701SN

3. Mechanical Specification

Item	Specification	Unit
Module size (H×V×D)	59.4 ×108.32 ×3.675	mm
Number of dots	480(RGB) ×800	pixel
Active area (H×V)	51.84×86.4	mm

4.Outline Dimension

LCM



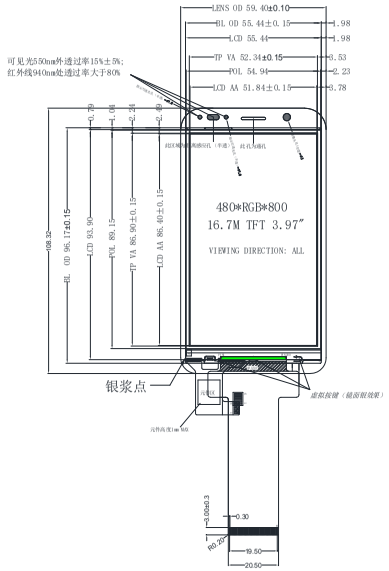
PIN:	SYMBLE
1	LEDK
2	LEDA
3	GND
4	VDD
5	D0
6	D1
7	D2
8	D3
9	D4
10	D5
11	D6
12	D7
13	D8
14	D9
15	D10
16	D11
17	D12
18	D13
19	D14
20	D15
21	D16
22	D17
23	GND
24	TP_2.8V
25	TP_INT
26	TP_SCL
27	TP_SDA
28	TP_RST
29	GND
30	DCLK
31	NC
32	HSYNC
33	VSYNC
34	DEN
35	NC
36	GND
37	SPI_SDI
38	SPI_SCI
39	SPI_CS
40	RESET

Customer No.:	CUSTOMER_NO.：

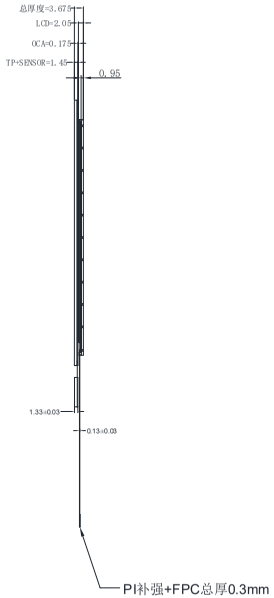
有害物质管理标准

- ■ 欧盟RoHS环保指令
- □ 欧盟RoHS环保指令+无卤素要求
- □ _____有害物质管理标准 第___版

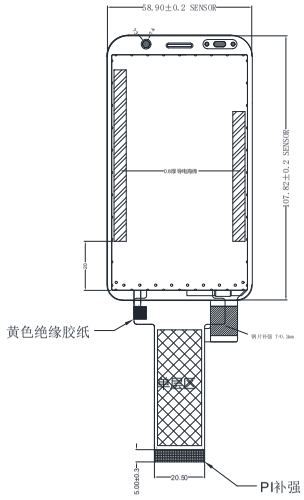
正视图



侧视图



背视图



接口定义：

PIN：	STYMBLE
1	LEDK
2	LEDA
3	GND
4	VDD
5	D0
6	D1
7	D2
8	D3
9	D4
10	D5
11	D6
12	D7
13	D8
14	D9
15	D10
16	D11
17	D12
18	D13
19	D14
20	D15
21	D16
22	D17
23	GND
24	TP_2.8V
25	TP_INT
26	TP_SCL
27	TP_SDA
28	TP_RST
29	GND
30	DCLK
31	NC
32	HSYNC
33	VSYNC
34	DEN
35	NC
36	GND
37	SPI_SDI
38	SPI_SCI
39	SPI_CS
40	RESET

PIN	SIGNAL
1	CTP_VCC(2.8V)
2	CTP_SCL(1.8V)
3	CTP_SDA(1.8V)
4	CTP_INT(1.8V)
5	CTP_RST(1.8V)
6	GND

NOTE

1. LCD显示模式： IPS。
   可视角：ALL；
   2. 驱动 IC ：ST7701SN
3. 工作温度：-20° C - 70° C
   储存温度：-30° C - 80° C
4. 背光LED灯:5串2并联
   模组亮度：400 cd/m2(typ.)， 450 cd/m2(min.)，
5. 未注公差:±0.15

BOMWIDTH BOMHEIGHT BOMSTARTPOS1 BOMSECONDLINE

BOMTHIRDLINE PDMUPDATE BOMSTARTPOS2 BOMSTARTPOS3

1	结构	G+F+F
2	IC	CHSC5448 多点
3	透光率	
4	表明硬度	
5	材质及厚度	T=1.1+0.35mm
6	工作温度	-20℃~+60℃;20-90RH
7	储存湿温度	-30℃~+70℃;20-90RH
8	翘曲度	≤0.3%
9	盖板厚度	0.20mm
10	跌落要求	
11	屏分辨率	480*800
12	所有的材料符合ROHS	

NO.	NAME	QTY	Part No.	VENDER && NOTE

AMEND			TOLERANCE: DECIMAL .x ± .30 .xx ± .20 ∠ ± 1/4°	立信（万安）智显科技有限公司			
X04	CONTENT4	DATE4		PRODUCT NO. 规格 LSC0397I07-R-V1		DRAW NO. 图号	REV V1
X03	CONTENT3	DATE3		DWN CHEN	DSN CHEN		
X02	CONTENT2	DATE2		CHKD LUO	APPD LUO		
X01	CONTENT1	DATE1		NOT IN SCALE	UNIT mm	SHEET: 分页号	
NO.	CONTENT	DATE					

LCM+CTP

LESSON 立信（万安）智显科技有限公司 Lesson Smart Dispaly Technology Co.,Ltd

5. Absolute Maximum Ratings

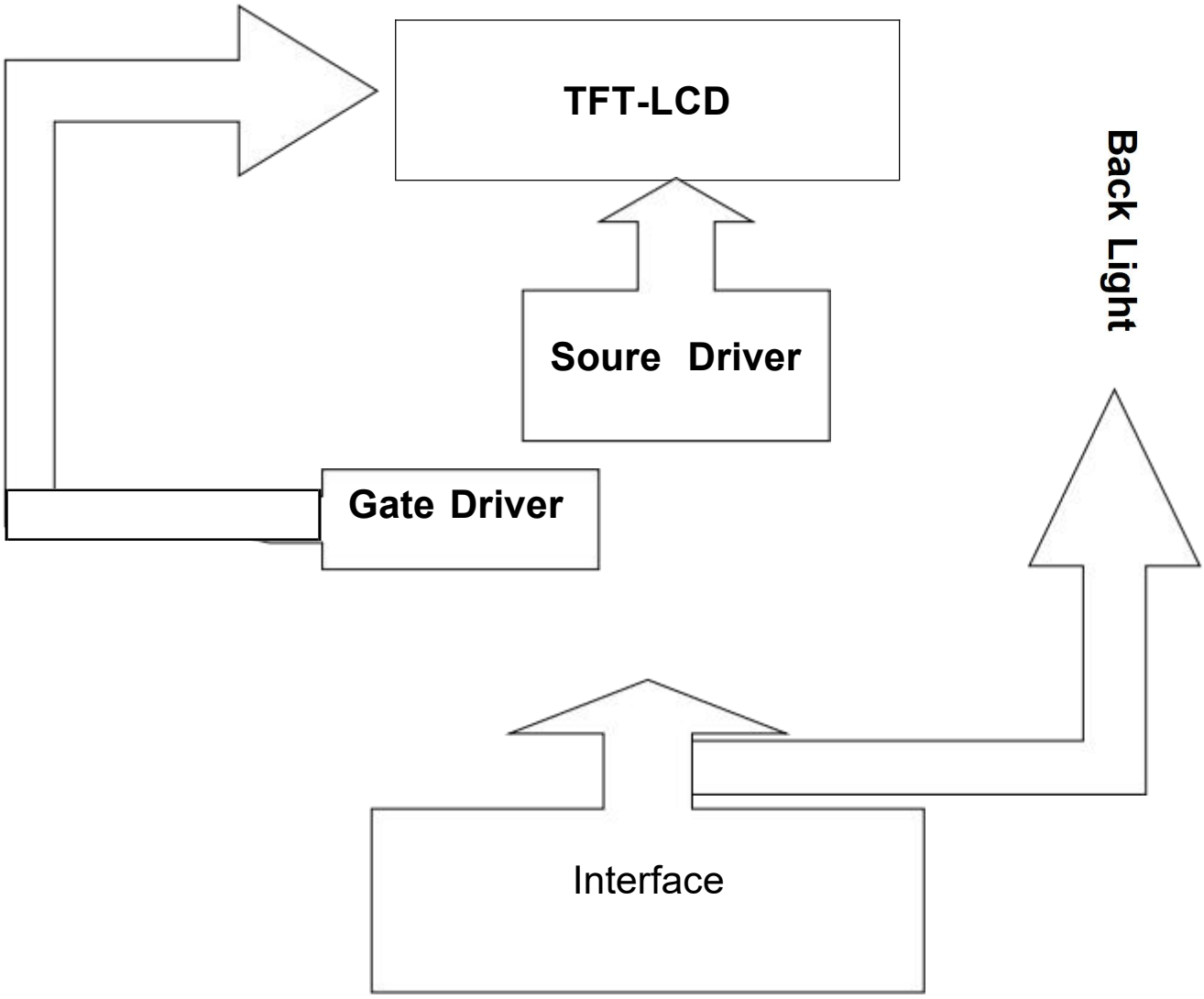
Item	Symbol	Min	Max	Unit	Remark
Supply voltage	VCC	-0.3	3.6	V	Note1 Note2
Supply voltage	IOVCC	-0.3	3.6	V	
Operating temperature	TOPR	-20	70	℃	
Storage temperature	TSTR	-30	80	℃	

6. Electrical Characteristics

Item		Symbol	Rating			Unit	Remark
			Min	Typ	Max		
Supply voltage		VCC	2.5	2.8	3.6	V	Note1
Supply voltage		IOVCC	1.65	1.8	3.3	V	
Input Voltage	L level	VIL	VSS	---	0.3*IOVCC	V	
	H level	VIH	0.7*IOVCC	---	IOVCC	V	
LCD Drive Power current		ILCD		TBD		mA	

7. Module Function Description

7-1. Block Diagram Of LCM



7-2. Pin Description

PIN NO.	Symbol	I/O	Description
1	LEDK		Power for LED backlight cathode
2	LEDA		Power for LED backlight anode
3	GND		Ground
4	VDD		Power Supply
5-22	D0-D17		parallel data bus for RGB Interface
23	GND		Ground
24	TP_2.8V		Power Supply
25	TP_INT		Interrupt signal
26	TP_SCL		Serial clock pin
27	TP_SDA		Serial data input/output bidirection pin
28	TP_RST		Reset signal pin
29	GND		Ground
30	DCLK		Dot clock signal for RGB interface operation
31	NC		
32	HS		Line synchronizing signal for RGB interface operation
33	VS		Frame synchronizing signal for RGB interface operation
34	DE		Data enable signal for RGB interface operation Low: access enabled High: access inhibited
35	NC		
36	GND		Ground
37	SPI_SDA		SDA: Serial data input/output bidirectional pin for SPI Interface.
38	SPI_SCL		SCL: Serial clock input for SPI interface.
39	SPI_CS		chip select signal Low: the chip is selected and accessible High: the chip is not selected and not accessible
40	RESET		The external reset input - Initializes the chip with a low input. Be sure to execute a power-on reset after supplying power.

7-3 Timing Characteristics

7.5.1 Serial Interface Characteristics (3-line serial):

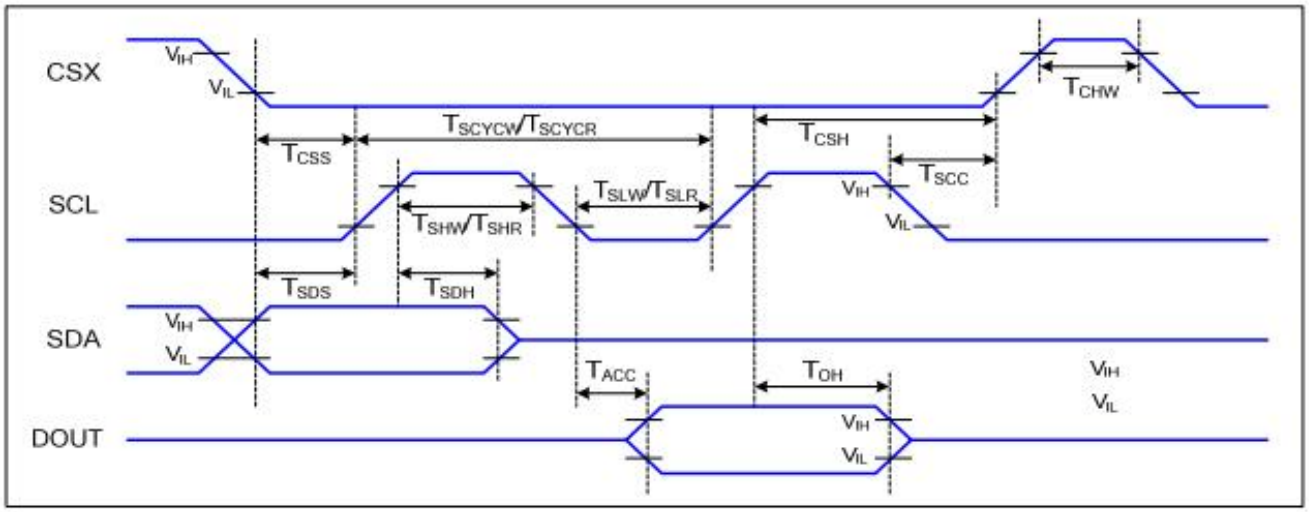


Figure 1 3-line serial Interface Timing Characteristics

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	60		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	
	T_{SLW}	SCL "L" pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	

Table 4 3-line serial Interface Characteristics

Note : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

7.5.3 RGB Interface Characteristics :

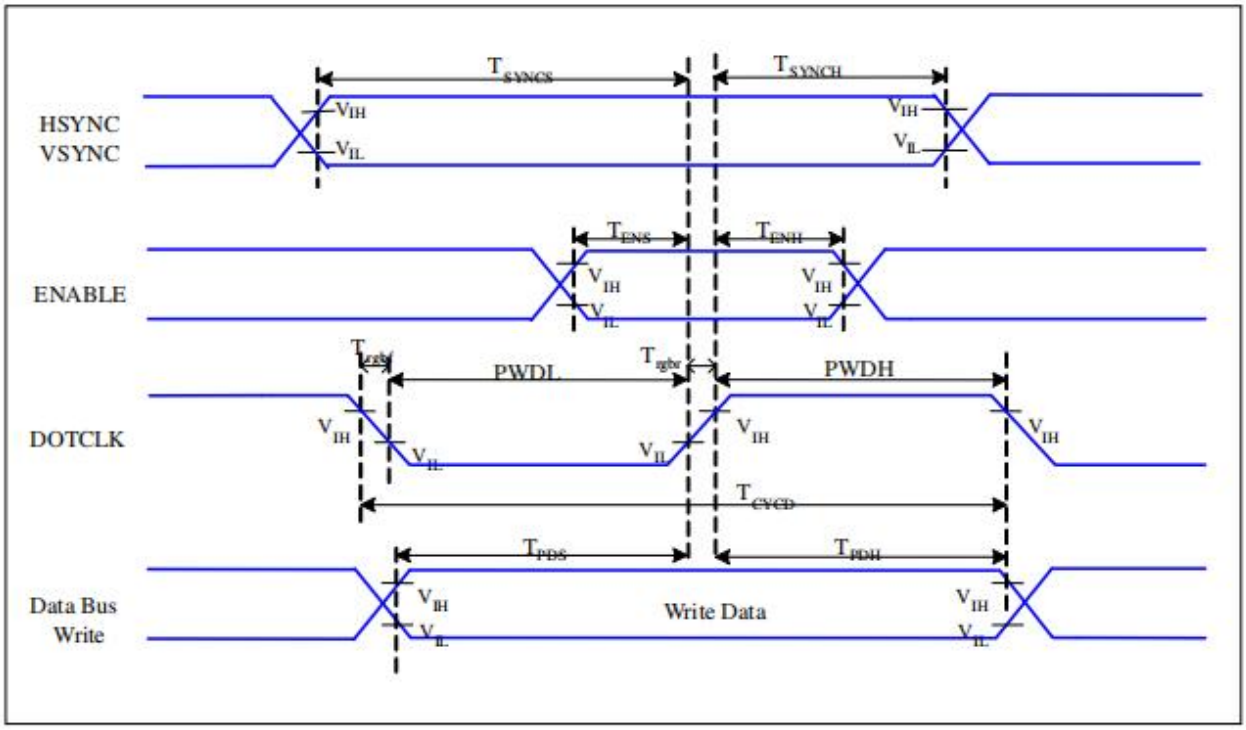


Figure 3 RGB Interface Timing Characteristics

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	5	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	5	-	ns	
	T_{ENH}	Enable Hold Time	5	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	15	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	15	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	33	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	15	ns	
DB	T_{PDS}	PD Data Setup Time	5	-	ns	
	T_{PDH}	PD Data Hold Time	5	-	ns	

Table 6 18/16 Bits RGB Interface Timing Characteristics

7.5.5 Reset Timing:

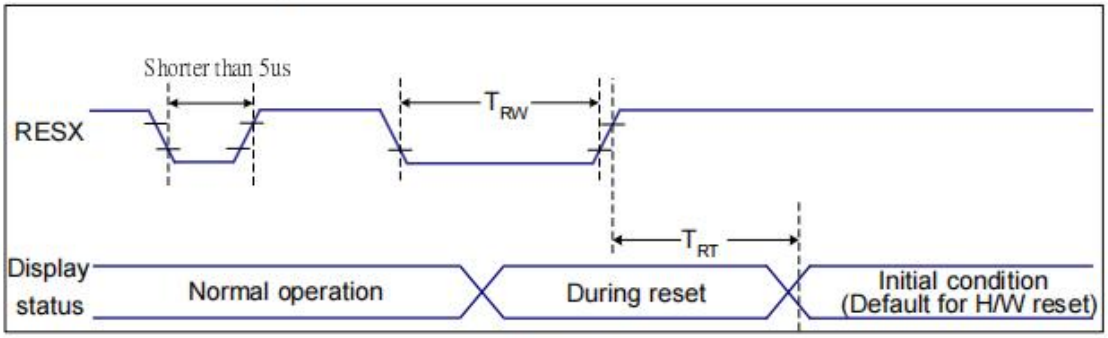


Figure 9 Reset Timing

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120(Note 1, 6, 7)	ms

Table 9 Reset Timing

Notes:

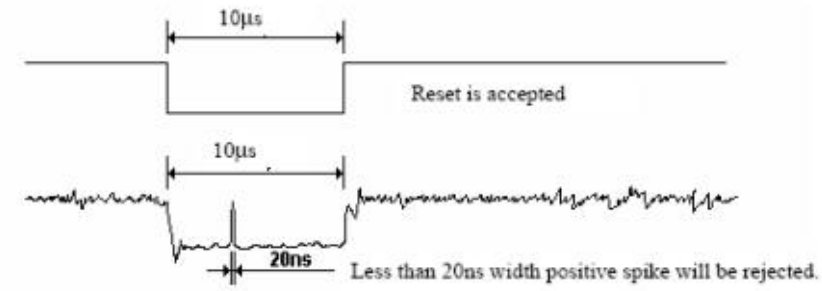
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

8. Electro-Optical Characteristics

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time		Tr +Tf	θx = θy =0	---	35	---	ms	Note 1
Contrast Ratio		CR		550	800	---	---	Note 2
Transmittance		T%		3.34	3.93	---	%	
Color Chromaticity (CIE1931)	White	W x	θx = θy =0	---	0.292	---	---	
		W y		---	0.333	---	---	
Viewing angle	θ_T		CR > 10	---	85	---	Deg.	Note 3
	θ_B			---	85	---		
	θ_L			---	85	---		
	θ_R			---	85	---		
Luminance (I_F = 40mA)		L		400	450	---	cd/m2	Note4

Note:

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see FIGURE 1).

2. Contrast measurements shall be made at viewing angle of Θ= 0 and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state . (see FIGURE 1) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Transmittance is the Value with Polarizer

4. The color chromaticity coordinates specified in Table 5 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

5. The electro-optical response time measurements shall be made as FIGURE 3 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Tr, and 90% to 10% is Td.

Figure 1. The Definition of Vth & Vsat

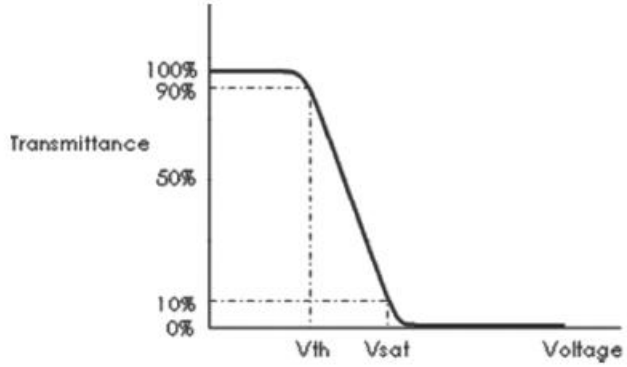


Figure 2. Measurement Set Up

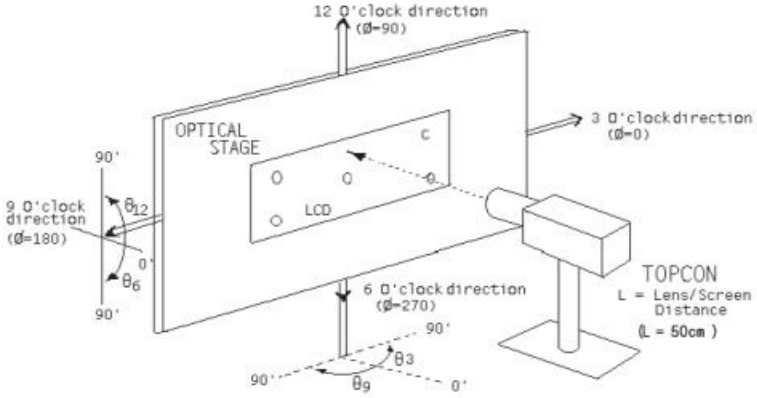
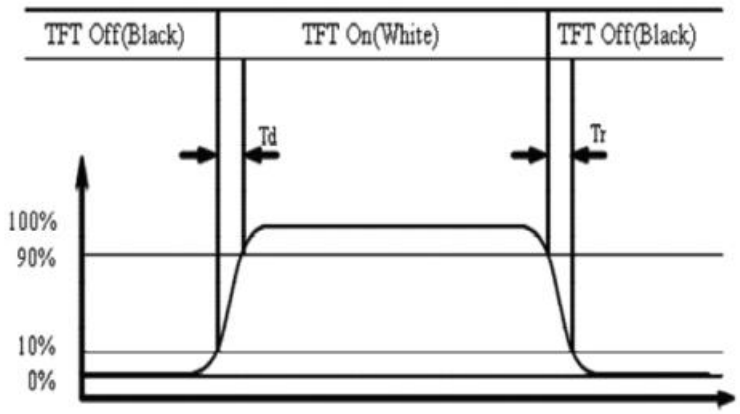
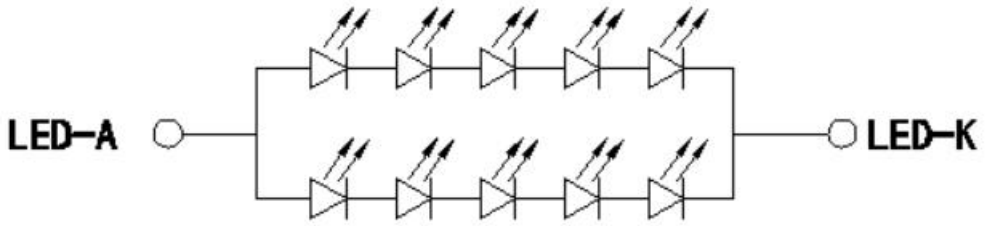


Figure 3. Response Time Testing



Note(4) Backlight circuit



If=40mA Vf=14V∽16V

9. Inspection Standards

1. AQL(Acceptable Quality Level)

AQL of major and minor defect

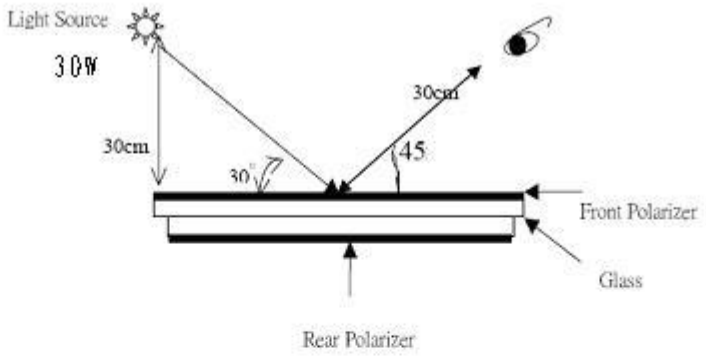
According to GB/T 2828-2003 ; , normal inspection, Class Ⅱ

MAJOR DEFECT	MINORDEFECT
0.65	1.5

2. Basic conditions for inspection

The LCM face to us, in normal environment, About an angle of incidence 30, a distance of 30cm with normal eye,with an angle of 45 degree to check the products without uncovering the film!

(As shown below)

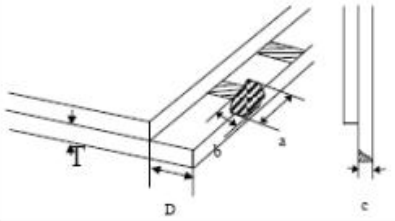
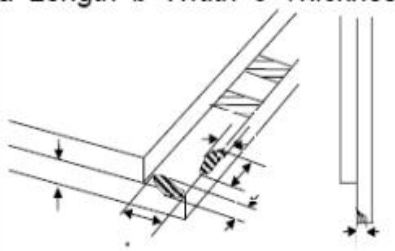


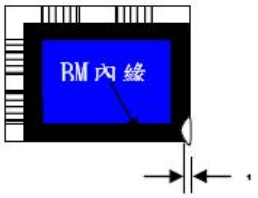
3. Inspection item and criteria

3.1 Visual inspection criterion in immobility

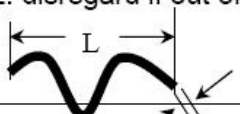
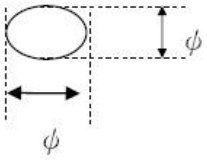
3.1.1 Glass defect

No	Defect item	Criteria	Remark
1	Dimension Unconformity (Major defect)	By Engineering Drawing	

No	Defect item	Criteria	Remark
2	Cracks (Major defect)	1.Linear cracks on panel 【Reject】 2. Nonlinear crack contrast by limited sample	
3	Glass extrude the conductive area (minor defect)	a: disregards and no influence assemblage 1) b≦1/3Pin width(non bonding area) 【Accept】 2) bonding area≦0.5mm 【Accept】	a:Length, b:Width
4	Pin-side、conductive area damaged (minor defect)	(a c：disregards) b≦ 1/3 of effective length for bonding electrode 【Accept】	a:Length、b:Width、c:Thickness 
5	Pin-side、non-conductive area damaged (minor defect)	1) Damage area don't touch the ITO (Inclueling contraposition mark,except scribing mark) 【Accept】 2) c<T b≦BM 1/3 of width 【Accept】 3) c=T b not touch the seal glue 【Accept】 4) a disregards	a:Length、b:Width、c:Thickness 

No	Defect item	Criteria	Remark
6	Non-pin-side damage (minor defect)	c<T 1) b exceeds 1/3 BM 【Reject】 c=T b not touch the seal glue 【Reject】	c : Thickness b: width of damage 

3.1.2 LCD appearance defect (View area)

No	Defect item	Criteria		Remark
1	Fiber、glass cratch、polarizer scratch/folded (minor defect)	Specification	Allowable	note1: L：Length，W：Width note2: disregard if out of AA 
		0.05mm<W≦0.1mm; L≦3.0mm	1	
		W>0.1mm ; L>3.0mm	0	
2	Polarizer bubble、concave and convex (minor defect)	ψ≦0.2mm	disregard	note 1:ψ=(L+W)/2；L：Length，W：Width note2: disregard if out of AA
		0.2mm<ψ ≦ 0.3mm	2	
		0.3mm<ψ ≦ 0.5mm	1	
		0.5mm<ψ	0	
3	Black dots、dirty dots、impurities、eyewinker (Major defect)	ψ≦0.15mm	disregard	note2: disregard if out of AA 
		0.15mm<ψ ≦ 0.25mm	2	
		0.25mm<ψ ≦ 0.3mm	1	
		0.3mm<ψ	0	
4	Polarizer prick (Major defect)	ψ≦0.1mm	disregard	note1:ψ=(L+W)/2 ；L= Length，W=Width note2: the distance between two dots ＞5mm
		0.1mm<ψ≦0.25mm	3	
		ψ＞0.25mm	0	

3.1.3 .FPC

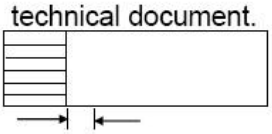
No	Defect item	Criteria		Remark
1	Copper screen peel (Major defect)	Copper screen peel 【Reject】		
2	No release tape or peel (Major defect)	No release tape or peel 【Reject】		
3	Dirty dot and impurity of FPC for customer using side (minor defect)	Specification	Allowable	note1: Cannot have stride ITO impurities
		ψ≦0.25mm	2	
		ψ>0.25	0	

3.1.4 Black tape & Mara tape

1	FPC or H/S black tape shift (minor defect)	1.shift spec: 1)glue to the polarize 【Reject】 2) IC bare 【Reject】 2. left-and-right spec: 1) exceed of FPC edge or H-S edge 【Reject】 2)IC bare 【Reject】	
2	No black tape (Major defect)	No black tape 【Reject】	
3	Tape position mistake (minor defect)	Not by engineering drawing 【Reject】	
4	Mara tape defect (minor defect)	Peel before pulling the protecting film. 【Reject】	

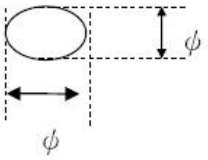
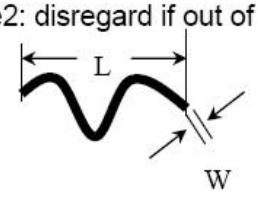
3.1.5 Silicon and Tuffy glue

No	Defect item	Criteria	Remark
1	Quantity of silicon (minor defect)	Uncover the ITO and circuit area. 【Reject】	note: compared by engineering drawing.

No	Defect item	Criteria	Remark
2	Tuffy glue (minor defect)	1. Uncover the reveal copper area 【Reject】 2. Cover layer 0.3mm(Min) ~ 3.0mm(Max) 【accept】	note:if customer has special requirement , refer to the technical document. 
3	Depth of glue covering (minor defect)	Depth of glue covering overtop front Polarizer 【Reject】	Except of the special requirement。

3.2 Electrical criteria

No	Defect item	Criteria	Remark
1	No display (Major defect)	No display 【Reject】	
2	Missing line (Major defect)	Missing line 【Reject】	
3	Seg-com light and dark (Major defect)	Seg-com light and dark 【Reject】	ND filter 2% test
4	No display in immobility (Major defect)	No display in immobility 【Reject】	
5	Flicker of Pattern (Major defect)	Flicker of Pattern 【Reject】	
6	Mura (Major defect)	ND filter 2% test	
7	Over current (Major defect)	Over current 【Reject】	
8	Voltage out of specification (Major defect)	Voltage out of specification 【Reject】	
9	Pattern blur ,error code (Major defect)	Pattern blur ,error code 【Reject】	
10	Dark light, Flicker (Major defect)	Dark light, Flicker 【Reject】	

No	Defect item	Criteria	Remark	
11	Black/White dots、Dirty dots、eyewinker (Major defect)	Specification	Allowable	Note1: disregard if out of AA 
		ψ≦0.15mm	disregard	
		0.15mm<ψ ≦ 0.25mm	2	
		0.25mm<ψ ≦ 0.3mm	1	
		0.3mm<ψ	0	
12	Fiber、glass cratch、polarizer scratch/folded (minor defect)	W≦0.03mm	disregard	note1: L : Length、W : Width note2: disregard if out of AA 
		0.03mm<W≦0.05mm ; L≦3.0mm	2	
		0.05mm<W≦0.1mm; L≦3.0mm	1	
		W>0.1mm ; L>3.0mm	0	

10.Records Of Version

Version	Revise Date	Page	Content
00	2025-4-27	all	New released