PRODUCT SPECIFICATION FOR LCD MODULE

Revision: 1.0

Model No: LS014I02-MP-V1

Module Type: COG+FPC+B/L

APPROVED SIGNATURE

■ Approved Product Specification only

□ Approved Product Specification and Samples

Prepared By	Checked By	Approved By

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1. General Description

LS014I02-MP-V1 is a transmissive type a-Si TFT-LCD (amorphous silicon thin film transistor liquid crystal display) module, which is composed of a TFT-LCD panel, a driver circuit and a backlight unit. The panel size is 1.4 inch and the resolution is 320(RGB)*320, the panel can display up to 16.7M colors.

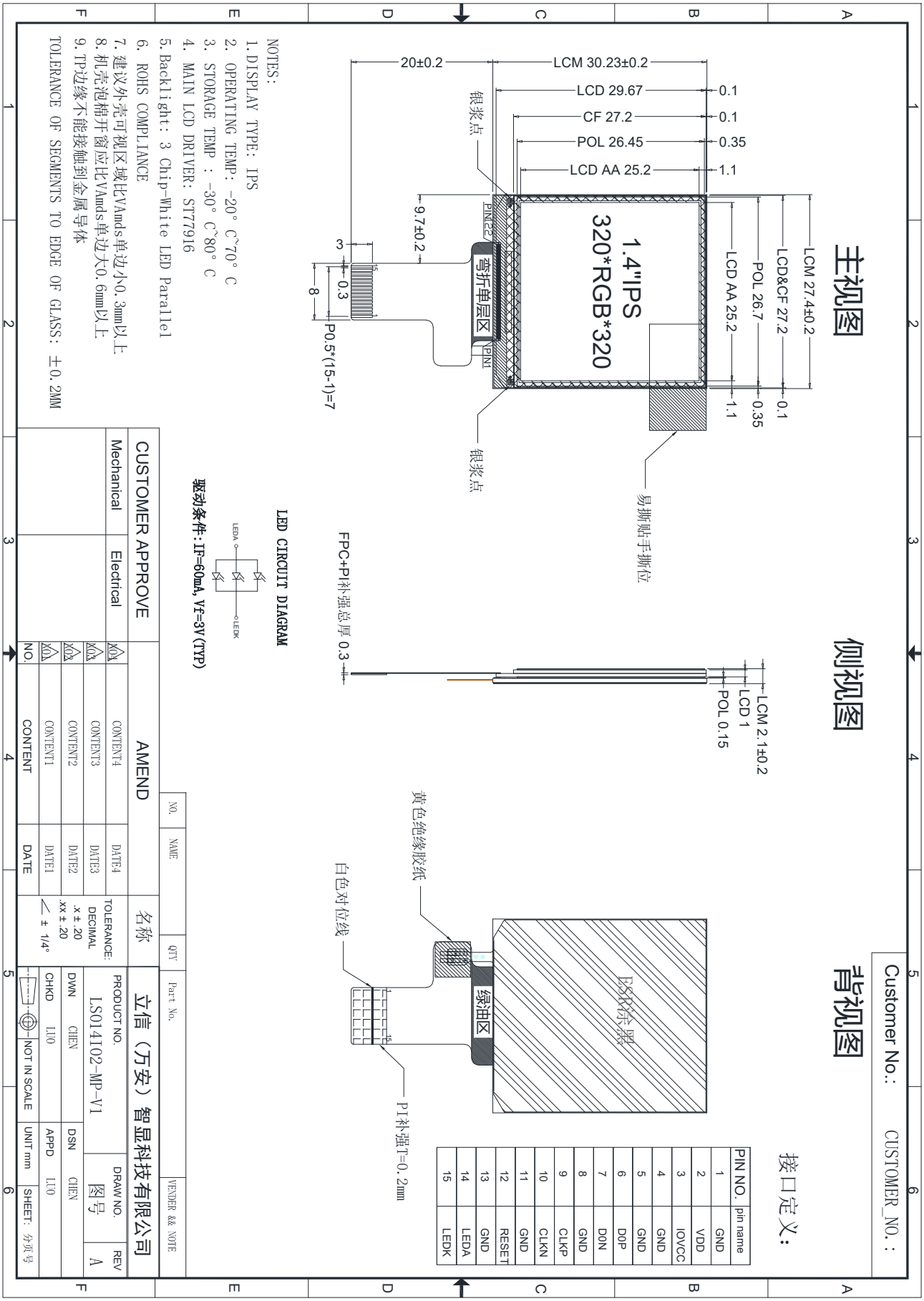
2. Physical Features

Display Mode	TFT-LCD Module
	Active matrix TFT, Transmissive type
Display Format	Graphic 320(RGB)×320 Dot-matrix
Input Data	MIPI
Viewing Direction （Grayscale Inversion）	Free（IPS）
Drive	ST77916

3. Mechanical Specification

Item	Specification	Unit
Module size (H×V×D)	27.4 ×30.23 ×2.1	mm
Number of dots	320(RGB) ×320	pixel
Active area (H×V)	25.2×25.2	mm

4. Outline Dimension



5. Absolute Maximum Ratings

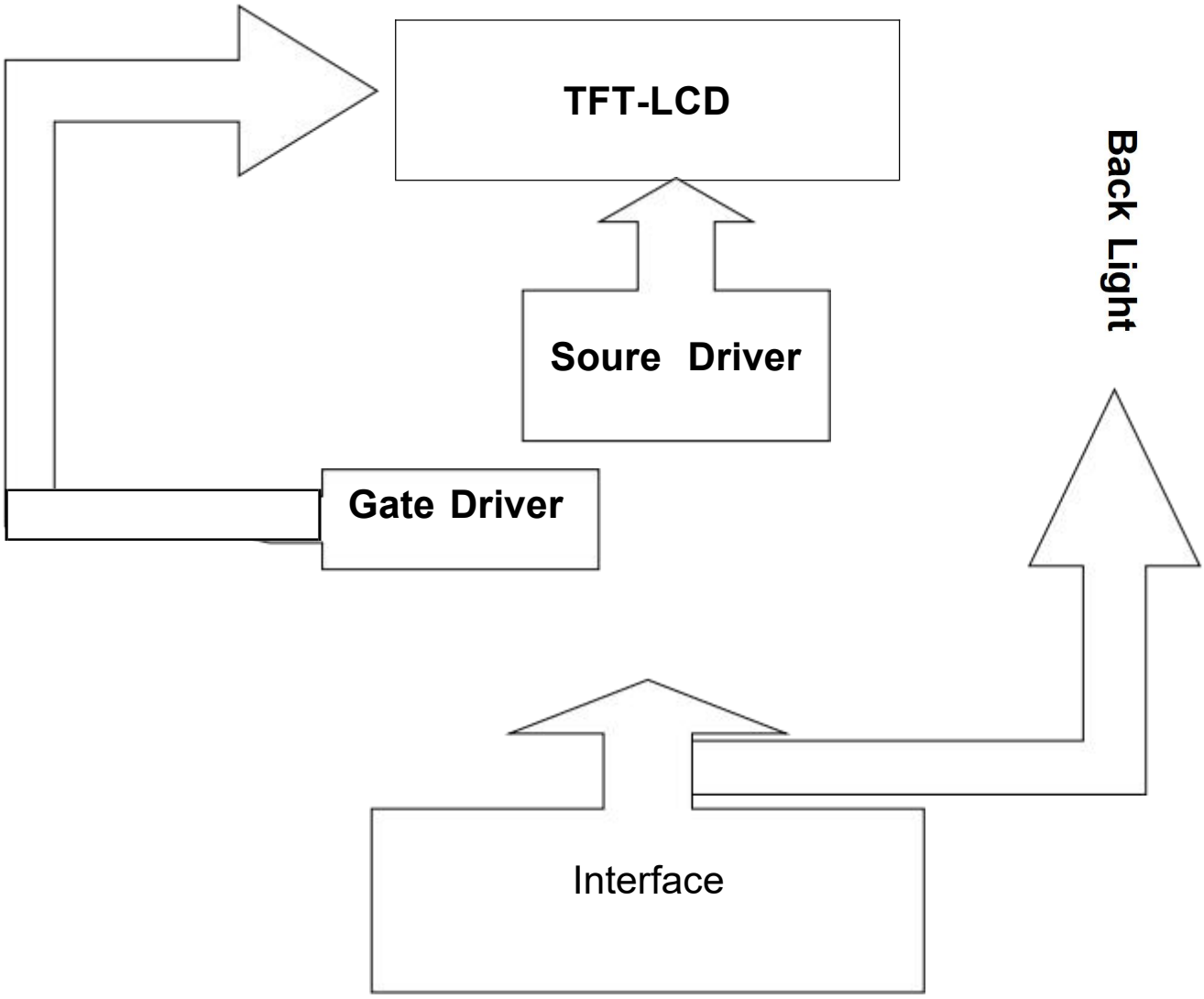
Item	Symbol	Min	Max	Unit	Remark
Supply voltage	VCC	-0.3	4.6	V	Note1 Note2
Supply voltage	IOVCC	-0.3	4.0	V	
Operating temperature	TOPR	-20	70	℃	
Storage temperature	TSTR	-30	80	℃	

6. Electrical Characteristics

Item		Symbol	Rating			Unit	Remark
			Min	Typ	Max		
Supply voltage		VCC	2.65	2.8	3.3	V	Note1
Supply voltage		IOVCC	1.65	1.8	3.3	V	
Input Voltage	L level	VIL	0	---	0.3*IOVCC	V	
	H level	VIH	0.7*IOVCC	---	IOVCC	V	

7. Module Function Description

7-1. Block Diagram Of LCM



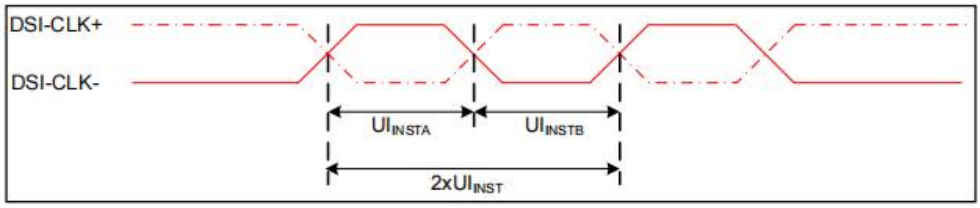
7-2. Pin Description

PIN NO.	Symbol	I/O	Description
1	GND	P	Ground
2	VDD	P	Power Supply
3	IOVCC	P	Power Supply
4	GND	P	Ground
5	GND	P	Ground
6	D0P	I	MIPI-DSI data lane positive-end input pin
7	D0N	I	MIPI-DSI data lane negative-end input pin
8	GND	P	Ground
9	CLKP	I	MIPI-DSI clock lane positive-end input pin
10	CLKN	I	MIPI-DSI clock lane negative-end input pin
11	GND	P	Ground
12	RESET	I	Reset pin.
13	GND	P	Ground
14	LEDA	P	Power for LED backlight anode
15	LEDK	P	Power for LED backlight cathode

7-3 Timing Characteristics

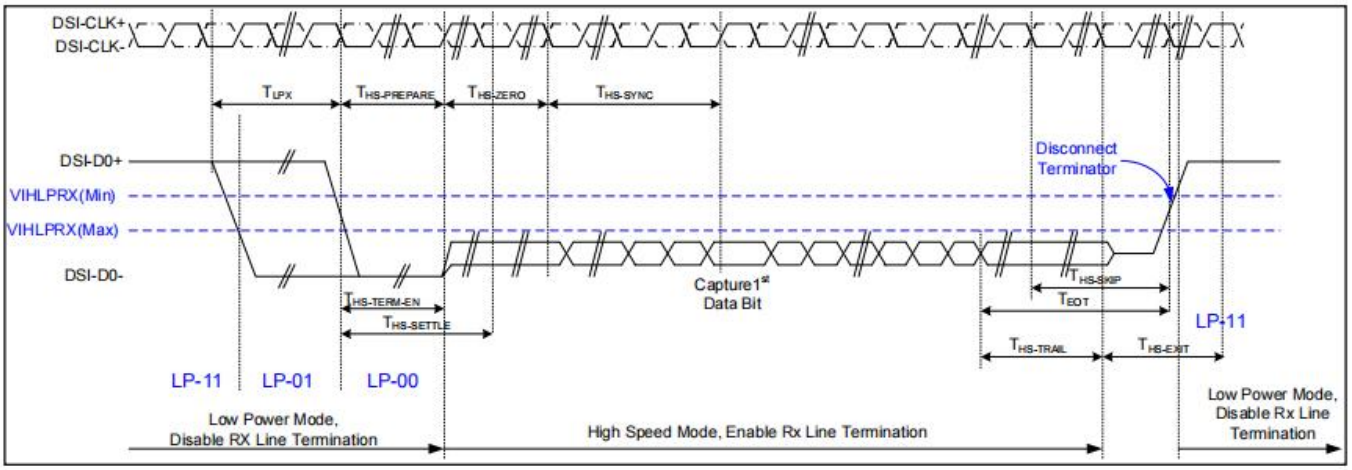
7.4.6 MIPI Interface Characteristics

High Speed Mode – Clock Channel Timing



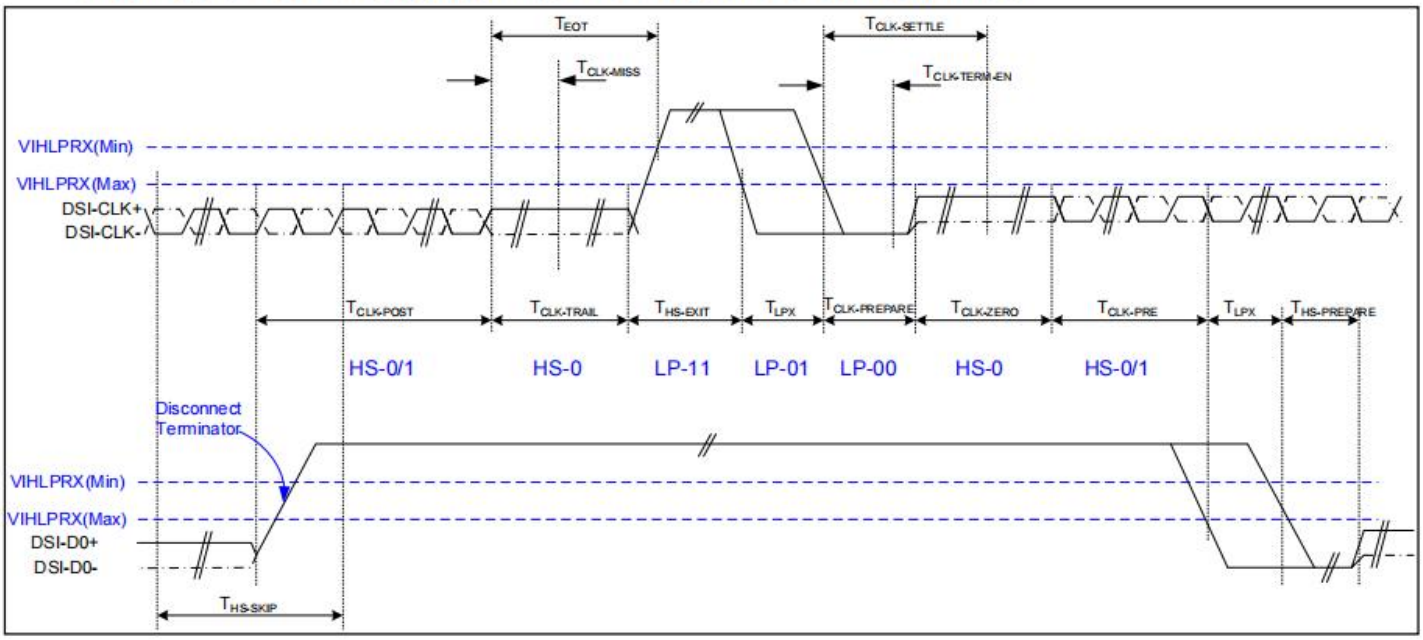
Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-DATA_P/N	2xUI INST	Double UI instantaneous	8	25	ns	
DSI-DATA_P/N	UI INSTA ,UI INSTB	UI instantaneous Half	4	12.5	ns	

High-Speed Data Transmission



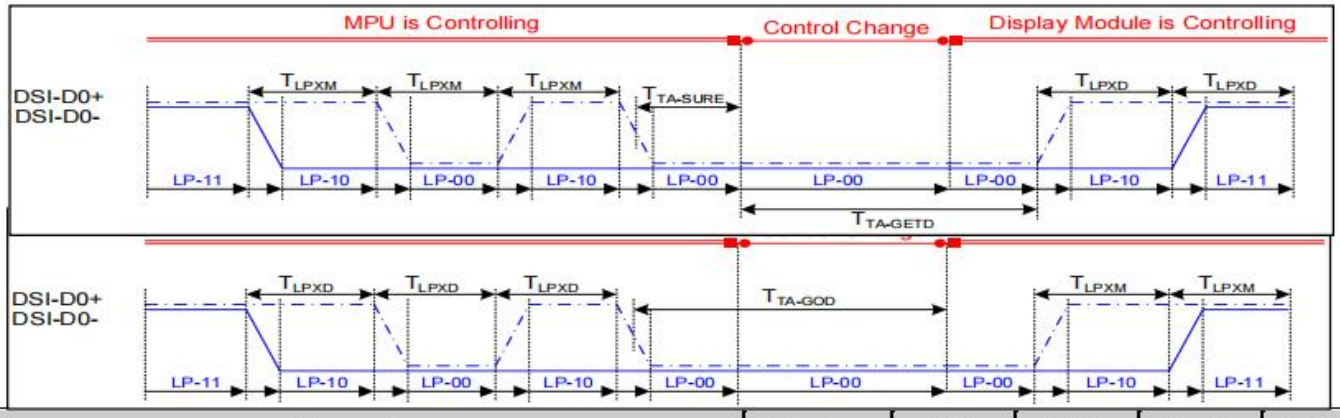
Parameter	Symbol	MIN	TYP	MAX	Unit
Time to drive LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40+4UI		85+6UI	ns
Time from start of t HS-TRAIL or t CLK-TRAIL period to start of LP-11 state	T_{EOT}			105+12UI	ns
Time to enable data receiver line termination measured from when Dn crosses VILMAX	$T_{HS-TERM-EN}$			35+4UI	ns
Time to drive flipped differential state after last payload data bit of a HS transmission	$T_{HS-TRAIL}$	60+4UI			ns
Time-out at RX to ignore transition period of EoT	$T_{HS-SKIP}$	40		55+4UI	ns
Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	100			ns
Length of any Low-Power state period	T_{LPX}	50			ns
Sync sequence period	$T_{HS-SYNC}$		8UI		ns
Minimum lead HS-0 drive period before the Sync sequence	$T_{HS-ZERO}$	105+6UI			ns

Switching the Clock Lane between Clock Transmission and Low-Power Mode



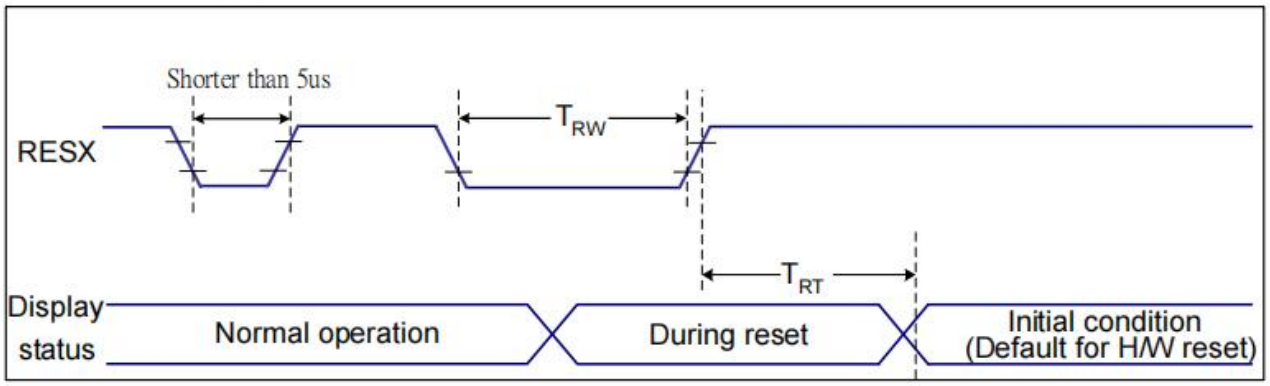
Parameter	Symbol	MIN	TYP	MAX	Unit
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLK-POST}$	60+52UI			ns
Detection time that the clock has stopped toggling	$T_{CLK-MISS}$			60	ns
Time to drive LP-00 to prepare for HS clock transmission	$T_{CLK-PREPARE}$	38		95	ns
Minimum lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE}$ +$T_{CLK-ZERO}$	300			ns
Time to enable Clock Lane receiver line termination measured from when Dn cross VIL,MAX	$T_{HS-TERM-EN}$			38	ns
Minimum time that the HS clock must be set prior to any associated date lane beginning the transmission from LP to HS mode	$T_{CLK-PRE}$	8			UI
Time to drive HS differential state after last payload clock bit of a HS transmission burst	$T_{CLK-TRAIL}$	60			ns

Bus Turnaround Procedure



Parameter	Symbol	MIN	TYP	MAX	Unit
Length of any Low-Power state period : Master side	T_{LPX}	50		75	ns
Length of any Low-Power state period : Slave side	T_{LPX}	47.5	50	52.5	ns
Ratio of T_{LPX} (MASTER)/ T_{LPX} (SLAVE) between Master and Slave side	Ratio T_{LPX}	2/3		3/2	
Time-out before new TX side start driving	$T_{TA-SURE}$	T_{LPX}		2 T_{LPX}	ns
Time to drive LP-00 by new TX	T_{TA-GET}		5 T_{LPX}		ns
Time to drive LP-00 after Turnaround Request	T_{TA-GO}		4 T_{LPX}		ns

7.4.7 Reset Timing



VDDI=1.8V,VDD=2.8V, GND=RGND=0V, Ta=25℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
			-	120 (Note 1, 6, 7)	ms

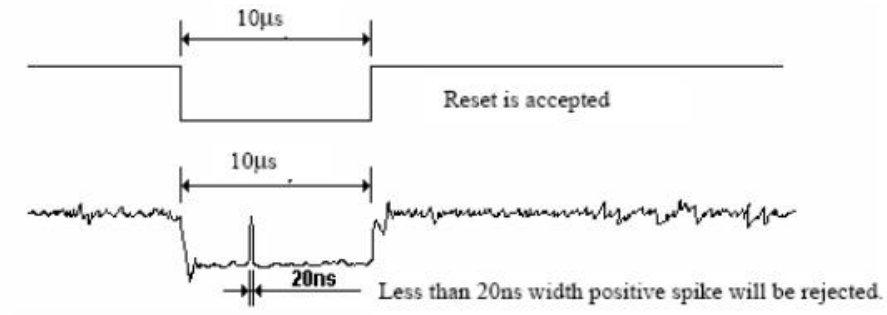
Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. *During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.*
4. *Spike Rejection also applies during a valid reset pulse as shown below:*



5. *When Reset applied during Sleep In Mode.*
6. *When Reset applied during Sleep Out Mode.*
7. *It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.*

8. Electro-Optical Characteristics

Item		Symbol	Condition	Min	Typ	Max	Unit	Remark
Response time		Tr+ Tf	θ=0° ∅=0°	---	35	45	ms	Note2
Contrast ratio		Cr		900	1200	---	---	Note3
Transmittance (with POL)		T		---	3.7	---	%	C light
Viewing angle range (CR≥10)		θ	∅ = 90°	70	80	---	deg	Note4
			∅ = 270°	70	80	---	deg	
			∅ = 0°	70	80	---	deg	
			∅ = 180°	70	80	---	deg	
NTSC		---	---	---	70	---	%	
CIE(x,y) chromaticity	Red	x	θ=0° ∅=0°	0.638	0.658	0.678	---	Note5 CF glass (C light)
		y		0.312	0.332	0.352		
	Green	x		0.271	0.291	0.311		
		y		0.564	0.584	0.604		
	Blue	x		0.117	0.137	0.157		
		y		0.069	0.089	0.109		
	White	x		0.291	0.311	0.331		
		y		0.320	0.340	0.360		

Note1. Measuring Condition
(1) Measuring surrounding: dark room
(2) Ambient temperature: Ta=25℃
(3) 15min. warm-up time

Note2. Response time is the time required for the display to transition from Black to White (Rise Time, Tr) and from White to Black (Decay Time, Tf). The measurement instrument is DMS-803. For more information, please refer to FIG 1 and FIG 2.

Note3. Contrast Ratio (CR) is defined mathematically as below. Measured at the center point of panel by DMS-803, please refer to FIG 1

$$\textbf{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

Note4. Viewing angle is the angle at which the contrast ratio is greater than 10(CR≥10:1). The measurement instrument is DMS-803. For more information, please refer to FIG 1 and FIG 3.

Note5. CIE (x, y) chromaticity for CF only, measured with Olympus MHL-450 under C light.

FIG. 2 The definition of Response Time

The response time is defined as the following figure and shall be measured by switching the input signal for "black" and "white". This definition is valid for a normally black display. For a normally white display the opposite definition applies.

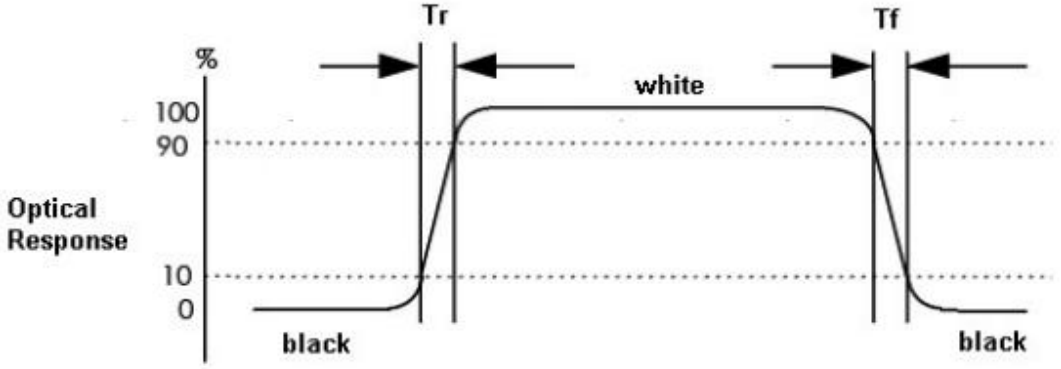
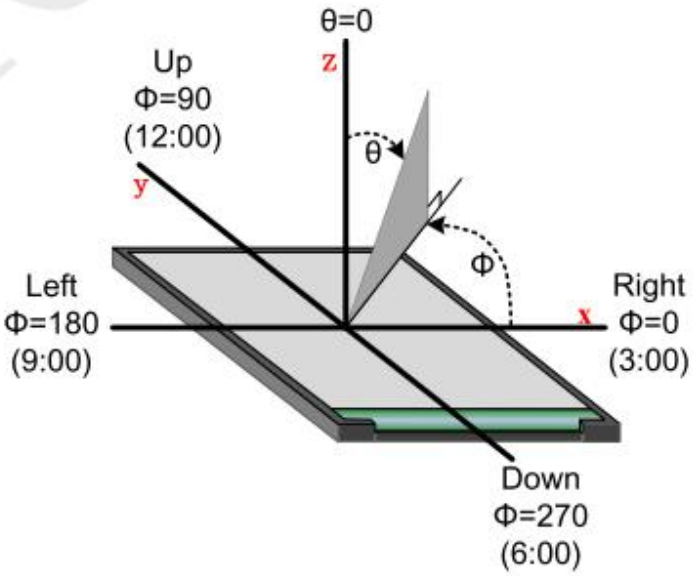
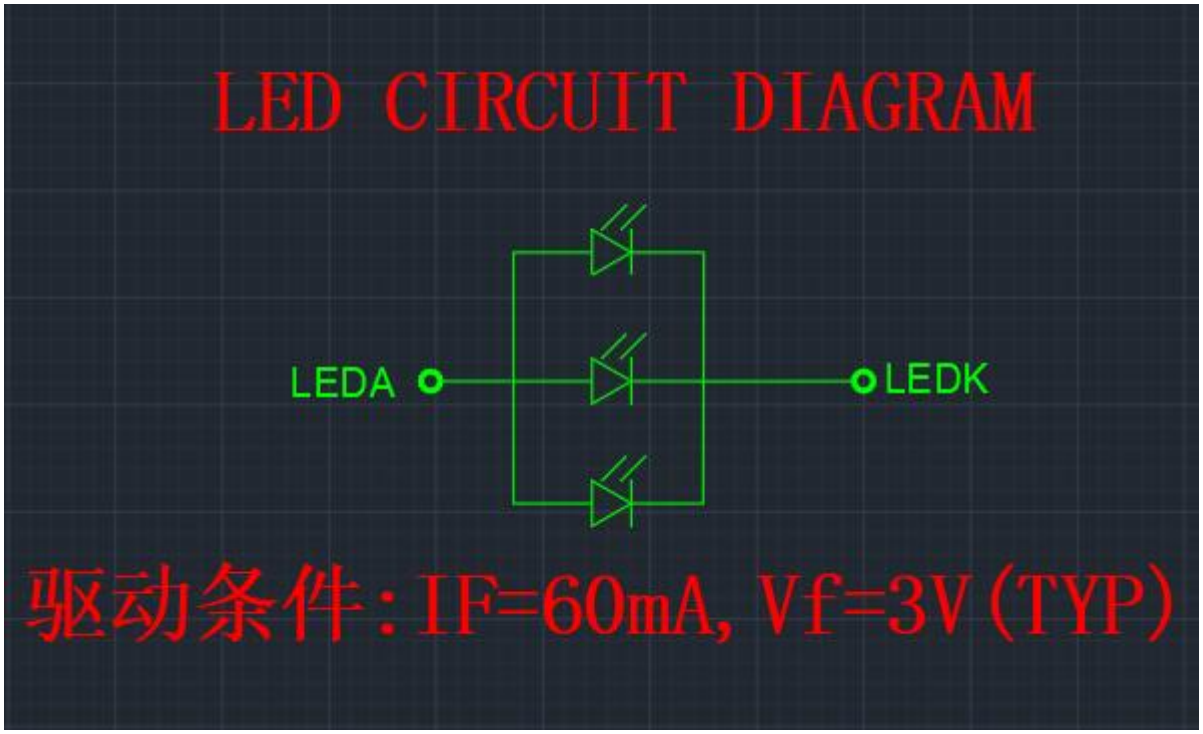


FIG. 3 The definition of viewing angle



Note(4) Backlight circuit



9.Records Of Version

Version	Revise Date	Page	Content
00	2026-6-2	ALL	New released