PRODUCT SPECIFICATION FOR LCD MODULE

Revision: 1.0

Model No: LS0397I01-MP-V1

Module Type: COG+FPC+B/L

APPROVED SIGNATURE

■ Approved Product Specification only

□ Approved Product Specification and Samples

Prepared By	Checked By	Approved By

Contents

目录

1. General Description

LS0397I01-MP-V1is a transmissive type a-Si TFT-LCD (amorphous silicon thin film transistor liquid crystal display) module, which is composed of a TFT-LCD panel, a driver circuit and a backlight unit. The panel size is 3.97 inch and the resolution is 480(RGB)*800, the panel can display up to 16.7M colors. The LCM can be easily accessed by RGB interface.

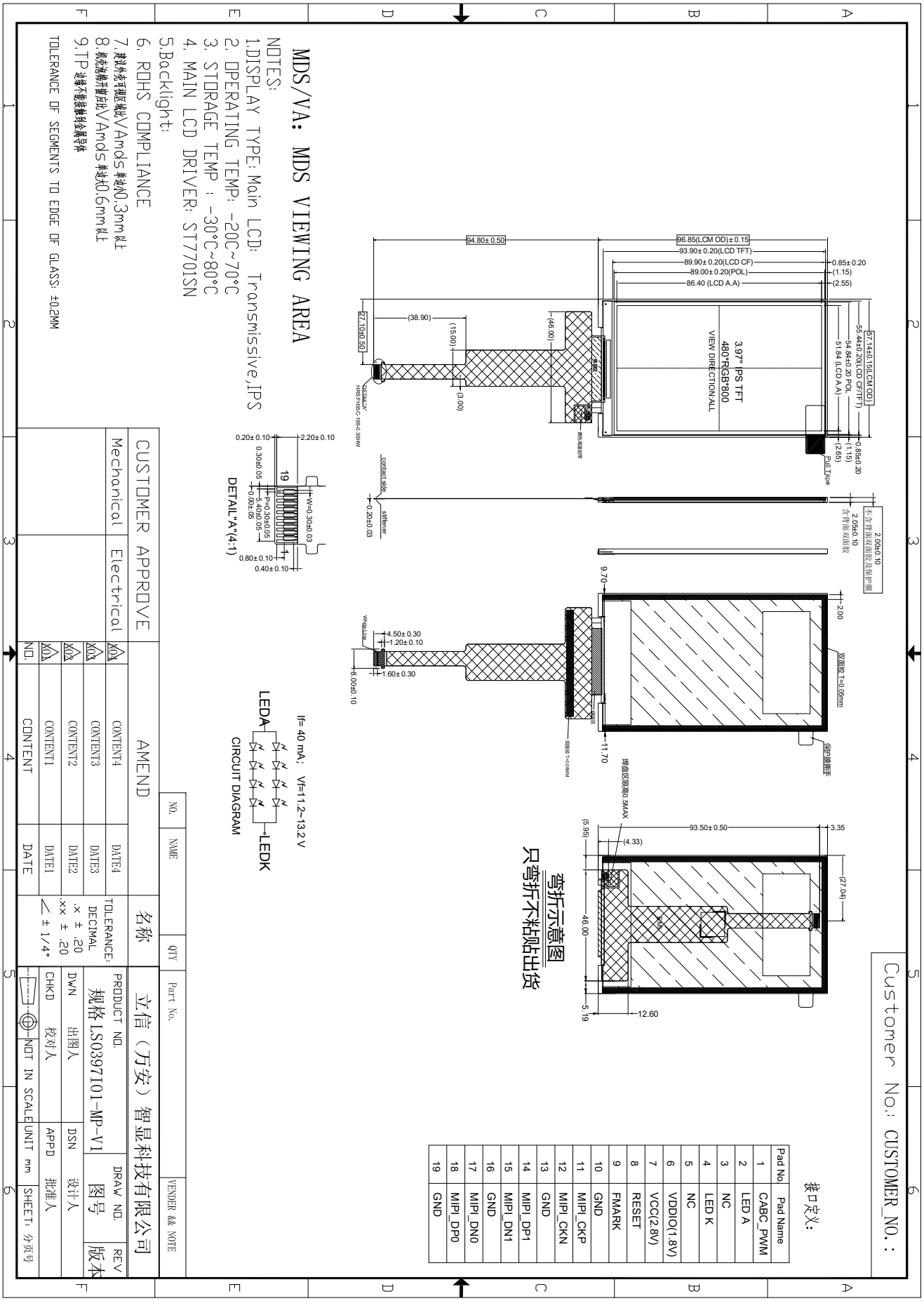
2. Physical Features

Display Mode	TFT-LCD Module
	Active matrix TFT, Transmissive type
Display Format	Graphic 480(RGB)×800 Dot-matrix
Input Data	MIPI
Viewing Direction （Grayscale Inversion）	Free（IPS）

3. Mechanical Specification

Item	Specification	Unit
Module size (H×V×D)	57.14 ×96.85 ×2.0	mm
Number of dots	480(RGB) ×800	pixel
Active area (H×V)	51.84×86.4	mm

4. Outline Dimension



5. Absolute Maximum Ratings

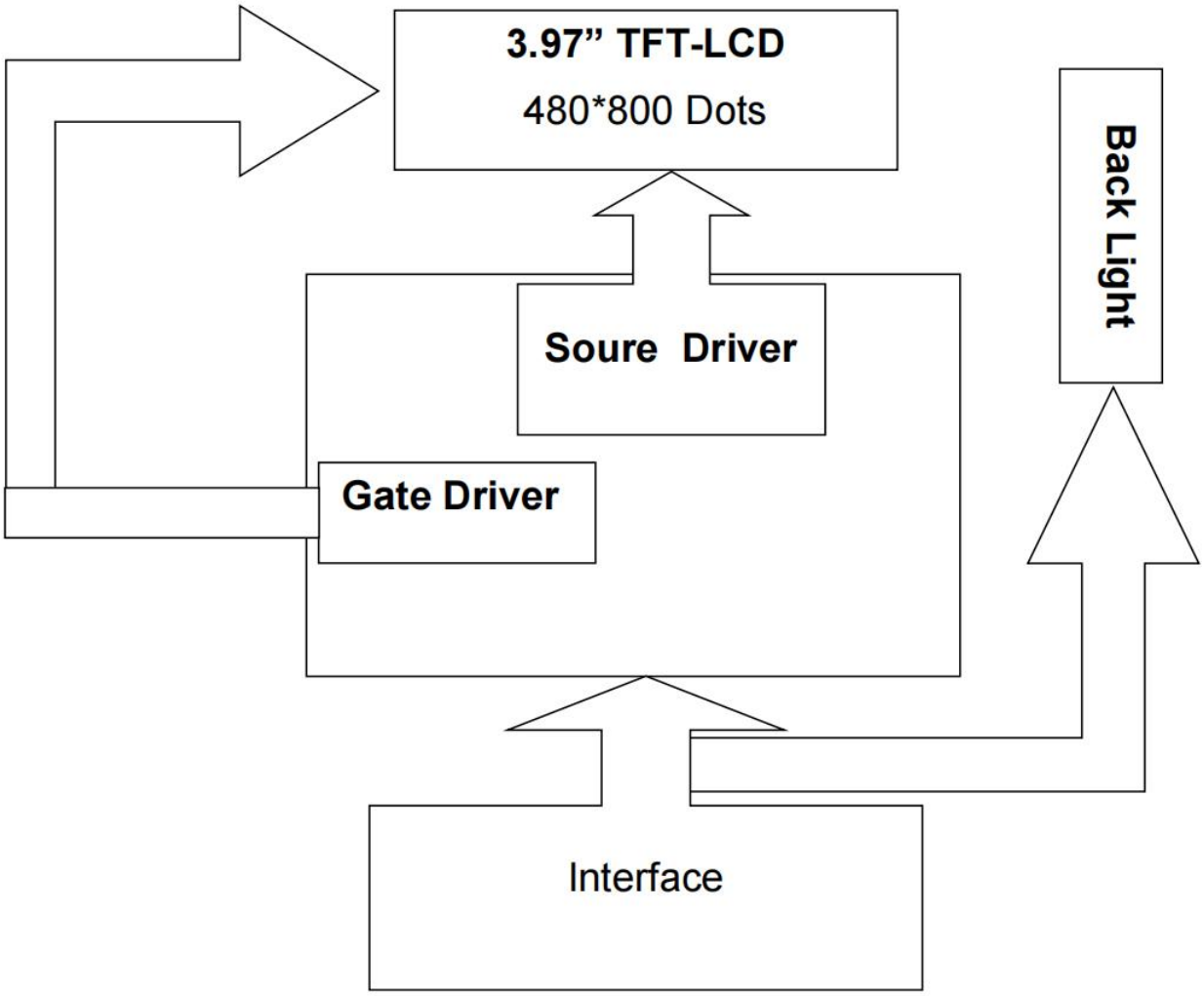
Item	Symbol	Min	Max	Unit	Remark
Supply voltage	VDD	-0.3	3.6	V	Note1 Note2
Supply voltage	VDDIO	-0.3	3.6	V	
Operating temperature	TOPR	-20	70	℃	
Storage temperature	TSTR	-30	80	℃	

6. Electrical Characteristics

Item		Symbol	Rating			Unit	Remark
			Min	Typ	Max		
Supply voltage		VDD	2.5	2.8	3.3	V	Note1
Supply voltage		VDDIO	1.65	1.8	3.3	V	
Input Voltage	L level	VIL	0	---	0.3*VDDIO	V	
	H level	VIH	0.7*VDDIO	---	VDDIO	V	

7. Module Function Description

7-1. Block Diagram Of LCM

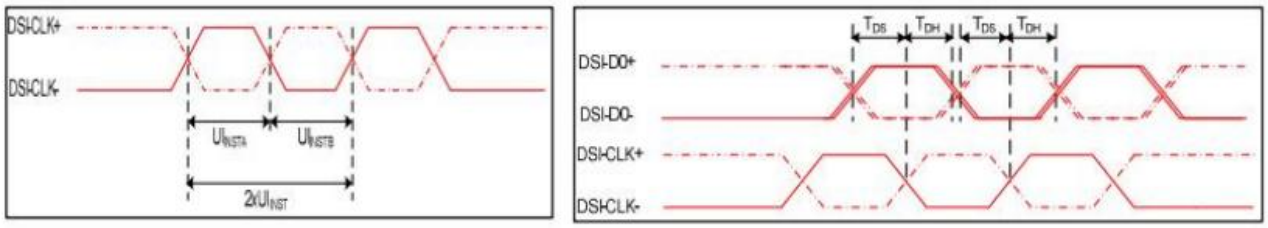


7-2. Pin Description

PIN NO.	Symbol	I/O	Description
1	CABC_PWM	I	Control signal for brightness of LED backlight.
2	LEDA	P	Power for LED backlight anode
3	NC	/	NC
4	LED-	P	Power for LED backlight cathode
5	NC	/	NC
6	VDDIO(1.8V)	P	I/O circuit supply voltage
7	VCC(2.8V)	P	Internal analog power supply
8	RESET	I	Reset signal input pin
9	FMARK	/	TEST
10	GND	P	Power ground
11	MIPI_CLKP	I	Positive polarity of low voltage differential clock signal
12	MIPI_CLKN	I	Negative polarity of low voltage differential clock signal
13	GND	P	Power ground
14	MIPI_1P	I	Positive polarity of low voltage differential data signal
15	MIPI_1N	I	Negative polarity of low voltage differential data signal
16	GND	P	Power ground
17	MIPI_0N	I	Negative polarity of low voltage differential data signal
18	MIPI_0P	I	Positive polarity of low voltage differential data signal
19	GND	P	Power ground

7-3 Timing Characteristics

7.3.1 High Speed Mode



VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-CLK+/-	$2xUI_{INSTA}$	Double UI instantaneous	4	25	ns	
DSI-CLK+/-	UI_{INSTA} UI_{INSTB}	UI instantaneous halfs	2	12.5	ns	$UI = UI_{INSTA} = UI_{INSTB}$
DSI-Dn+/-	tDS	Data to clock setup time	0.15	-	UI	
DSI-Dn+/-	tDH	Data to clock hold time	0.15	-	UI	

Table 7 Mipi Interface- High Speed Mode Timing Characteristics

7.3.2 Lowe Power Mode

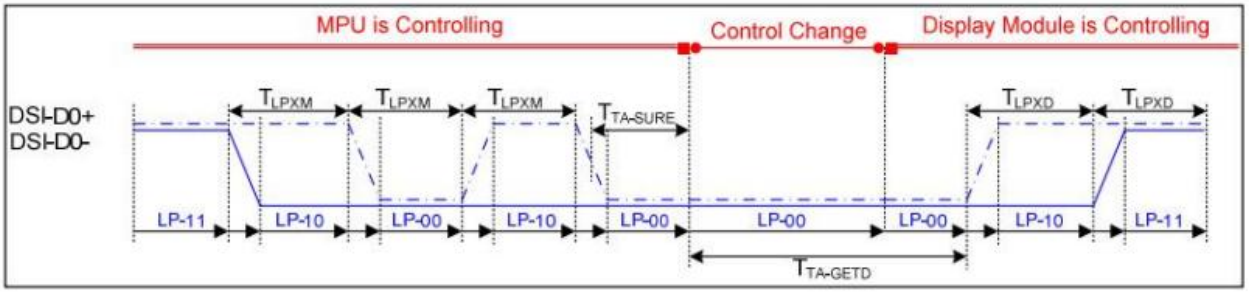


Figure 6 Bus Turnaround (BTA) from display module to MPU Timing

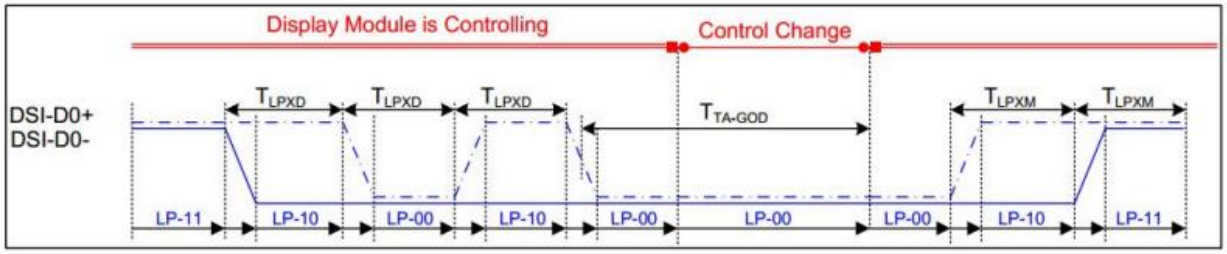


Figure 7 Bus Turnaround (BTA) from MPU to display module Timing

7.4 SIGNAL TIMING SPECIFICATIONS

7.4.1 High-speed Clock Mode

DSI-CLK+/- lanes can be driven to the High Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State Codes.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM).

This sequence is illustrated below.

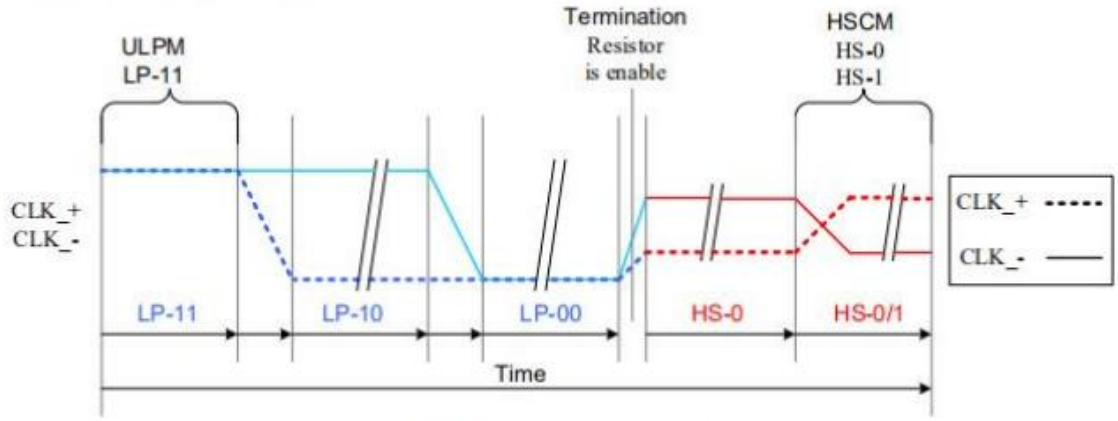


Figure 31 From LPM to HSCM

The mode change is also illustrated below:

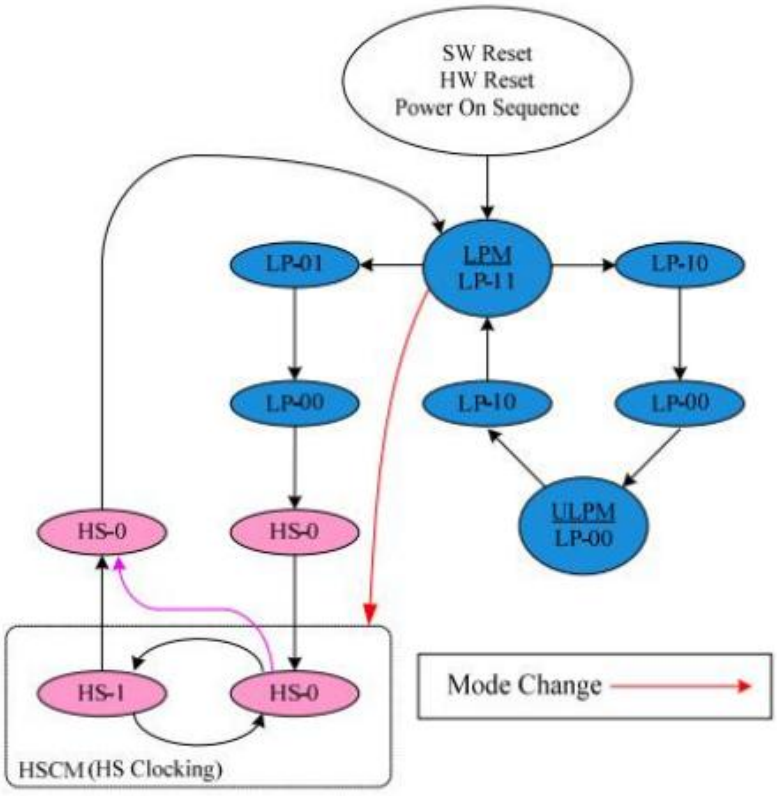
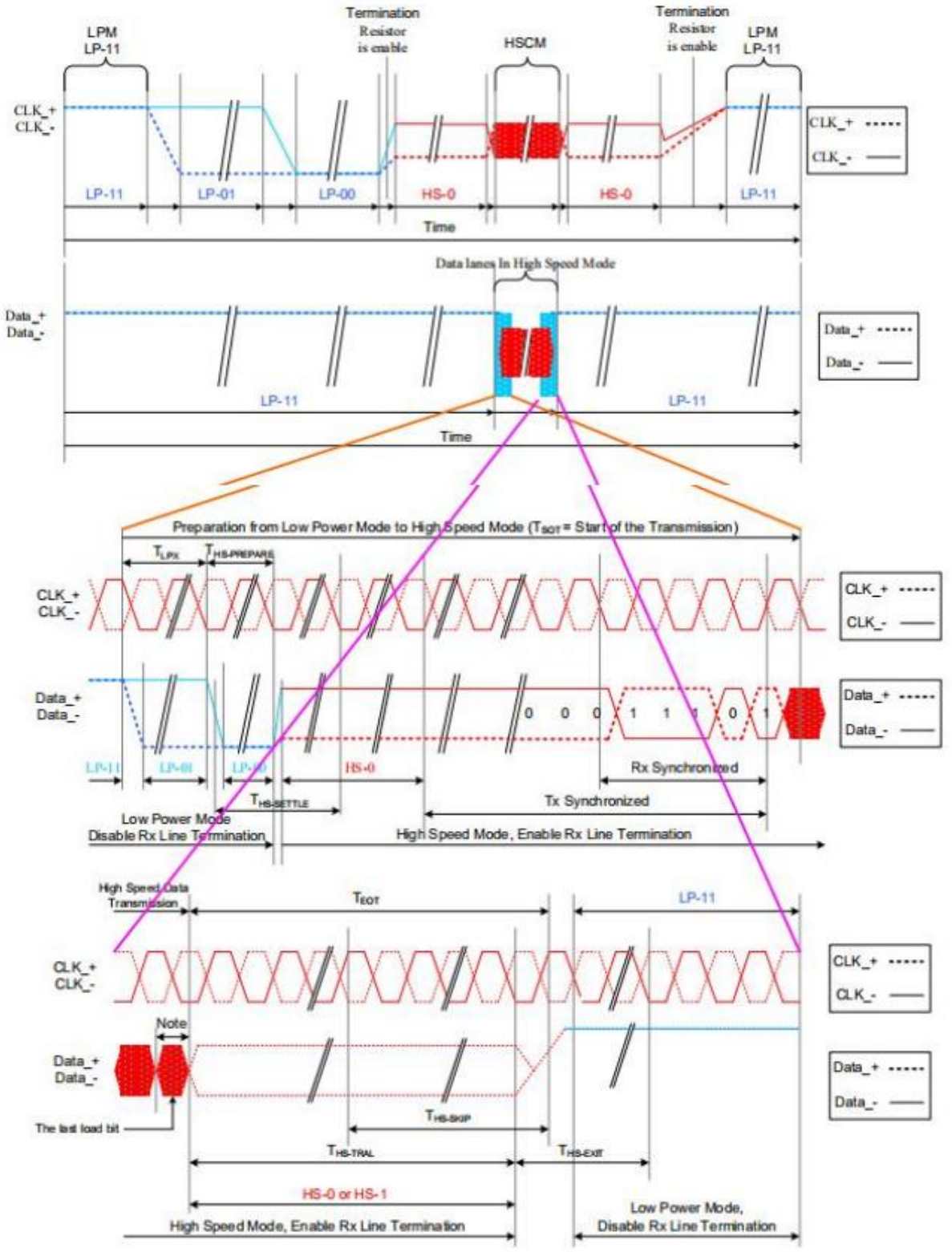


Figure 32 Mode Change from LPM to HSCM on the Flow Chart

The high speed clock (DSI-CLK+/-) is started before high speed data is sent via DSI-Dn+/- lanes. The high speed clock continues clocking after the high speed data sending has been stopped.



7.4.2 Low Power Mode

DSI-CLK+/- lanes can be driven to the Low Power Mode(LMP),when DSI-CLK lanes are entering LP-11 State Code , in three different ways: After SW Reset,HW Reset or Power On Sequence=>LP-11
After DSI-CLK+/- lanes are leaving Ultra Low Power Mode (ULPM,LP-00 State Code)=>LP10=>LP-11(LPM).
This sequence is illustrated below.

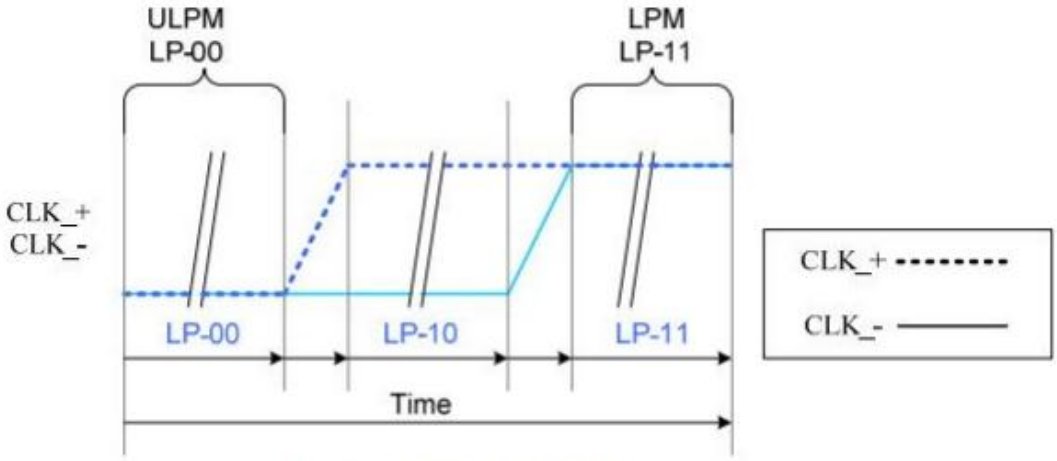


Figure 26 From ULPM to LPM

After DSI-CLK+/- lanes are leaving High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) =>HS-0 =>LP-11 (LPM).

This sequence is illustrated below.

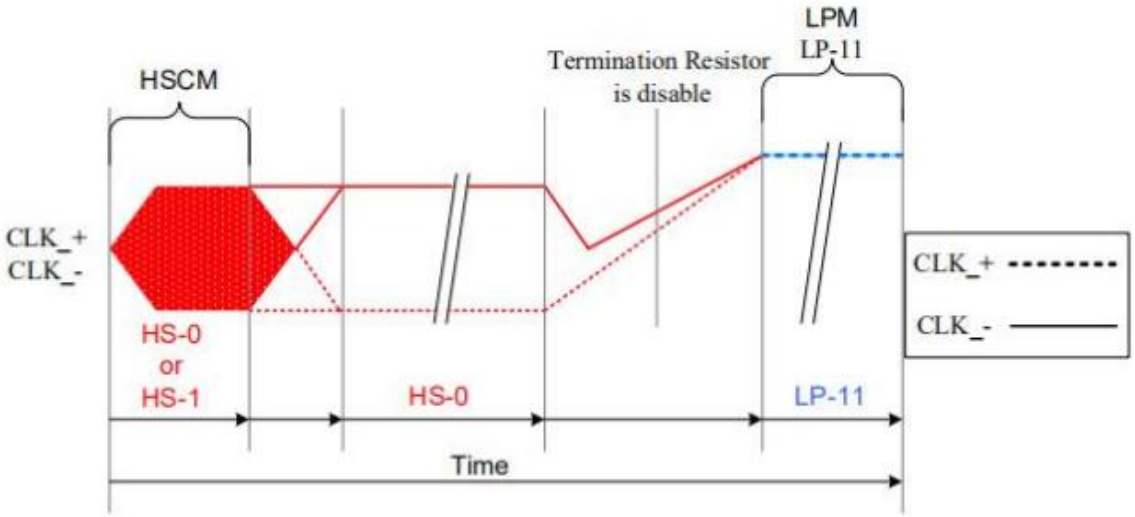


Figure 27 From HSCM to LPM

7.5 Reset Timing

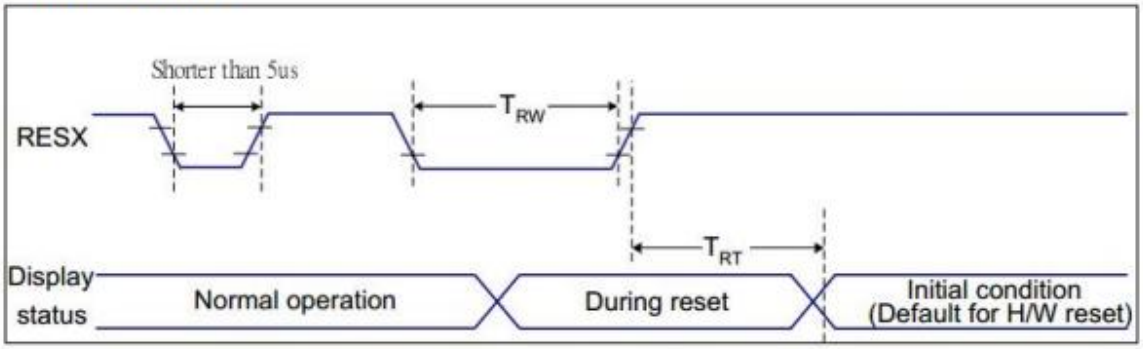


Figure 9 Reset Timing

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120(Note 1, 6, 7)	ms

Notes:

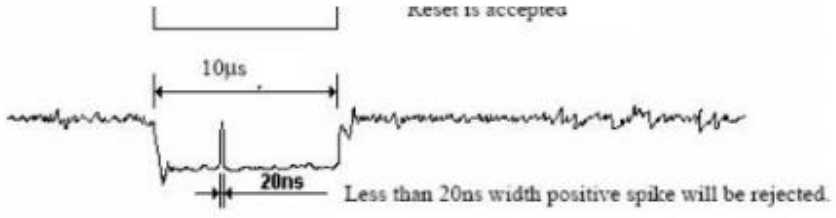
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

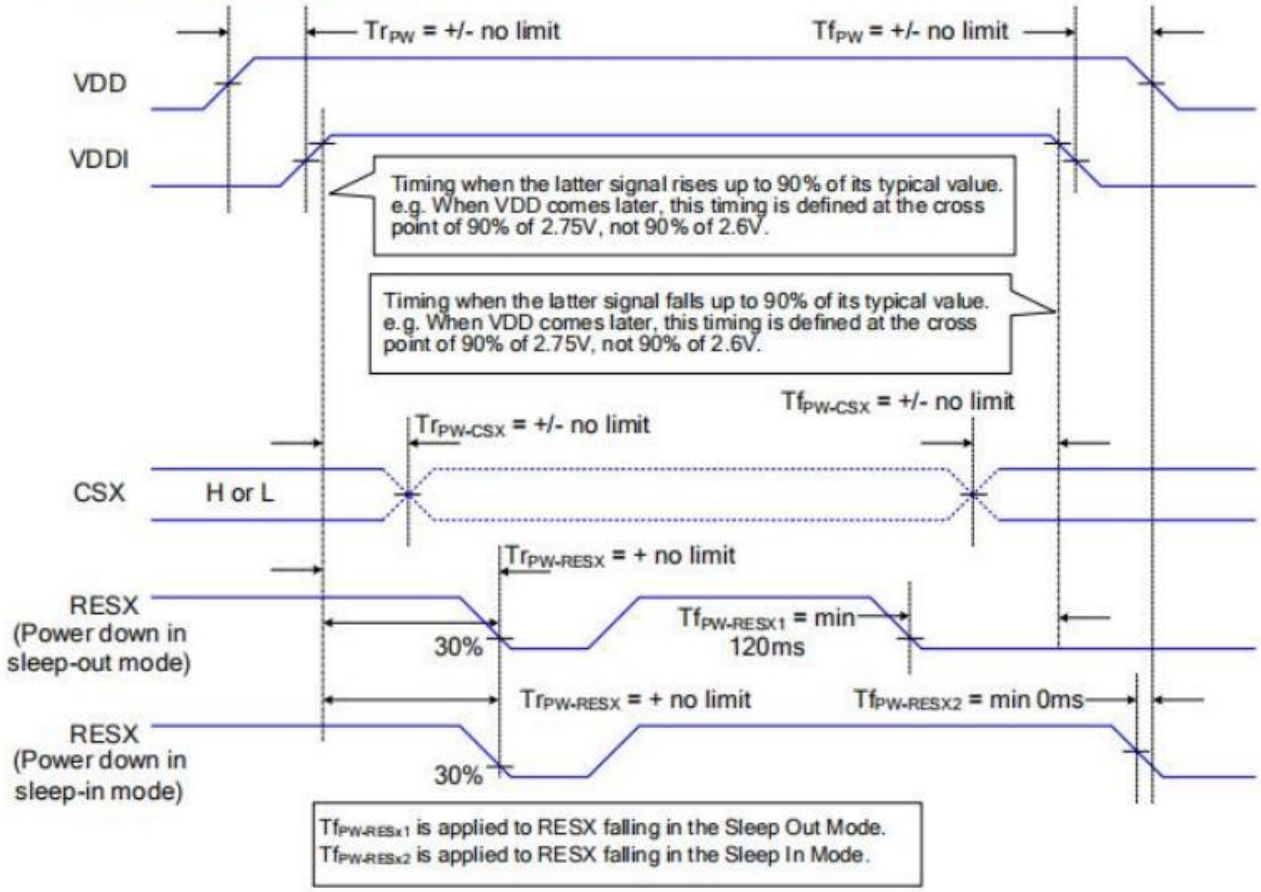
7.6 POWER ON/OFF SEQUENCE

VDDI and VDDA can be applied or powered down in any order. During the Power Off sequence, if the LCD is in the Sleep Out mode, VDDA and VDDI must be powered down with minimum 120msec. If the LCD is in the Sleep In mode, VDDA and VDDI can be powered down with minimum 0msec after the RESX is released. CSX can be applied at any timing or can be permanently grounded. RESX has high priority over CSX.

Notes:

1. There will be no damage to the ST7701S if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
3. There will be no abnormal visible effects on the display between the end of Power On Sequence and before receiving the Sleep Out command, and also between receiving the Sleep In command and the Power Off Sequence.
4. If the RESX line is not steadily held by the host during the Power On Sequence as defined in Sections 9.1 and 9.2, then it will be necessary to apply the Hardware Reset (RESX) after the completion of the Host Power On Sequence to ensure correct operations. Otherwise, all the functions are not guaranteed.

The power on/off sequence is illustrated below



8. Electro-Optical Characteristics

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time		Tr +Tf	θx = θy =0	---	35	---	ms	Note 1
Contrast Ratio		CR		550	800	---	---	Note 2
Transmittance		T%		3.34	3.93	---	%	
Color Chromaticity (CIE1931)	White	W x	θx = θy =0	---	TBD	---	---	
		W y		---	TBD	---	---	
Viewing angle	θ_T		CR > 10	80	85	---	Deg.	Note 3
	θ_B			80	85	---		
	θ_L			80	85	---		
	θ_R			80	85	---		
Luminance (I_F = 40mA)		L		---	400	---	cd/m2	Note4

Note :

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see FIG.2).
2. Contrast measurements shall be made at viewing angle of θ= 0° and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (See FIGURE 1 shown in Appendix) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Transmittance is the value with Polarizer.
4. The color chromaticity coordinates specified in the table above shall be calculated from the spectral data measured with all pixels first in red, green, blue and white; Measurements shall be made at the center of the C/F; Measurement condition is C - light source & Halogen Lamp.
5. The electro-optical response time measurements shall be made as FIG.3 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Tf, and 90% to 10% is Tr.

Figure 1. The definition of Vth & Vsat

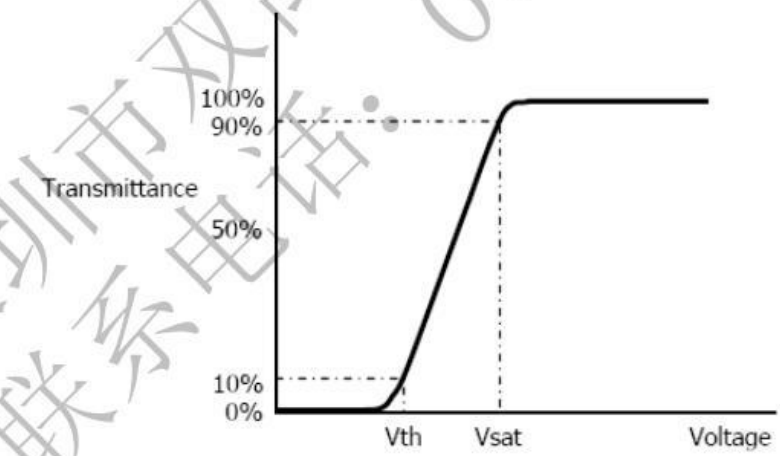


Figure 2. Measurement Set Up

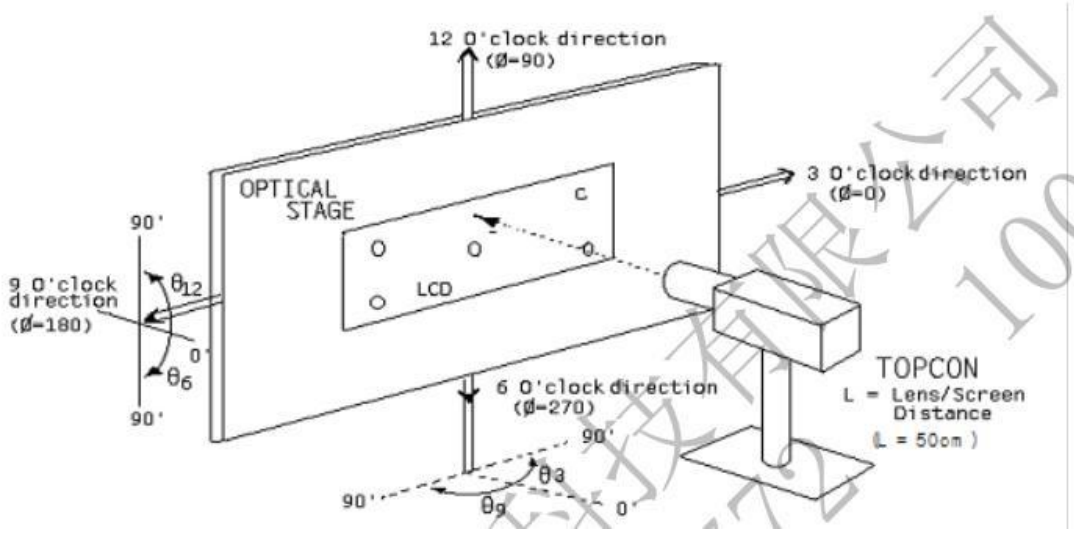
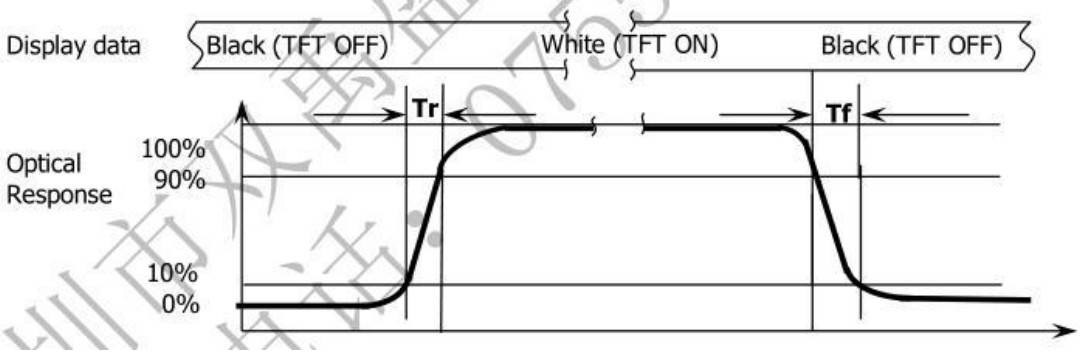


Figure 3. Response Time Testing



9. Reliability

10. 1. MTBF

The LCD module shall be designed to meet a minimum MTBF value of 50000 hours with normal. (25°C in the room without sunlight)

10. 2. Test condition

ITEM	CONDITIONS	CRITERION
OPERATING TEMPERATURE	HIGH TEMPERTURE +70℃ 48HRS	NO DEFECT IN DISPLAYING AND OPERATIONAL FUNCTION
	LOW TEMPERTURE -20℃ 48HRS	
STORAGE TEMPERATURE	HIGH TEMPERTURE +80℃ 48HRS	NO DEFECT IN DISPLAYING AND OPERATIONAL FUNCTION
	LOW TEMPERTURE -30℃ 48HRS	
HUMIDITY	60℃ 90%RH 48HRS	NO DEFECT IN DISPLAYING AND OPERATIONAL FUNCTION

Note：The need to restore at room temperature for 2 hours after the test。

10.Inspection Standards

1. AQL(Acceptable Quality Level)

AQL of major and minor defect

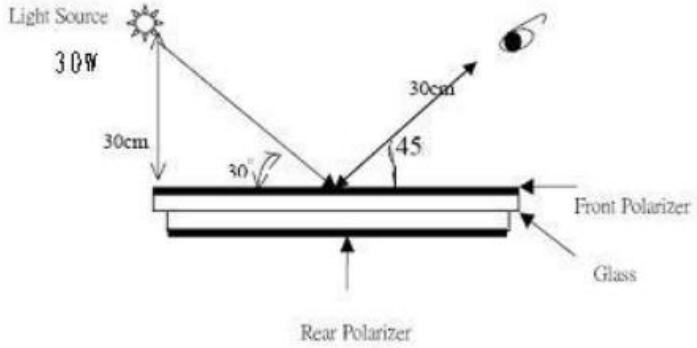
According to GB/T 2828-2003 ; , normal inspection, Class II

MAJOR DEFECT	MINORDEFECT
0.65	1.5

2. Basic conditions for inspection

The LCM face to us, in normal environment, About an angle of incidence 30, a distance of 30cm with normal eye,with an angle of 45 degree to check the products without uncovering the film!

(As shown below)

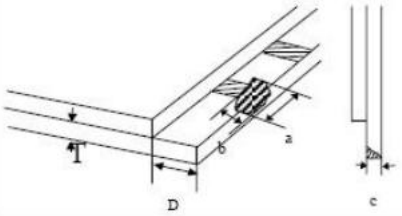
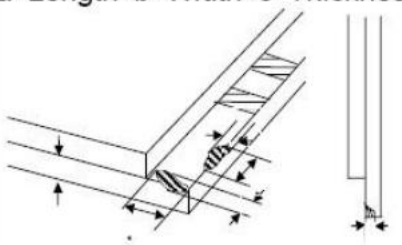


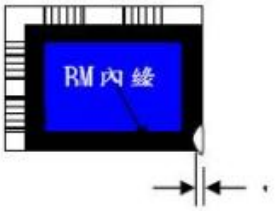
3. Inspection item and criteria

3.1 Visual inspection criterion in immobility

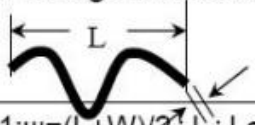
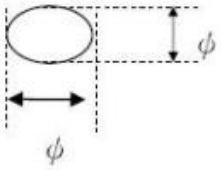
3.1.1 Glass defect

No	Defect item	Criteria	Remark
1	Dimension Unconformity (Major defect)	By Engineering Drawing	

No	Defect item	Criteria	Remark
2	Cracks (Major defect)	1.Linear cracks on panel 【Reject】 2. Nonlinear crack contrast by limited sample	
3	Glass extrude the conductive area (minor defect)	a: disregards and no influence assemblage 1) b≦1/3Pin width(non bonding area) 【Accept】 2) bonding area≦0.5mm 【Accept】	a:Length, b:Width
4	Pin-side，conductive area damaged (minor defect)	(a c：disregards) b≦ 1/3 of effective length for bonding electrode 【Accept】	a：Length，b：Width，c：Thickness 
5	Pin-side，non-conductive area damaged (minor defect)	1) Damage area don't touch the ITO (Inclueling contraposition mark,except scribing mark) 【Accept】 2) c<T b≦BM 1/3 of width 【Accept】 3) c=T b not touch the seal glue 【Accept】 4) a disregards	a：Length，b：Width，c：Thickness 

No	Defect item	Criteria	Remark
6	Non-pin-side damage (minor defect)	c<T 1) b exceeds 1/3 BM 【Reject】 c=T b not touch the seal glue 【Reject】	c : Thickness b: width of damage 

3.1.2 LCD appearance defect (View area)

No	Defect item	Criteria		Remark
1	Fiber、glass cratch、polarizer scratch/folded (minor defect)	Specification	Allowable	note1: L：Length、W：Width note2: disregard if out of AA 
		0.05mm<W≦0.1mm; L≦3.0mm	1	
		W>0.1mm ; L>3.0mm	0	
2	Polarizer bubble、concave and convex (minor defect)	ψ≦0.2mm	disregard	note 1:ψ=(L+W)/2；L：Length、W：Width note2: disregard if out of AA 
		0.2mm<ψ ≦ 0.3mm	2	
		0.3mm<ψ ≦ 0.5mm	1	
		0.5mm<ψ	0	
3	Black dots、dirty dots、impurities、eyewinker (Major defect)	ψ≦0.15mm	disregard	note2: disregard if out of AA 
		0.15mm<ψ ≦ 0.25mm	2	
		0.25mm<ψ ≦ 0.3mm	1	
		0.3mm<ψ	0	
4	Polarizer prick (Major defect)	ψ≦0.1mm	disregard	note1:ψ=(L+W)/2 ；L= Length、W=Width note2: the distance between two dots ＞5mm
		0.1mm<ψ≦0.25mm	3	
		ψ＞0.25mm	0	

3.1.3 .FPC

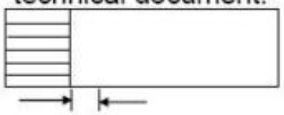
No	Defect item	Criteria		Remark
1	Copper screen peel (Major defect)	Copper screen peel 【Reject】		
2	No release tape or peel (Major defect)	No release tape or peel 【Reject】		
3	Dirty dot and impurity of FPC for customer using side (minor defect)	Specification	Allowable	note1: Cannot have stride ITO impurities
		ψ≦0.25mm	2	
		ψ>0.25	0	

3.1.4 Black tape & Mara tape

1	FPC or H/S black tape shift (minor defect)	1.shift spec: 1)glue to the polarize 【Reject】 2) IC bare 【Reject】 2. left-and-right spec: 1) exceed of FPC edge or H-S edge 【Reject】 2)IC bare 【Reject】	
2	No black tape (Major defect)	No black tape 【Reject】	
3	Tape position mistake (minor defect)	Not by engineering drawing 【Reject】	
4	Mara tape defect (minor defect)	Peel before pulling the protecting film. 【Reject】	

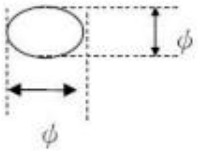
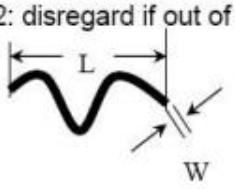
3.1.5 Silicon and Tuffy glue

No	Defect item	Criteria	Remark
1	Quantity of silicon (minor defect)	Uncover the ITO and circuit area. 【Reject】	note: compared by engineering drawing.

No	Defect item	Criteria	Remark
2	Tuffy glue (minor defect)	1. Uncover the reveal copper area 【Reject】 2. Cover layer 0.3mm(Min) ~ 3.0mm(Max) 【accept】	note:if customer has special requirement , refer to the technical document. 
3	Depth of glue covering (minor defect)	Depth of glue covering overtop front Polarizer 【Reject】	Except of the special requirement。

3.2 Electrical criteria

No	Defect item	Criteria	Remark
1	No display (Major defect)	No display 【Reject】	
2	Missing line (Major defect)	Missing line 【Reject】	
3	Seg-com light and dark (Major defect)	Seg-com light and dark 【Reject】	ND filter 2% test
4	No display in immobility (Major defect)	No display in immobility 【Reject】	
5	Flicker of Pattern (Major defect)	Flicker of Pattern 【Reject】	
6	Mura (Major defect)	ND filter 2% test	
7	Over current (Major defect)	Over current 【Reject】	
8	Voltage out of specification (Major defect)	Voltage out of specification 【Reject】	
9	Pattern blur ,error code (Major defect)	Pattern blur ,error code 【Reject】	
10	Dark light, Flicker (Major defect)	Dark light, Flicker 【Reject】	

No	Defect item	Criteria	Remark	
11	Black/White dots 、Dirty dots 、eyewinker (Major defect)	Specification	Allowable	Note1: disregard if out of AA 
		ψ≦0.15mm	disregard	
		0.15mm<ψ ≦ 0.25mm	2	
		0.25mm<ψ ≦ 0.3mm	1	
		0.3mm<ψ	0	
12	Fiber 、glass cratch 、polarizer scratch/folded (minor defect)	W≦0.03mm	disregard	note1: L : Length 、W : Width note2: disregard if out of AA 
		0.03mm<W≦0.05mm ; L≦3.0mm	2	
		0.05mm<W≦0.1mm; L≦3.0mm	1	
		W>0.1mm ; L>3.0mm	0	

3.3 Image sticking

温度条件：室温 20 + 5 ℃ and 50 ℃

测试环境：100±50lux

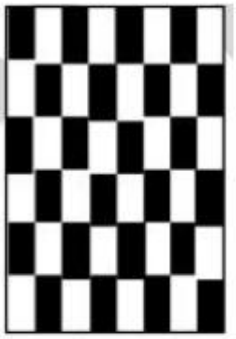
测试方法：

常规残影测试：在棋盘格画面点亮2 hours后，用128灰阶画面检查，常温残影现象需在5min内消

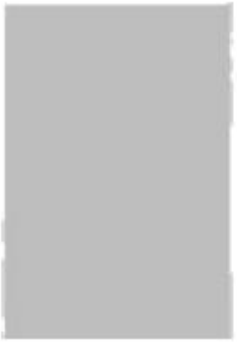
失。

高温50℃残影测试：在棋盘格画面点亮0.5 hours后，用128灰阶画面检查，高温残影现象需在5m

in内消失。



棋盘格画面(6 x 8)
测试画面



128灰阶换面
确认画面

11.Records Of Version

Version	Revise Date	Page	Content
00	2024-4-10	ALL	New released