

PRODUCT SPECIFICATION **FOR LCD MODULE**

Revision: 1.0

Model No: LSC062I02-MP-V2

Module Type: COG+FPC+B/L+CTP

APPROVED SIGNATURE

- ☒ Approved Product Specification only
- ☐ Approved Product Specification and Samples

For Customer's Acceptance

Approved by	Comment

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1. General Description

LSC062I02-MP-V2 is a transmissive type a-Si TFT-LCD (amorphous silicon thin film transistor liquid crystal display) module, which is composed of a TFT-LCD panel, a driver circuit and a backlight unit. The panel size is 6.2 inch and the resolution is 480(RGB)*1280, the panel can display up to 16.7 M colors.

2. Physical Features

Display Mode	TFT-LCD Module
	Active matrix TFT, Transmissive type
Display Format	Graphic 480(RGB)×1280 Dot-matrix
Input Data	MIPI input
Viewing Direction (Grayscale Inversion)	Free (IPS)
Drive	JD9265T

3. Mechanical Specification

Item	Specification	Unit
Module size (H×V×D)	67.25 ×161.7 ×3.58	mm
Number of dots	480(RGB) ×1280	pixel
Active area (H×V)	54.43×146.65	mm

5. Absolute Maximum Ratings

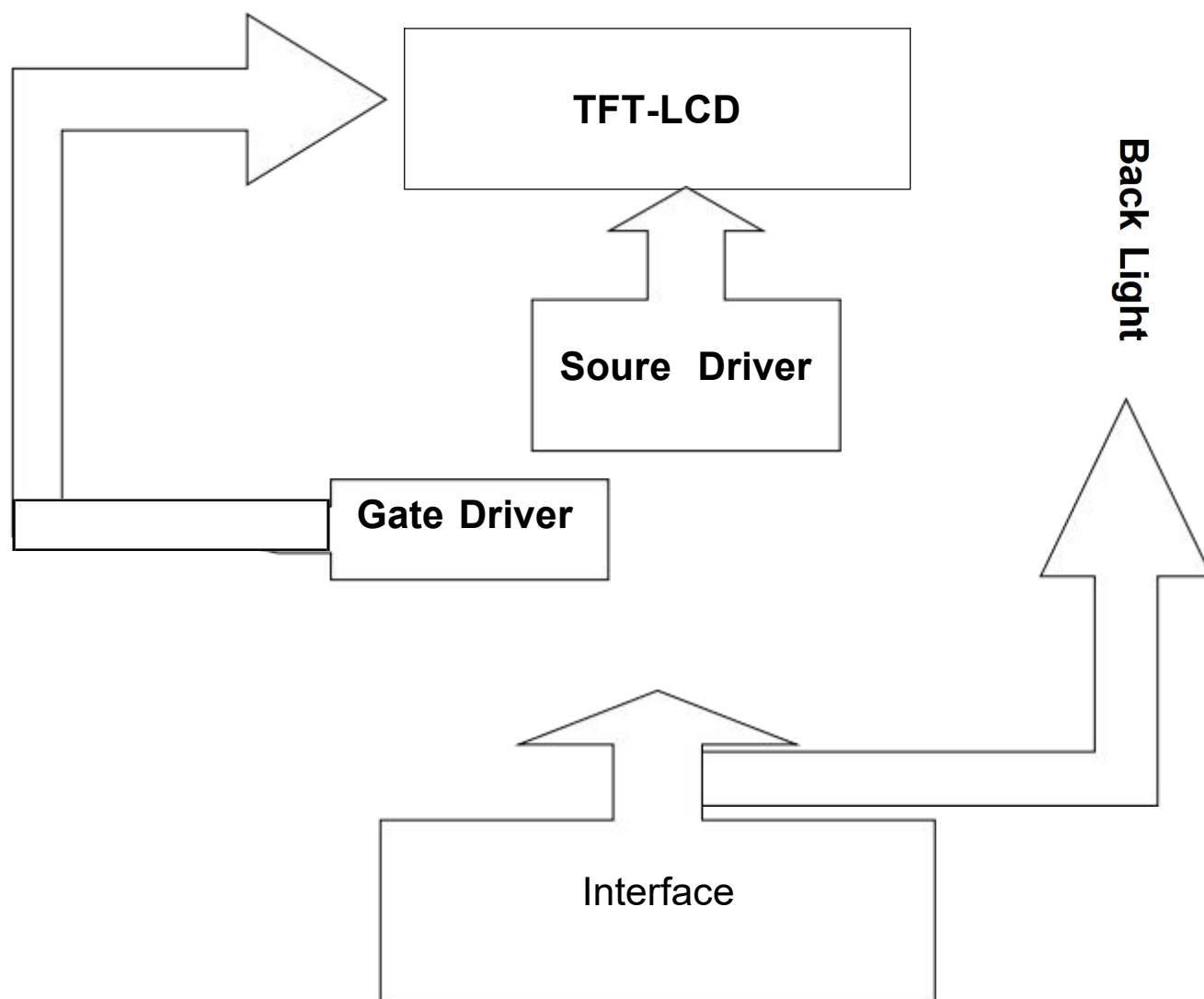
Item	Symbol	Min	Max	Unit	Remark
Supply voltage	VCC	-0.3	4.0	V	Note1 Note2
Supply voltage	IOVCC	-0.3	3.6	V	
Operating temperature	TOPR	-20	70	°C	
Storage temperature	TSTR	-30	80	°C	

6. Electrical Characteristics

Item		Symbol	Rating			Unit	Remark
			Min	Typ	Max		
Supply voltage		VCC	2.5	2.8	3.7	V	Note1
Supply voltage		IOVCC	1.65	1.8	3.3	V	
Input Voltage	L level	VIL	VSS	---	0.3*IOVCC	V	
	H level	VIH	0.7*IOVCC	---	IOVCC	V	

7. Module Function Description

7- 1. Block Diagram Of LCM



7-2. Pin Description

PIN NO.	Symbol	I/O	Description
1	NC		
2	RESET	I	Global reset pin
3	IOVCC	P	Power voltage
4	VDD	P	Power voltage
5	GND	P	GND
6	D1P	I	Negative MIPI differential data inputs
7	D1N	I	Negative MIPI differential data inputs
8	GND	P	GND
9	CLKP	I	Negative MIPI differential clock inputs
10	CLKN	I	Negative MIPI differential clock inputs
11	GND	P	GND
12	D0P	I	Negative MIPI differential data inputs
13	D0N	I	Negative MIPI differential data inputs
14	GND	P	GND
15	GND	P	GND
16	GND	P	GND
17	GND	P	GND
18	GND	P	GND
19	GND	P	GND
20	GND	P	GND
21	GND	P	GND
22	GND	P	GND
23	GND	P	GND
24	GND	P	GND
25	GND	P	GND
26	GND	P	GND
27	GND	P	GND
28	GND	P	GND
29	GND	P	GND
30	GND	P	GND
31	GND	P	GND
32	TP_RST	I	Reset signal for TP
33	TP_INT	I	Interrupt request to the host, or Wakeup request from the host.
34	TP_SDA	I	12C Data input & Output
35	TP_SCL	I	12C Clock input
36	TP_VDD	P	Power voltage
37	GND	P	GND
38	LEDK	P	Backlight LED Cathode.
39	LEDA	P	Backlight LED Anode.

7-3 Timing Characteristics

11.3.1. Reset input timings

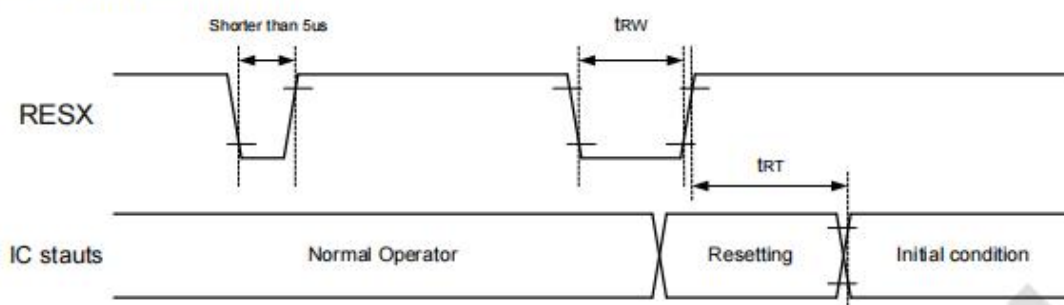


Figure 11.1: Reset input timings

Symbol	Parameter	Related pins	Min.	Max.	Unit
t_{RW}	Reset pulse width ⁽²⁾	RESX	10	-	μs
t_{RT}	Reset complete time ⁽³⁾	-	-	5 (Note 5)	ms
		-	-	120 (Note 6, 7)	ms

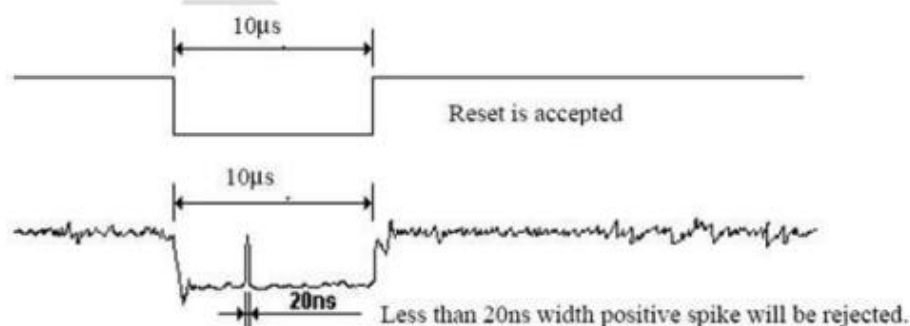
Note: (1) The reset complete time also required time for loading ID bytes from OTP to registers. This loading is done every time when there is HW reset cancel time (t_{RT}) within 5 ms after a rising edge of RESX.

(2) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5 μs	Reset Rejected
Longer than 10 μs	Reset
Between 5 μs and 10 μs	Reset Start

(3) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then returns to Default condition for H/W reset.

(4) Spike Rejection also applies during a valid reset pulse as shown below:



(5) When Reset is applied during Sleep In Mode.

(6) When Reset is applied during Sleep Out Mode.

(7) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

(8) After Sleep Out Command, it is necessary to wait 120msec then send RESX.

Table 11.3: Reset timings

11.3.6.DSI D-PHY electronic characteristics

The Description of D-PHY Layer

In general, the DSI - PHY may contain the following electrical functions: Low-Power Receiver (LP-RX), High-Speed Receiver (HS-RX), the Low-Power Contention Detector (LP-CD), and Low Power Transmitter (LP-TX). Figure 11.5 shows the complete set of electronic functions required for a fully featured PHY transceiver.

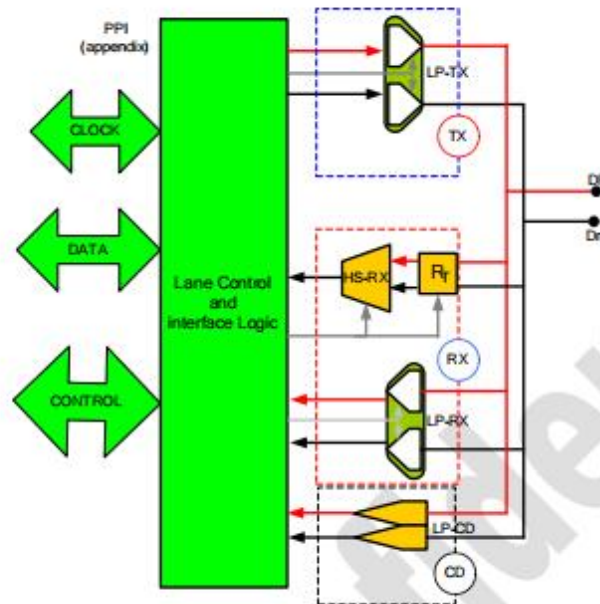


Figure 11.5: Electronic functions of a D-PHY transceiver

Figure 11.6 shows both the HS and LP signal levels of electronic characteristics, respectively. Where, the HS receiver utilizes low-voltage swing differential signaling. The LP transmitter and LP receiver utilize low-voltage swing single signaling. Because the HS signaling levels are below the LP low-level input threshold, Lane switches between Low-Power and High-Speed mode during normal operation.

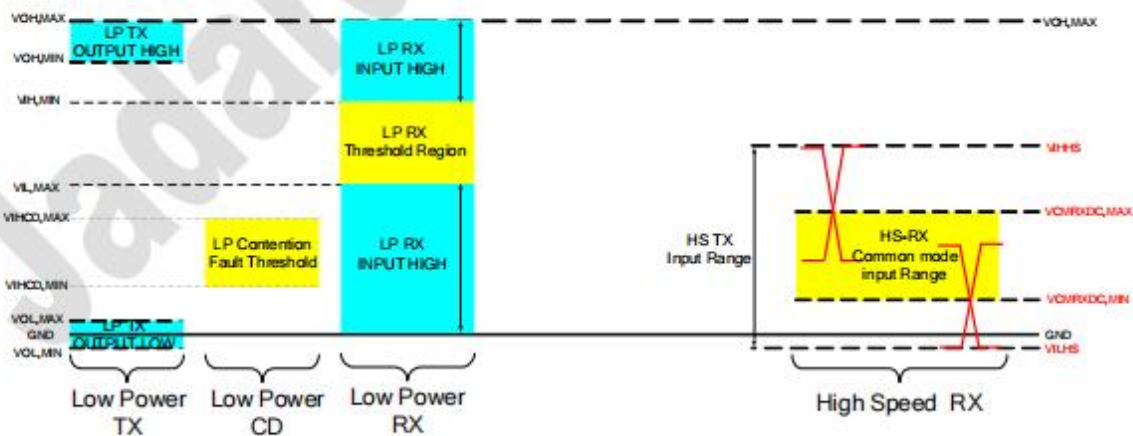


Figure 11.6: HS and LP signal levels

The Electronic Characteristics of Low-Power Transmitter (TX)

The Low-Power TX shall be a slew-rate controlled push-pull driver. It is used for driving the Lines in all Low-Power modes. Hence, it is important to keep static power consumption of a LP TX be as low as possible. Under tables list DC and AC characteristic for Low power transmitter.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{OH}	Thevenin output high level	1.1	1.2	1.3	V	-
V_{OL}	Thevenin output low level	-50	-	50	mV	
Z_{OLP}	Output impedance of LP-TX	110	-	-	Ω	(1)

Note: (1) Though no maximum value for Z_{OLP} is specified, the LP transmitter output impedance shall ensure the t_{RLP}/t_{FLP} specification is met.

Table 11.4: LP-TX DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
t_{RLP}/t_{FLP}	15%-85% rise time and fall time	-	-	25	ns	(1)
$T_{LP-PER-TX}$	Period of the LP exclusive-OR clock	90			ns	
$\delta V/\delta t_{SR}$	Slew rate @ CLOAD = 0pF	30	-	500	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 5pF	-	-	300	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 20pF	-	-	250	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 70pF	-	-	150	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 0 to 70pF (Rising Edge Only)	30	-	-	mV/ns	(1),(3),(7)
	Slew rate @ CLOAD = 0 to 70pF (Rising Edge Only)	30 - 0.075 * ($V_{O,INST} - 700$)	-	-	mV/ns	(1),(8),(9)
	Slew rate @ CLOAD = 0 to 70pF (Falling Edge Only)	30	-	-	mV/ns	(1),(2),(3)
C_{LOAD}	Load capacitance	-	-	70	pF	-

Note: (1) CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.

(2) When the output voltage is between 400 mV and 930 mV.

(3) Measured as average across any 50 mV segment of the output signal transition.

(4) This parameter value can be lower than TLPX due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters.

(5) This value represents a corner point in a piecewise linear curve.

(6) When the output voltage is in the range specified by VPIN(absmax).

(7) When the output voltage is between 400 mV and 700 mV.

(8) Where $V_{O,INST}$ is the instantaneous output voltage, VDP or VDN, in millivolts.

(9) When the output voltage is between 700 mV and 930 mV.

Table 11.5: LP-TX AC Specifications

The Electronic Characteristics of Receiver (RX)

This part includes two parts which Low-Power RX and High-Speed RX. Because they have differential DC and AC characteristic, first to describe LP-RX then describe HS-RX.

Low-Power Receiver (RX)

The low power receiver is an un-terminated, single-ended receiver circuit. The LP receiver is used to detect the Low-Power state on each pin. For high robustness, the LP receiver shall filter out noise pulses and RF interference. It is recommended the implementer optimize the LP receiver design for low power. The LP receiver shall reject any input glitch when the glitch is smaller than $eSPIKE$. The filter shall allow pulses wider than T_{MIN} to propagate through the LP receiver. The Figure 11.7 shows Input Glitch Rejection of Low-Power RX. In addition, under tables list DC and AC characteristic for LP-RX.

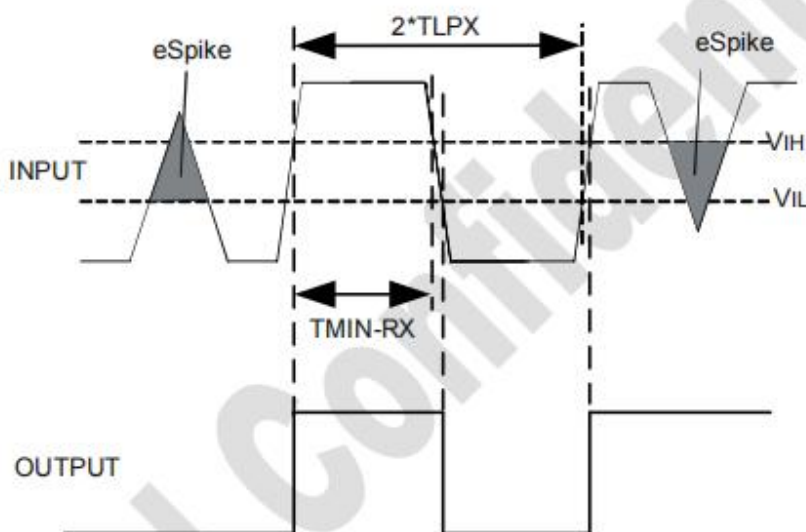


Figure 11.7: Input Glitch Rejections of Low-Power Receivers

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{IH}	Logic 1 input threshold	880	-	-	mV	-
V_{IL}	Logic 0 input threshold, not in ULP state	-	-	550	mV	-

Table 11.6: LP-RX DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
$eSPIKE$	Input pulse rejection	-	-	300	V.ps	1, 2, 3
T_{MIN}	Minimum pulse width response	20	-	-	ns	4
V_{INT}	Peak-to-peak interference voltage	-	-	200	mV	-
f_{INT}	Interference frequency	450	-	-	MHz	-

Note: (1) Time-voltage integration of a spike above V_{IL} when being in LP-0 state or below V_{IH} when being in LP-1 state

(2) An impulse less than this will not change the receiver state.

(3) In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.

(4) An input pulse greater than this shall toggle the output.

Table 11.7: LP-RX AC Specifications

Line Contention Detection

Contention can be inferred by following conditions:

1. Detect an LP high fault when the LP transmitter is driving high and the pin voltage is less than V_{IL} .
2. Detect an LP low fault shall be detected when the LP transmitter is driving low and the pad pin voltage is greater than V_{IHCD} .

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{IHCD}	Logic 1 contention threshold	450	-	-	mV	-
V_{ILCD}	Logic 0 contention threshold	-	-	200	mV	-

Table 11.8: Contention Detector DC Specifications

High-Speed Receiver (RX)

The HS receiver is a differential line receiver. It contains a switch-able parallel input termination, ZID, between the positive input pin D_p and the negative input pin D_n . Under Tables list DC and AC characteristic for HS-RX.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{CMRXDC}	Common-mode voltage HS receive mode	70	-	330	mV	(1),(2)
V_{IDTH}	Differential input high threshold	-	-	70	mV	-
V_{IDTL}	Differential input low threshold	-70	-	-	mV	-
V_{IHHS}	Single-ended input high voltage	-	-	460	mV	(1)
V_{ILHS}	Single-ended input low voltage	-40	-	-	mV	(1)
Z_{ID}	Differential input impedance	80	100	125	Ω	-

Note: (1) Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.

(2) This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz

Table 11.9: HS Receiver DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
$\Delta V_{CMRX(HF)}$	Common mode interference beyond 450 MHz	-	-	100	mV _{PP}	(1)
C_{CM}	Common mode termination	-	-	60	pF	(2)

Note: (1) $\Delta V_{CMRX(HF)}$ is the peak amplitude of a sine wave superimposed on the receiver inputs.

(2) For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.

Table 11.10: HS Receiver AC Specifications

High-Speed Data-Clock Timing

This section specifies the required timings on the high-speed signaling interface independent of the electrical characteristics of the signal. The PHY is a source synchronous interface in the Forward direction. In either the Forward or Reverse signaling modes there shall be only one clock source. In the Reverse direction, Clock is sent in the Forward direction and one of four possible edges is used to launch the data.

The Master side of the Link shall send a differential clock signal to the Slave side to be used for data sampling. This signal shall be a DDR (half-rate) clock and shall have one transition per data bit time. All timing relationships required for correct data sampling are defined relative to the clock transitions. Therefore, implementations may use frequency spreading modulation on the clock to reduce EMI.

The DDR clock signal shall maintain a quadrature phase relationship to the data signal. Data shall be sampled on both the rising and falling edges of the Clock signal. The term "rising edge" means "rising edge of the differential signal, i.e. CLKP – CLKN, and similarly for "falling edge". Therefore, the period of the Clock signal shall be the sum of two successive instantaneous data bit times. This relationship is shown in Figure 11.8.

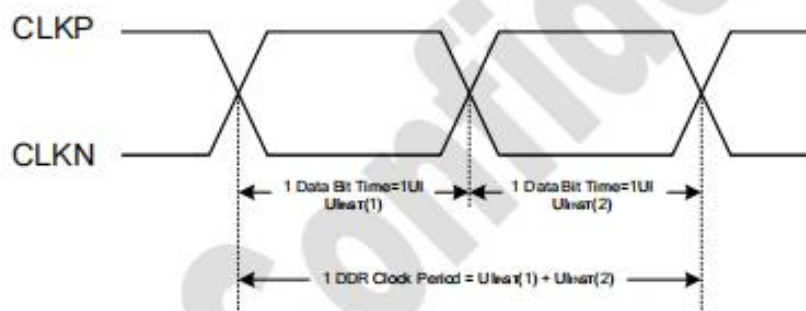


Figure 11.8: DDR Clock Definition

The same clock source is used to generate the DDR Clock and launch the serial data. Since the Clock and Data signals propagate together over a channel of specified skew, the Clock may be used directly to sample the Data lines in the receiver. Such a system can accommodate large instantaneous variations in UI.

The allowed instantaneous UI variation can cause large, instantaneous data rate variations. Therefore, devices shall either accommodate these instantaneous variations with appropriate FIFO logic outside of the PHY or provide an accurate clock source to the Lane Module to eliminate these instantaneous variations.

The UIINST specifications for the Clock signal are summarized in following Table.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
UI instantaneous	UI_{INST}	-	-	12.5	ns	(1), (2), (3), (4), (5), (6)

Note: (1) This value corresponds to a minimum 80 Mbps data rate.

(2) The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.

(3) Maximum total bit rate is 850Mbps of 1 data lane 24-bit data format/ 630Mbps of 1 data lane 18-bit data format/ 560Mbps of 1 data lane 16-bit data format.

(4) Maximum total bit rate is 1.7Gbps of 2 data lanes 24-bit data format/ 1.27Gbps of 2 data lane 18-bit data format/ 1.13Gbps of 2 data lane 16-bit data format.

(5) Maximum total bit rate is 2.62Gbps of 3 data lanes 24-bit data format/ 1.96Gbps of 3 data lane 18-bit data format/ 1.74Gbps of 3 data lane 16-bit data format.

(6) Maximum total bit rate is 2.62Gbps of 4 data lanes 24-bit data format/ 1.96Gbps of 4 data lane 18-bit data format/ 1.74Gbps of 4 data lane 16-bit data format.

Table 11.11: Reverse HS Data Transmission Timing Parameters

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 11.9. Data is launched in a quad-capture relationship to the clock such that the Clock signal edge may be used directly by the receiver to sample the received data.

The transmitter shall ensure that a rising edge of the DDR clock is sent during the first payload bit of a transmission burst such that the first payload bit can be sampled by the receiver on the rising clock edge, the second bit can be sampled on the falling edge, and all following bits can be sampled on alternating rising and falling edges.

All timing values are measured with respect to the actual observed crossing of the Clock differential signal. The effects due to variations in this level are included in the clock to data timing budget.

Receiver input offset and threshold effects shall be accounted as part of the receiver setup and hold parameters.

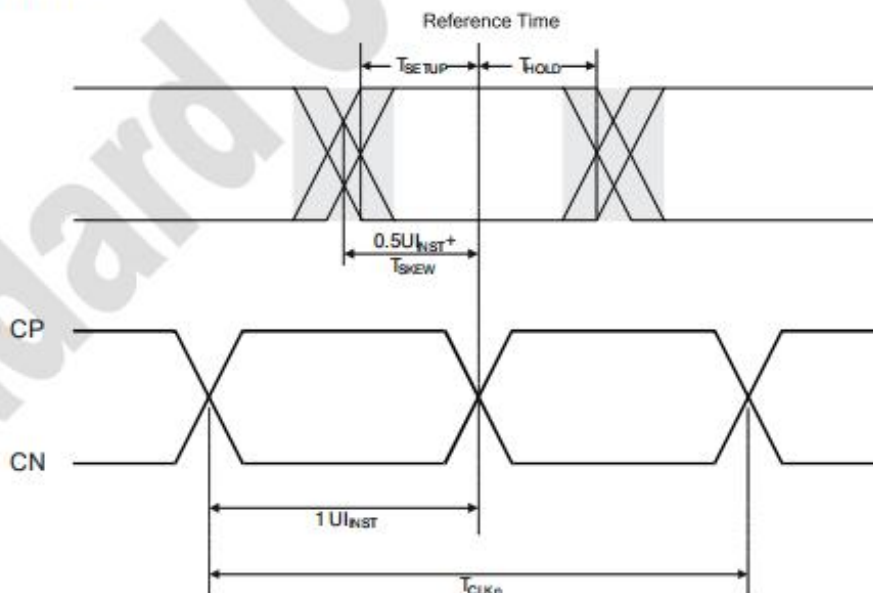


Figure 11.9: Data to Clock Timing Definitions

Data-Clock Timing Specifications

The Data-Clock timing specifications are shown in Table 11.12. Implementers shall specify a value $UI_{INST,MIN}$ that represents the minimum instantaneous UI possible within a High-Speed data transfer for a given implementation. Parameters in Table 11.12 are specified as a part of this value.. The setup and hold times, $T_{SETUP[RX]}$ and $T_{HOLD[RX]}$, respectively, describe the timing relationships between the data and clock signals. $T_{SETUP[RX]}$ is the minimum time that data shall be present before a rising or falling clock edge and $T_{HOLD[RX]}$ is the minimum time that data shall remain in its current state after a rising or falling clock edge. The timing budget specifications for a receiver shall represent the minimum variations observable at the receiver for which the receiver will operate at the maximum specified acceptable bit error rate.

The intent in the timing budget is to leave $0.4 \cdot UI_{INST}$, i.e. $\pm 0.2 \cdot UI_{INST}$ for degradation contributed by the interconnect.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Data to Clock Setup Time [RX]	$T_{SETUP[RX]}$	0.15	-	-	UI_{INST}	1
Clock to Data Hold Time [RX]	$T_{HOLD[RX]}$	0.15	-	-	UI_{INST}	1

Note: (1) Total setup and hold window for receiver of $0.3 \cdot UI_{INST}$.

Table 11.12: Data to Clock Timing Specifications

Burst Mode Data Transmission

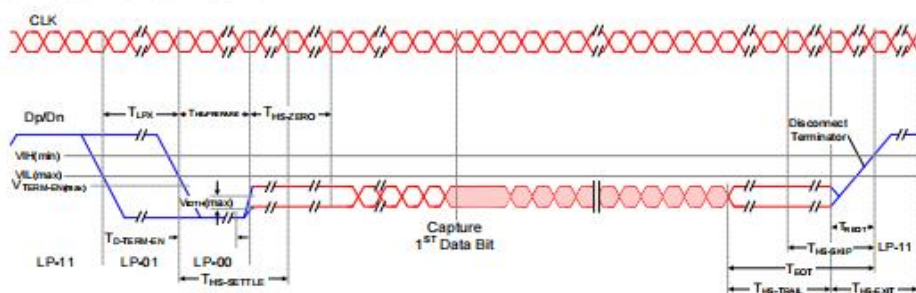


Figure 11.10: High-Speed Data Transmission in Bursts

Parameter	Description	Min	Typ	Max	UNIT
T_{LPX}	Transmitted length of any Low-Power state period	50	-	-	ns
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	$40 + 4 \cdot UI$	-	$85 + 6 \cdot UI$	ns
$T_{HS-PREPARE} + T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	$145 + 10 \cdot UI$	-	-	ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination.	-	-	$35 + 4 \cdot UI$	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions.	$85 + 6 \cdot UI$	-	$145 + 10 \cdot UI$	ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	$\max(n \cdot 8 \cdot UI, 60 + n \cdot 4 \cdot UI)$	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns

Table 11.13: MIPI AC Timing Specifications Part 1

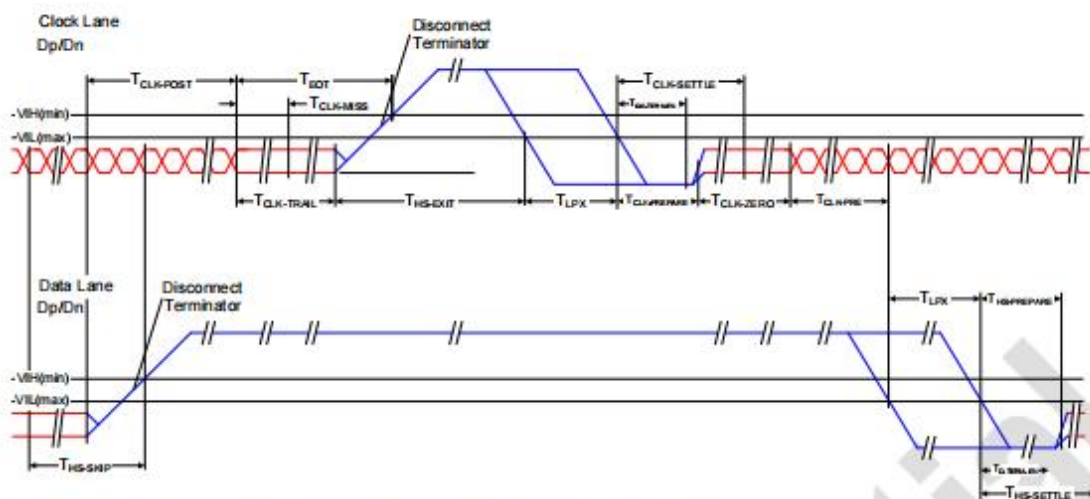


Figure 11.11: Switching the Clock Lane between Clock Transmission and Low-Power Mode

Parameter	Description	Min	Typ	Max	UNIT
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode.	$60 + 52 \cdot UI$	-	-	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	$8 \cdot UI$	-	-	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38	-	95	ns
$T_{CLK-PREPARE} + T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300	-	-	ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination.	-	-	38	ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns

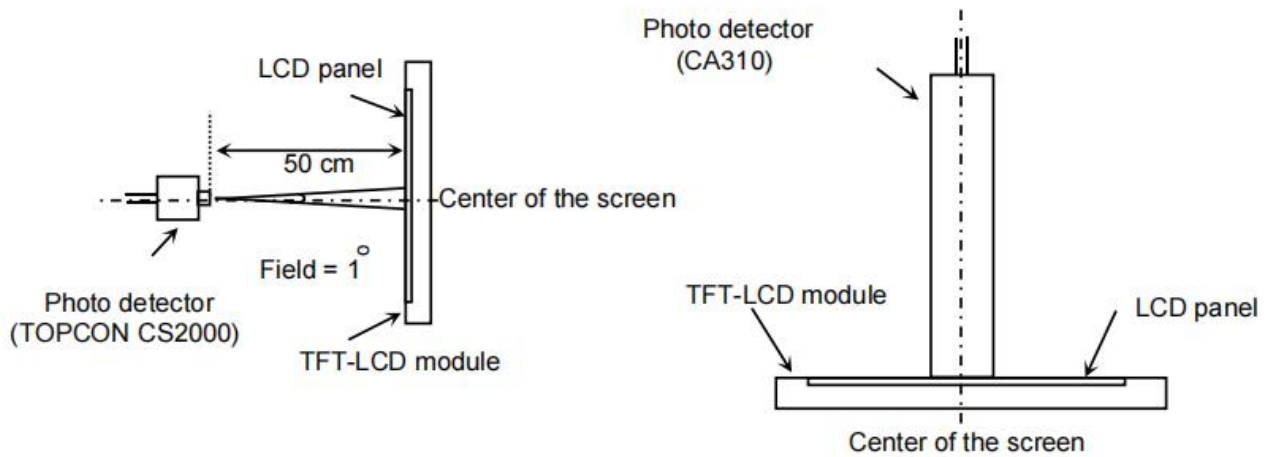
Table 11.14: MIPI AC Timing Specifications Part 2

8. Electro-Optical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time	Tr + Tf	$\theta_x = \theta_y = 0$	---	35	40	ms	Note 1
Contrast Ratio	CR		900	1200	---	---	Note 2
Transmittance	T%		3.6	4.2	---	%	
Color Chromaticity (CIE1931)	White	W x	$\theta_x = \theta_y = 0$	0.302	---	---	
		W y		0.338	---	---	
Viewing angle	θ_T	CR > 10	80	85	---	Deg.	Note 3
	θ_B		80	85	---		
	θ_L		80	85	---		
	θ_R		80	85	---		

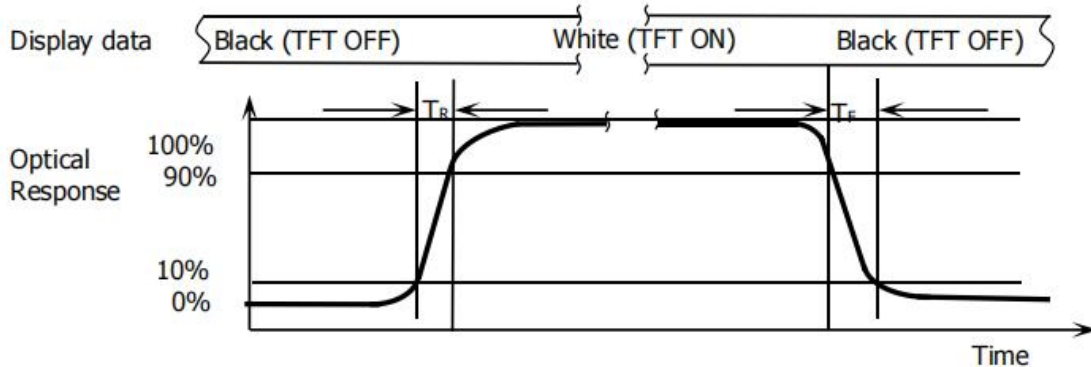
Optical measurements

Figure 1. Measurement Set Up



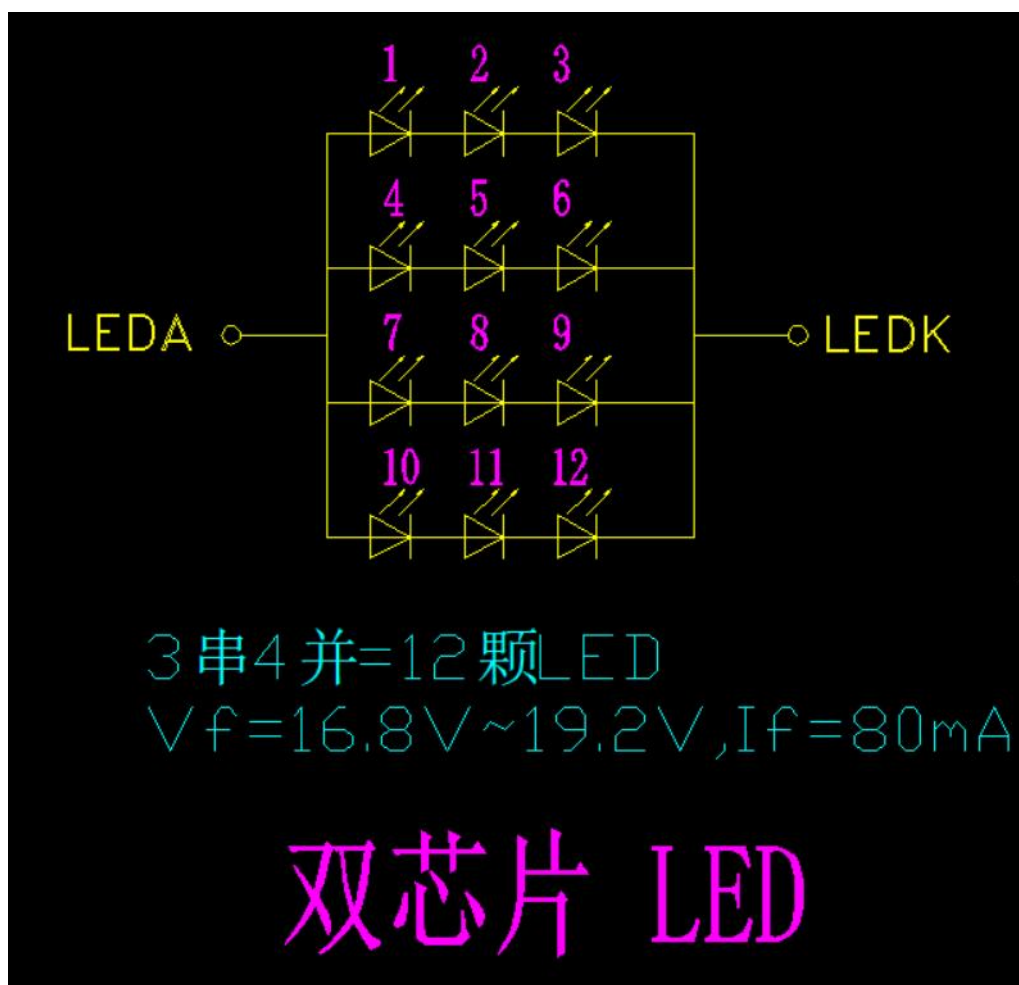
View angel range, uniformity, etc. measurement setup Flicker, measurement setup

Figure 2. Response Time Testing



The electro-optical response time measurements shall be made as shown in FIGURE 3 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Tr and 90% to 10% is Td.

Note(4) Backlight circuit



9. Inspection Standards

1. AQL(Acceptable Quality Level)

AQL of major and minor defect

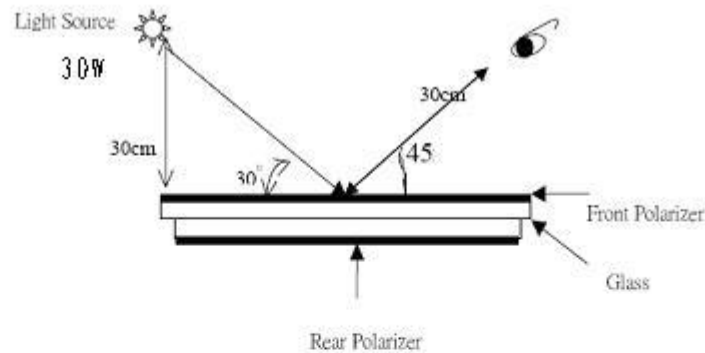
According to GB/T 2828-2003 ; , normal inspection, Class II

MAJOR DEFECT	MINOR DEFECT
0.65	1.5

2. Basic conditions for inspection

The LCM face to us, in normal environment, About an angle of incidence 30°, a distance of 30cm with normal eye, with an angle of 45° degree to check the products without uncovering the film!

(As shown below)

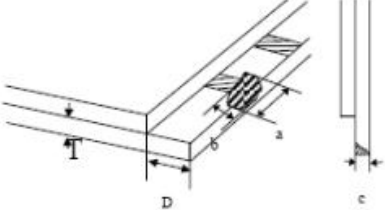
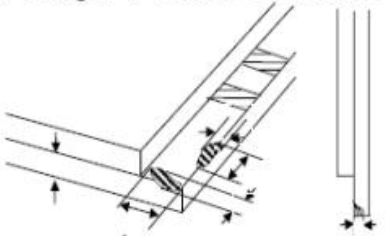


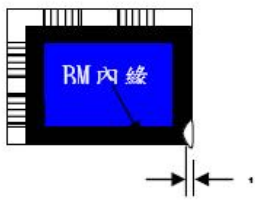
3. Inspection item and criteria

3.1 Visual inspection criterion in immobility

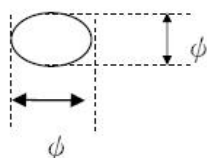
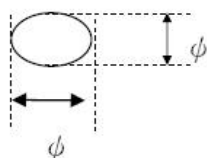
3.1.1 Glass defect

No	Defect item	Criteria	Remark
1	Dimension Unconformity (Major defect)	By Engineering Drawing	

No	Defect item	Criteria	Remark
2	Cracks (Major defect)	1.Linear cracks on panel 【Reject】 2. Nonlinear crack contrast by limited sample	
3	Glass extrude the conductive area (minor defect)	a: disregards and no influence assemblage 1) $b \leq 1/3$ Pin width(non bonding area) 【Accept】 2) bonding area $\leq 0.5\text{mm}$ 【Accept】	a:Length, b:Width
4	Pin-side , conductive area damaged (minor defect)	(a c : disregards) $b \leq 1/3$ of effective length for bonding electrode 【Accept】	a:Length, b: Width, c: Thickness  The diagram shows a 3D perspective of a rectangular panel with a grid of pins. A rectangular area on the side of a pin is shaded to represent damage. Dimensions are labeled: 'a' for the length of the damaged area along the pin, 'b' for the width of the damaged area across the panel, and 'c' for the thickness of the panel. A cross-section view on the right shows the panel thickness 'c' and the pin diameter 'D'.
5	Pin-side , non-conductive area damaged (minor defect)	1) Damage area don't touch the ITO (Inclueing contraposition mark,except scribing mark) 【Accept】 2) $c < T$ $b \leq BM$ 1/3 of width 【Accept】 3) $c = T$ b not touch the seal glue 【Accept】 4) a disregards	a:Length, b: Width, c: Thickness  The diagram shows a 3D perspective of a rectangular panel with a grid of pins. A rectangular area on the side of a pin is shaded to represent damage. Dimensions are labeled: 'a' for the length of the damaged area along the pin, 'b' for the width of the damaged area across the panel, and 'c' for the thickness of the panel. A cross-section view on the right shows the panel thickness 'c' and the pin diameter 'D'.

No	Defect item	Criteria	Remark
6	Non-pin-side damage (minor defect)	$c < T$ 1) b exceeds 1/3 BM $c = T$ b not touch the seal glue 【Reject】 【Reject】	c : Thickness b: width of damage 

3.1.2 LCD appearance defect (View area)

No	Defect item	Criteria		Remark
1	Fiber 、 glass cratch 、 polarizer scratch/folded (minor defect)	Specification	Allowable	note1: L : Length , W : Width note2: disregard if out of AA 
		$0.05\text{mm} < W \leq 0.1\text{mm};$ $L \leq 3.0\text{mm}$	1	
		$W > 0.1\text{mm}; L > 3.0\text{mm}$	0	
2	Polarizer bubble 、 concave and convex (minor defect)	$\psi \leq 0.2\text{mm}$	disregard	note 1: $\psi = (L+W)/2$; L : Length , W : Width note2: disregard if out of AA 
		$0.2\text{mm} < \psi \leq 0.3\text{mm}$	2	
		$0.3\text{mm} < \psi \leq 0.5\text{mm}$	1	
		$0.5\text{mm} < \psi$	0	
3	Black dots 、 dirty dots 、 impurities 、 eyewinker (Major defect)	$\psi \leq 0.15\text{mm}$	disregard	note2: disregard if out of AA 
		$0.15\text{mm} < \psi \leq 0.25\text{mm}$	2	
		$0.25\text{mm} < \psi \leq 0.3\text{mm}$	1	
		$0.3\text{mm} < \psi$	0	
4	Polarizer prick (Major defect)	$\psi \leq 0.1\text{mm}$	disregard	note1: $\psi = (L+W)/2$; L= Length , W=Width note2: the distance between two dots > 5mm
		$0.1\text{mm} < \psi \leq 0.25\text{mm}$	3	
		$\psi > 0.25\text{mm}$	0	

3.1.3 .FPC

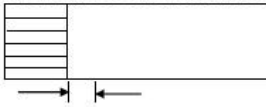
No	Defect item	Criteria		Remark
1	Copper screen peel (Major defect)	Copper screen peel 【 Reject】		
2	No release tape or peel (Major defect)	No release tape or peel 【 Reject】		
3	Dirty dot and impurity of FPC for customer using side (minor defect)	Specification	Allowable	note1: Cannot have stride ITO impurities
		$\psi \leq 0.25\text{mm}$	2	
		$\psi > 0.25$	0	

3.1.4 Black tape & Mara tape

1	FPC or H/S black tape shift (minor defect)	1.shift spec: 1)glue to the polarize 【 Reject】 2) IC bare 【 Reject】 2. left-and-right spec: 1) exceed of FPC edge or H-S edge 【 Reject】 2)IC bare 【 Reject】	
2	No black tape (Major defect)	No black tape 【 Reject】	
3	Tape position mistake (minor defect)	Not by engineering drawing 【 Reject】	
4	Mara tape defect (minor defect)	Peel before pulling the protecting film. 【 Reject】	

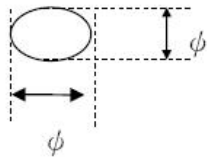
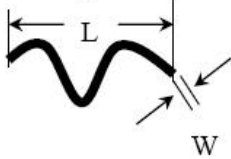
3.1.5 Silicon and Tuffy glue

No	Defect item	Criteria	Remark
1	Quantity of silicon (minor defect)	Uncover the ITO and circuit area. 【 Reject】	note: compared by engineering drawing.

No	Defect item	Criteria	Remark
2	Tuffy glue (minor defect)	1. Uncover the reveal copper area 【 Reject】 2. Cover layer 0.3mm(Min) ~ 3.0mm(Max) 【 accept】	note:if customer has special requirement , refer to the technical document. 
3	Depth of glue covering (minor defect)	Depth of glue covering overtop front Polarizer 【 Reject】	Except of the special requirement °

3.2 Electrical criteria

No	Defect item	Criteria	Remark
1	No display (Major defect)	No display 【 Reject】	
2	Missing line (Major defect)	Missing line 【 Reject】	
3	Seg-com light and dark (Major defect)	Seg-com light and dark 【 Reject】	ND filter 2% test
4	No display in immobility (Major defect)	No display in immobility 【 Reject】	
5	Flicker of Pattern (Major defect)	Flicker of Pattern 【 Reject】	
6	Mura (Major defect)	ND filter 2% test	
7	Over current (Major defect)	Over current 【 Reject】	
8	Voltage out of specification (Major defect)	Voltage out of specification 【 Reject】	
9	Pattern blur ,error code (Major defect)	Pattern blur ,error code 【 Reject】	
10	Dark light, Flicker (Major defect)	Dark light, Flicker 【 Reject】	

No	Defect item	Criteria	Remark	
11	Black/White dots 、 Dirty dots 、 eyewinker (Major defect)	Specification	Allowable	Note1: disregard if out of AA 
		$\psi \leq 0.15\text{mm}$	disregard	
		$0.15\text{mm} < \psi \leq 0.25\text{mm}$	2	
		$0.25\text{mm} < \psi \leq 0.3\text{mm}$	1	
		$0.3\text{mm} < \psi$	0	
12	Fiber 、 glass cratch 、 polarizer scratch/folded (minor defect)	$W \leq 0.03\text{mm}$	disregard	note1: L : Length 、 W : Width note2: disregard if out of AA 
		$0.03\text{mm} < W \leq 0.05\text{mm} ;$ $L \leq 3.0\text{mm}$	2	
		$0.05\text{mm} < W \leq 0.1\text{mm} ;$ $L \leq 3.0\text{mm}$	1	
		$W > 0.1\text{mm} ; L > 3.0\text{mm}$	0	

10.Records Of Version

Version	Revise Date	Page	Content
00	2025-10-16	all	New released